MachXO3L™ Family Data Sheet

Advance DS1047 Version 00.3, May 2014

MachXO3L Family Data Sheet Introduction

May 2014 Advance Data Sheet DS1047

Features

- **Solutions**
  - Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
  - Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
  - High IO/logic, lowest cost/IO, high IO devices for IO expansion applications
- **Flexible Architecture**
  - Logic Density ranging from 640 to 6.9K LUT4
  - High IO to LUT ratio with up to 325 IO pins
- **Advanced Packaging**
  - 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
  - 0.5mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x10 mm BGA packages with up to 269 IOs
  - 0.8mm pitch: 1K to 6.9K densities with up to 325 IOs in BGA packages
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRx2, DDRx4
- **High Performance, Flexible I/O Buffer**
- **Programmable sysIO™ buffer supports wide range of interfaces:**
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-Phy Emulated
  - Schmitt trigger inputs
  - Ideal for IO bridging applications
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **sysCLOCK PLL Support**
- **Non-volatile, Multi-time Programmable**
  - Single-chip, secure solution
  - Programmable through JTAG, I2C and SPI
- **TransFR Reconfiguration**
  - In-field logic update while IO holds the system state
- **Enhanced System Level Support**
  - On-chip Oscillator
  - Single power supply support
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Applications**
  - Consumer Electronics
  - Compute and Storage
  - Wireless Communications
  - Industrial Control Systems
  - Automotive System

Table 1-1. MachXO3L Family Selection Guide

Features		XO3L-640	XO3L-1300	XO3L-2100	XO3L-4300	XO3L-6900
LUTs		640	1300	2100	4300	6900
Distributed RAM (Kbits)		10	10	16	34	54
EBR SRAM (Kbits)		0	64	74	92	240
Number of PLLs		1	1	1	2	2
Hardened Functions:	I2C	2	2	2	2	2
	SPI	1	1	1	1	1
	Timer/Counter	1	1	1	1	1
	Oscillator	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		Yes	Yes	Yes	Yes	Yes
Packages				**IO**		
36-ball WLCSP[1] (2.5 mm x 2.5 mm, 0.4 mm)			28			
49-ball WLCSP[1] (3.2 mm x 3.2 mm, 0.4 mm)				38		
81-ball WLCSP[1] (3.8 mm x 3.8 mm, 0.4 mm)					63	
121-ball fcCSP[1] (6 mm x 6 mm, 0.5 mm)		100	100	100	100	
256-ball fcCSP[1] (9 mm x 9 mm, 0.5 mm)			206	206	206	206
324-ball fcCSP[1] (10 mm x 10 mm, 0.5 mm)				267	267	281
256-ball caBGA[2] (14 mm x 14mm, 0.8 mm)			206	206	206	206
324-ball caBGA[2] (15 mm x 15 mm, 0.8 mm)				279	279	279
400-ball caBGA[2] (17 mm x 17 mm, 0.8 mm)					335	335

1. Package is only available for E=1.2 V devices.
2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

Mach XO3L device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The device family spans from 640LUT to 6.9K LUT density which targets the low LUT count, small footprint Consumer Mobile Electronics market to the high LUT count, compute and speed intensive Communications and Compute and Storage markets.

Different LUT density points have focus features for different end applications. As such, the low LUT density end of the device family focuses its features on small foot print, low cost and IO bridging while the high LUT density end of the device family focuses its features on highest IO per LUT density, high-speed system interfaces, SERDES and DSP functions. All of these capabilities are offered with advance technology that supports instant-on capability with SRAM and Multi-time programmable Non-Volatile Configuration Memory (NVCM) support.

MachXO3L Family Data Sheet Architecture

Architecture Overview

The MachXO3L family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM or ROM in different width and depth configurations.

The MachXO3L registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

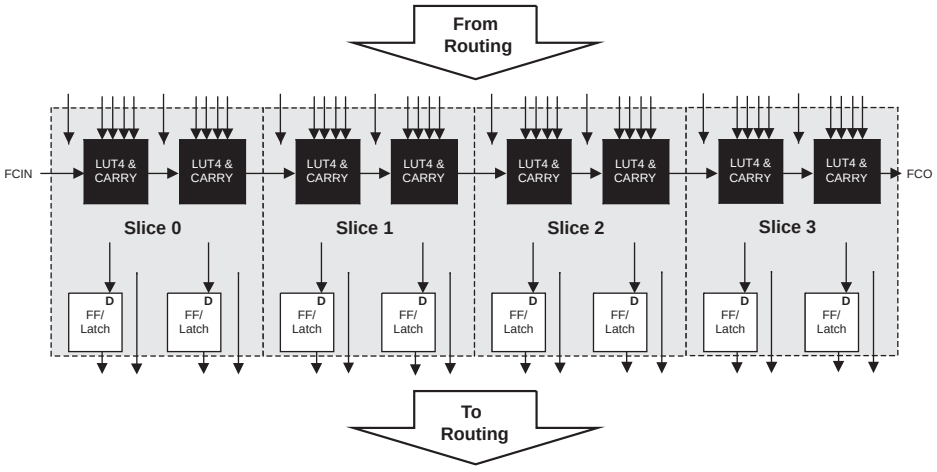
The MachXO3L architecture also provides sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L devices provide commonly used hardened functions such as SPI controller, I2C controller and timer/counter. These hardened functions can be accessed from the user logic through the routing resources. Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU (Programmable Functional Unit) Blocks

The core of the MachXO3L device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-1. Each slice contains two LUTs and two registers. There are a number of inputs and outputs associated with each PFU block that provides access to the routing resources.

Figure 2-1. PFU Block Diagram



sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

Embedded Block RAM (EBR)

The EBR consists of a 9-Kbit with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO. The sysMEM block can implement single port, dual port, pseudo dual port or FIFO (via external PFU) memories. Each block can be used in a variety of depths and widths.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO3L devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L devices, two adjacent PIOs can be combined to provide a complementary output driver pair. On certain PIO two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers but only certain half of the PIO pairs on specified IO banks can be configured as true LVDS transmit pairs.

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic. The input and output register blocks supports gearing logic to synchronize IO bandwidth to the fabric speed. The gearing logic for Double Data Rate (DDR), DDRx2, DDRx4 and 7:1 Gearing for display I/O standards are supported.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including: 3.3 V, 2.5 V, 1.8 V, 1.5 V and 1.2 V LVCMOS; 3.3 V LVTTL; Emulated Sub-LVDS; LVDS25; LVPECL; and BLVDS.

Configuration

MachXO3L configuration is supported via JTAG, I2C and SPI interfaces. The JTAG, Test Access Port (TAP), which supports in-system test and configuration capabilities while the sysCONFIG port supports serial configuration through SPI. The JTAG TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification.

MachXO3L device family supports instant-on security via proprietary NVCM (Non-Volatile Configuration Memory). This feature enables multi-time programmable capability for the user while providing a lowest cost non-volatile solution.

MachXO3L Family Data Sheet DC and Switching Characteristics

February 2014 Advance Data Sheet DS1047

Absolute Maximum Ratings[1, 2, 3, 4]

	MachXO3L E (1.2V)	MachXO3L C (2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32 V	-0.5 to 3.75 V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75 V	-0.5 to 3.75 V
I/O Tri-state Voltage Applied[5]	-0.5 to 3.75 V	-0.5 to 3.75 V
Dedicated Input Voltage Applied	-0.5 to 3.75 V	-0.5 to 3.75 V
Storage Temperature (Ambient)	-55 °C to 125 °C	-55 °C to 125 °C
Junction Temperature (T_J)	-40 °C to 125 °C	-40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.
5. The dual function I^2C pins SCL and SDA are limited to -0.25V to 3.75V or to -0.3V with a duration of <20ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for C devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

To be completed

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	-10	—	10	µA
		Clamp OFF and V_{CCIO} - 0.97 V < V_{IN} < V_{CCIO}	-175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} - 0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < $V_{IN} < V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	-30	—	-309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < $V_{IN} < V_{CCIO}$	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	-309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For true LVDS output pins in MachXO3L devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1280, MachXO3L sysIO Usage Guide.

Static Supply Current – C/E Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L-1300C	4.80	mA
		LCMXO3L-2100C	4.80	mA
		LCMXO3L-4300C	8.45	mA
		LCMXO3L-6900C	12.87	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5V	All devices	0	mA

1. For further information on supply current, please refer to TN1286, Power Estimation and Management for MachXO3L Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25°C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO3L peak start-up current data, use the Power Calculator tool.

Programming and Erase Supply Current – C/E Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO3L-1300C	22.1	mA
		LCMXO3L-2100C	22.1	mA
		LCMXO3L-4300C	26.8	mA
		LCMXO3L-6900C	33.2	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1286, Power Estimation and Management for MachXO3L Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. For the dedicated LVDS buffers

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
							12	-12
							16	-16
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
							12	-12
							16	-16
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
							12	-12
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	-2
							8	-6
					0.2	V_{CCIO} - 0.2	0.1	-0.1

1. MachXO3L devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO3L devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1280, MachXO3 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.
4. The average DC current drawn by I/O pins shall not exceed 8 mA.

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L PLD family.

LVDS

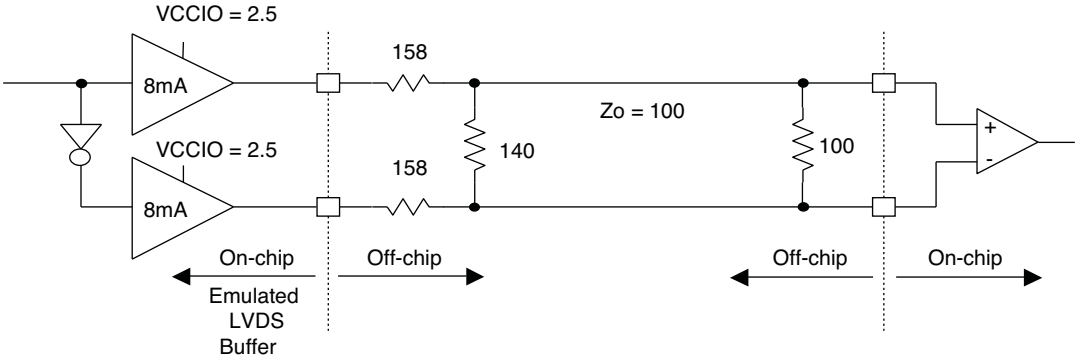
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3	0	—	2.605	V
		V_{CCIO} = 2.5	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO3L devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO3L family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

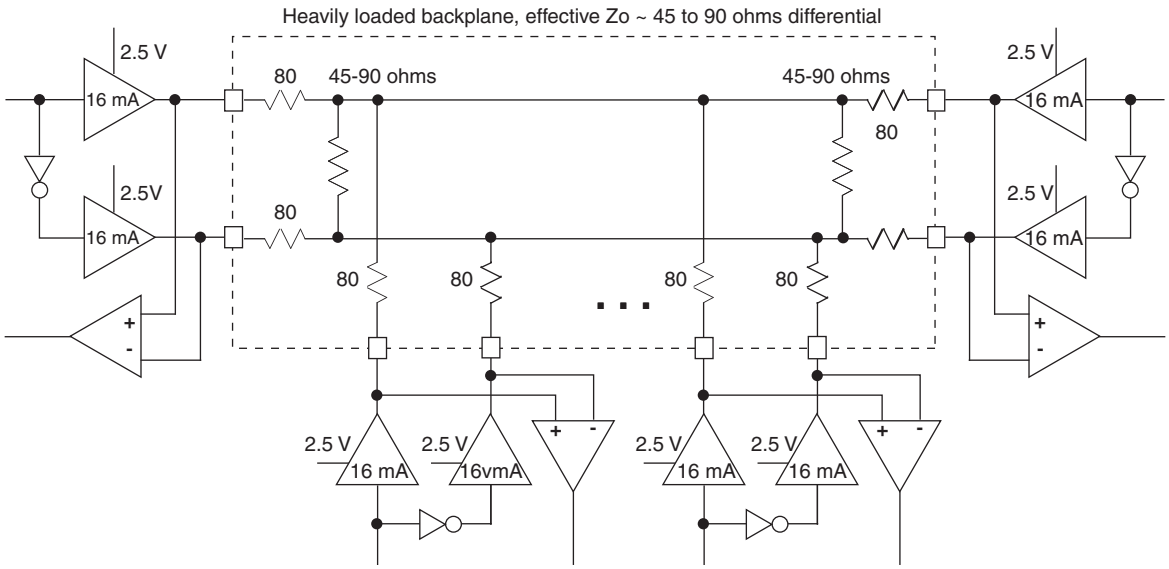


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	10	10	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO3L family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

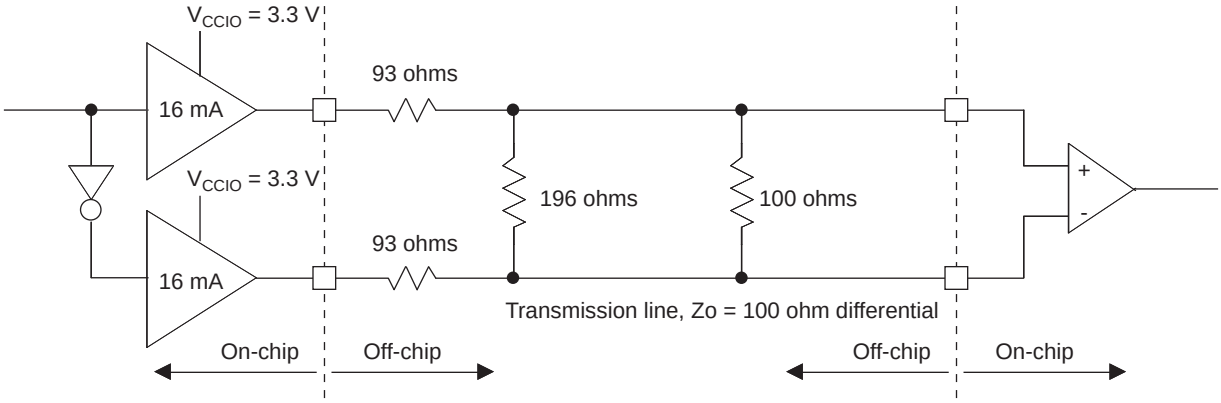


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	10	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

MIPI D-PHY Emulation

MachXO3L devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LS (Low Speed) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Speed IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors

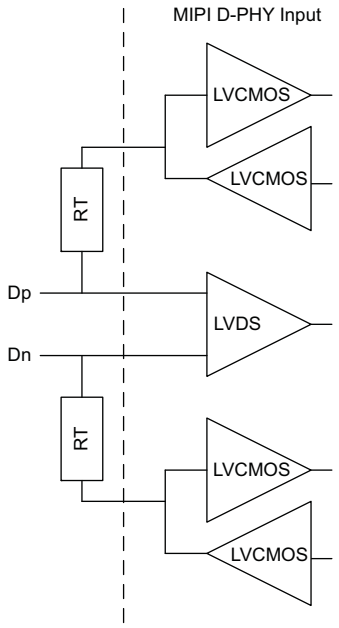


Table 3-4. MIPI DC Conditions

	Description	Typ.	Units
Receiver			
External Termination			
RT	1% external resistor with VCCIO=2.5V	50	Ohms
	1% external resistor with VCCIO=3.3V	50	Ohms
High Speed			
VCCIO	VCCIO of the Bank with LVDS25E input buffer	2.5	V
	VCCIO of the Bank with LVDS25E input buffer	3.3	V
VCMRX	Common-mode voltage HS receive mode	200	V
VIDTH	Differential input high threshold		mV
VIDTL	Differential input low threshold		mV
VIHHS	Single-ended input high voltage	300	mV
VILHS	Single-ended input low voltage	100	mV
VTERM-EN	Single-ended threshold for HS termination enable		mV
ZID	Differential input impedance	100	Ohms
Low Speed			
VCCIO	VCCIO of the Bank with LVCMOS12D 6mA drive bidirectional IO buffer	1.2	V
VIH	Logic 1 input voltage		V
VIL	Logic 0 input voltage, not in ULP State		V
VIL-ULPS	Logic 0 input voltage, ULP State		V
VHYST	Input hysteresis		V

Figure 3-5. MIPI D-PHY Output Using External Resistors

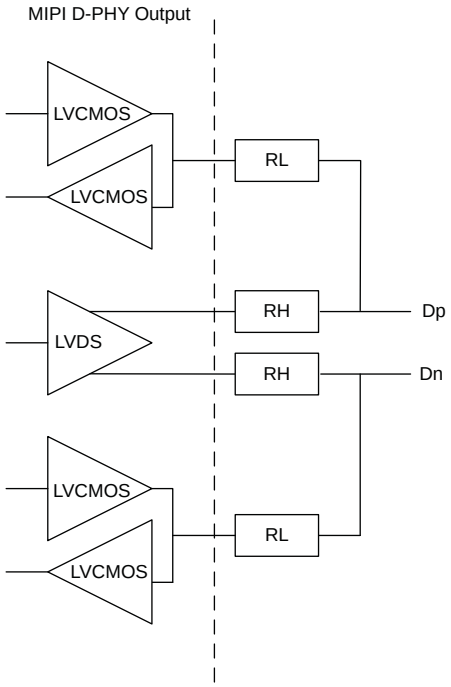


Table 3-5. MIPI D-PHY Output DC Conditions[1]

	Description	Typ.	Units
Transmitter			
External Termination			
RL	1% external resistor with VCCIO = 2.5V	50	Ohms
	1% external resistor with VCCIO = 3.3V	50	Ohms
RH	1% external resistor	330	Ohms
High Speed			
VCCIO	VCCIO of the Bank with LVDS25E output buffer	2.5	
	VCCIO of the Bank with LVDS25E output buffer	3.3	V
VCMTX	HS transmit static common mode voltage	200	mV
VOD	HS transmit differential voltage	200	mV
VOHHS	HS output high voltage		V
ZOS	Single ended output impedance		Ohms
ΔZOS	Single ended output impedance mismatch		Ohms
Low Speed			
VCCIO	VCCIO of the Bank with LVCMOS12D 6mA drive bidirectional IO buffer	1.2	V
VOH	Output high level	1.2	V
VOL	Output low level	0	V
ZOLP	Output impedance of LP transmitter		V

Typical Building Block Function Performance – C/E Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25		MHz
LVDS25E		MHz
BLVDS25		MHz
BLVDS25E		MHz
MLVDS25		MHz
MLVDS25E		MHz
LVPECL33		MHz
LVPECL33E		MHz
LVTTL33		MHz
LVTTL33D		MHz
LVCMOS33		MHz
LVCMOS33D		MHz
LVCMOS25		MHz
LVCMOS25D		MHz
LVCMOS18		MHz
LVCMOS18D		MHz
LVCMOS15		MHz
LVCMOS15D		MHz
LVCMOS12		MHz
LVCMOS12D		MHz

MachXO3L External Switching Characteristics – C/E Devices[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO3L devices	—	388	—	323	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L devices	0.5	—	0.6	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L-1300	—	867	—	897	ps
		MachXO3L-2100	—	867	—	897	ps
		MachXO3L-4300	—	865	—	892	ps
		MachXO3L-6900	—	902	—	942	ps
Edge Clock							
f_{MAX_EDGE}[7]	Frequency for Edge Clock	MachXO3L	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t_{PD}	Best case propagation delay through one LUT-4	All MachXO3L devices	—	6.72	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t_{CO}	Clock to Output - PIO Output Register	MachXO3L-1300	—	7.46	—	7.66	ns
		MachXO3L-2100	—	7.46	—	7.66	ns
		MachXO3L-4300	—	7.51	—	7.71	ns
		MachXO3L-6900	—	7.54	—	7.75	ns
t_{SU}	Clock to Data Setup - PIO Input Register	MachXO3L-1300	-0.20	—	-0.20	—	ns
		MachXO3L-2100	-0.20	—	-0.20	—	ns
		MachXO3L-4300	-0.23	—	-0.23	—	ns
		MachXO3L-6900	-0.23	—	-0.23	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	MachXO3L-1300	1.89	—	2.13	—	ns
		MachXO3L-2100	1.89	—	2.13	—	ns
		MachXO3L-4300	1.94	—	2.18	—	ns
		MachXO3L-6900	1.98	—	2.23	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L-1300	1.61	—	1.76	—	ns
		MachXO3L-2100	1.61	—	1.76	—	ns
		MachXO3L-4300	1.66	—	1.81	—	ns
		MachXO3L-6900	1.53	—	1.67	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L-1300	-0.23	—	-0.23	—	ns
		MachXO3L-2100	-0.23	—	-0.23	—	ns
		MachXO3L-4300	-0.25	—	-0.25	—	ns
		MachXO3L-6900	-0.21	—	-0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3 devices	—	388	—	323	MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Edge Clock without PLL)							
t_{COE}	Clock to Output - PIO Output Register	MachXO3L-1300	—	7.53	—	7.76	ns
		MachXO3L-2100	—	7.53	—	7.76	ns
		MachXO3L-4300	—	7.45	—	7.68	ns
		MachXO3L-6900	—	7.53	—	7.76	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	MachXO3L-1300	-0.19	—	-0.19	—	ns
		MachXO3L-2100	-0.19	—	-0.19	—	ns
		MachXO3L-4300	-0.16	—	-0.16	—	ns
		MachXO3L-6900	-0.19	—	-0.19	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	MachXO3L-1300	1.97	—	2.24	—	ns
		MachXO3L-2100	1.97	—	2.24	—	ns
		MachXO3L-4300	1.89	—	2.16	—	ns
		MachXO3L-6900	1.97	—	2.24	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L-1300	1.56	—	1.69	—	ns
		MachXO3L-2100	1.56	—	1.69	—	ns
		MachXO3L-4300	1.74	—	1.88	—	ns
		MachXO3L-6900	1.66	—	1.81	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L-1300	-0.23	—	-0.23	—	ns
		MachXO3L-2100	-0.23	—	-0.23	—	ns
		MachXO3L-4300	-0.34	—	-0.34	—	ns
		MachXO3L-6900	-0.29	—	-0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output - PIO Output Register	MachXO3L-1300	—	5.98	—	6.01	ns
		MachXO3L-2100	—	5.98	—	6.01	ns
		MachXO3L-4300	—	5.99	—	6.02	ns
		MachXO3L-6900	—	6.02	—	6.06	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	MachXO3L-1300	0.36	—	0.36	—	ns
		MachXO3L-2100	0.36	—	0.36	—	ns
		MachXO3L-4300	0.35	—	0.35	—	ns
		MachXO3L-6900	0.34	—	0.34	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	MachXO3L-1300	0.42	—	0.49	—	ns
		MachXO3L-2100	0.42	—	0.49	—	ns
		MachXO3L-4300	0.43	—	0.50	—	ns
		MachXO3L-6900	0.46	—	0.54	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L-1300	2.87	—	3.18	—	ns
		MachXO3L-2100	2.87	—	3.18	—	ns
		MachXO3L-4300	2.96	—	3.28	—	ns
		MachXO3L-6900	3.05	—	3.35	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L-1300	-0.83	—	-0.83	—	ns
		MachXO3L-2100	-0.83	—	-0.83	—	ns
		MachXO3L-4300	-0.87	—	-0.87	—	ns
		MachXO3L-6900	-0.91	—	-0.91	—	ns

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8]							
t_{DVA}	Input Data Valid After CLK	All MachXO3L devices, all sides	—		—		UI
t_{DVE}	Input Data Hold After CLK			—		—	UI
f_{DATA}	DDRX1 Input Data Speed		—		—		Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—		—		MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8]							
t_{SU}	Input Data Setup Before CLK	All MachXO3L devices, all sides		—		—	ns
t_{HO}	Input Data Hold After CLK			—		—	ns
f_{DATA}	DDRX1 Input Data Speed		—		—		Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—		—		MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After CLK	MachXO3L devices, bottom side only	—		—		UI
t_{DVE}	Input Data Hold After CLK			—		—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—		—		Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before CLK	MachXO3L devices, bottom side only		—		—	ns
t_{HO}	Input Data Hold After CLK			—		—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—		—		Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L devices, bottom side only	—		—		UI
t_{DVE}	Input Data Hold After ECLK			—		—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—		—		Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3L devices, bottom side only		—		—	ns
t_{HO}	Input Data Hold After ECLK			—		—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—		—		Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L devices, bottom side only	—		—		UI
t_{DVE}	Input Data Hold After ECLK			—		—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—		—		Mbps
f_{DDR71}	DDR71 ECLK Frequency		—		—		MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—		—	90	MHz
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Centered							
t_{SU}	Input Data Setup Before ECLK	All MachXO3L devices, bottom side only					ns
t_{HO}	Input Data Hold After ECLK						ns
f_{DATA}	MIPI D-PHY Input Data Speed						Mbps
f_{DDRX4}	MIPI D-PHY ECLK Frequency						MHz
f_{SCLK}	SCLK Frequency						MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	All MachXO3L devices, all sides	—		—		ns
t_{DIB}	Output Data Invalid Before CLK Output		—		—		ns
f_{DATA}	DDRX1 Output Data Speed		—		—		Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—		—		MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L devices, all sides		—		—	ns
t_{DVA}	Output Data Valid After CLK Output			—		—	ns
f_{DATA}	DDRX1 Output Data Speed		—		—		Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—		—		MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L devices, top side only	—		—		ns
t_{DIB}	Output Data Invalid Before CLK Output		—		—		ns
f_{DATA}	DDRX2 Serial Output Data Speed		—		—		Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L devices, top side only		—		—	ns
t_{DVA}	Output Data Valid After CLK Output			—		—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—		—		Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L devices, top side only	—		—		ns
t_{DIB}	Output Data Invalid Before CLK Output		—		—		ns
f_{DATA}	DDRX4 Serial Output Data Speed		—		—		Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L devices, top side only		—		—	ns
t_{DVA}	Output Data Valid After CLK Output			—		—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—		—		Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L devices, top side only.	—		—		ns
t_{DVA}	Output Data Valid After CLK Output		—		—		ns
f_{DATA}	DDR71 Serial Output Data Speed		—		—		Mbps
f_{DDR71}	DDR71 ECLK Frequency		—		—		MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—		—		MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_TX.ECLK.Centered							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L devices, top side only.	—		—		ns
t_{DVA}	Output Data Valid After CLK Output		—		—		ns
f_{DATA}	MIPI D-PHY Output Data Speed		—		—		Mbps
f_{DDRX4}	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—		—		MHz
f_{SCLK}	SCLK Frequency		—		—		MHz

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
6. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).
7. This number for general purpose usage. Duty cycle tolerance is +/-10%.
8. Duty cycle is +/- 5% for system usage.
9. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

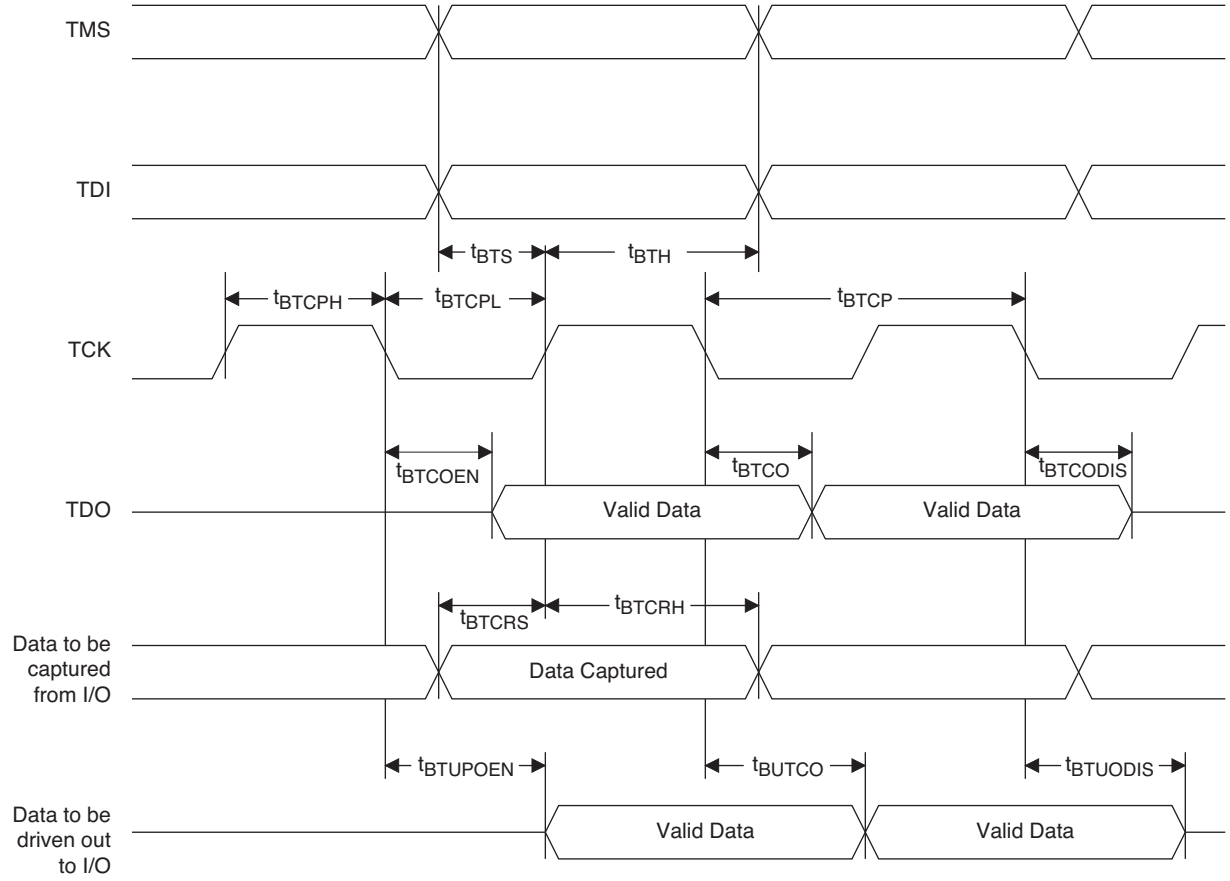
Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		-75	75	%
t_{PH}[4]	Output Phase Accuracy		-6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100MHz	—	150	ps p-p
		f_{OUT} < 100MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100MHz	—	180	ps p-p
		f_{OUT} < 100MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100MHz	—	160	ps p-p
		f_{PFD} < 100MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100MHz	—	230	ps p-p
		f_{OUT} < 100MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100MHz	—	230	ps p-p
		f_{OUT} < 100MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t_{W}	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-6. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
All Configuration Modes				
t_{PRGM}	PROGRAMN low pulse accept	55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection	—	25	ns
t_{INITL}	INITN low time	—	55	us
$t_{DPPINIT}$	PROGRAMN low to INITN low	—	70	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low	—	80	ns
t_{IODISS}	PROGRAMN low to I/O disable	—	120	ns
Slave SPI				
f_{MAX}	CCLK clock frequency	—	66	MHz
t_{CCLKH}	CCLK clock pulse width high	7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low	7.5	—	ns
t_{STSU}	CCLK setup time	2	—	ns
t_{STH}	CCLK hold time	0	—	ns
t_{STCO}	CCLK falling edge to valid output	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	10	ns
t_{SCS}	Chip select high time	25	—	ns
t_{SCSS}	Chip select setup time	3	—	ns
t_{SCSH}	Chip select hold time	3	—	ns
Master SPI				
f_{MAX}	MCLK clock frequency	—	133	MHz
t_{MCLKH}	MCLK clock pulse width high	3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low	3.75	—	ns
t_{STSU}	MCLK setup time	5	—	ns
t_{STH}	MCLK hold time	1	—	ns
t_{CSSPI}	INITN high to chip select low	100	200	ns
t_{MCLK}	INITN high to first MCLK edge	0.75	1	us

I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	KHz

1. MachXO3L supports the following modes:
   - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-7 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-7. Output Test Load, LVTTL and LVCMOS Standards

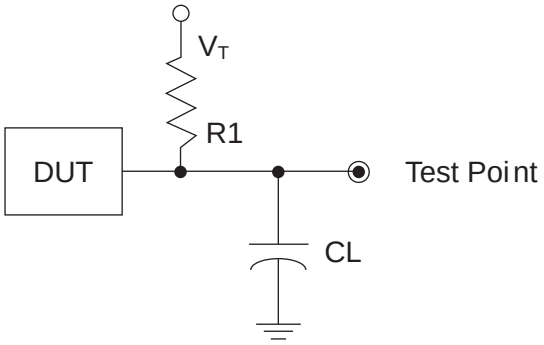


Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

Pin Information Summary

	MachXO3L -1300	MachXO3L-2100			MachXO3L-4300				MachXO3L-6900		
	CABGA 256	WLCSP 49	CABGA 256	CABGA 324	WLCSP 81	CABGA 256	CABGA 324	CABGA 400	CABGA 256	CABGA 324	CABGA 400
General Purpose IO per Bank											
Bank 0	50	19	50	71	29	50	71	83	50	71	83
Bank 1	52	0	52	68	0	52	68	84	52	68	84
Bank 2	52	13	52	72	20	52	72	84	52	72	84
Bank 3	16	0	16	24	7	16	24	28	16	24	28
Bank 4	16	0	16	16	0	16	16	24	16	16	24
Bank 5	20	6	20	28	7	20	28	32	20	28	32
Total General Purpose Single Ended IO	206	38	206	279	63	206	279	335	206	279	335
Differential IO per Bank											
Bank 0	25	10	25	36	15	25	36	42	25	36	42
Bank 1	26	0	26	34	0	26	34	42	26	34	42
Bank 2	26	6	26	36	10	26	36	42	26	36	42
Bank 3	8	0	8	12	3	8	12	14	8	12	14
Bank 4	8	0	8	8	0	8	8	12	8	8	12
Bank 5	10	3	10	14	3	10	14	16	10	14	16
Total General Purpose Differential IO	103	19	103	140	31	103	140	168	103	140	168
Dual Function IO	33	25	33	37	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes											
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	5	14	18	10	18	18	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	6	14	18	10	18	18	21	20	21	21
High Speed Differential Outputs											
Bank 0	14	5	14	18	10	18	18	21	20	21	21
VCCIO Pins											
Bank 0	4	2	4	4	3	4	4	5	4	4	5
Bank 1	4	0	4	4	0	4	4	5	4	4	5
Bank 2	4	1	4	4	2	4	4	5	4	4	5
Bank 3	1	0	1	2	1	1	2	2	1	2	2
Bank 4	2	0	2	2	0	2	2	2	2	2	2
Bank 5	1	1	1	2	1	1	2	2	1	2	2
VCC	8	2	8	10	4	8	10	10	8	10	10
GND	24	4	24	16	6	24	16	33	24	16	33
NC	1	0	1	0	0	1	0	0	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	256	49	256	324	81	256	324	400	256	324	400

MachXO3L Family Data Sheet Ordering Information

MachXO3L Part Number Description

LCMXO3L – XXXXX – XXXXXXX XX

Device Family
Low Density MachXO3L FPGA

Logic Capacity
1300 = 1280 LUTs
2100 = 2112 LUTs
4300 = 4320 LUTs
6900 = 6864 LUTs

Supply Voltage
C = 2.5 V/3.3 V
E = 1.2 V

Speed
5 = Slowest
6 = Fastest

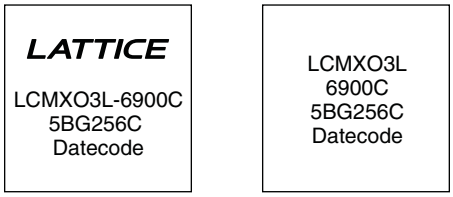
Shipping Method
Blank = Trays
TR = Tape and Reel
TR50 = WLCSP Package, 50 parts per reel
TR1K = WLCSP Package, 1,000 parts per re

Grade
C = Commercial
I = Industrial

Package
UWG49 = 49-Ball Halogen-Free WLCSP (0.4 mm Pitch)
UWG81 = 81-Ball Halogen-Free WLCSP (0.4 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
BG324 = 324-Ball Halogen-Free caBGA (0.8 mm Pitch)
BG400 = 400-Ball Halogen-Free caBGA (0.8 mm Pitch)

Ordering Information

MachXO3L devices have top-side markings, for commercial and industrial grades, as shown below:



Note: Markings are abbreviated for small packages.

Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	-5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	-6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	-5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	-5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	-5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	-5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	-5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	-5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49CTR	2100	1.2 V	-5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR50	2100	1.2 V	-5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR1K	2100	1.2 V	-5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49ITR	2100	1.2 V	-5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR50	2100	1.2 V	-5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR1K	2100	1.2 V	-5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	-5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	-6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO3L-1300C-5BG256C	1300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-5BG256I	1300	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO3L-1300C-6BG256C	1300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-6BG256I	1300	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND

MachXO3L Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO3L family are available on the Lattice web site.

- TN1282, MachXO3L sysCLOCK PLL Design and Usage Guide
- TN1281, Implementing High-Speed Interfaces with MachXO3L Devices
- TN1280, MachXO3L sysIO Usage Guide
- TN1279, MachXO3L Programming and Configuration Usage Guide
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO3L Device Pinout Files
- Thermal Management document
- Lattice design tools

MachXO3L Family Data Sheet Revision History

May 2014 **Advance Data Sheet DS1047**

Date	Version	Section	Change Summary
February 2014	00.1	—	Initial release.
	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
May 2014	00.3	Introduction	Updated Features section. Changed Advanced Packaging detail on the number of IOs for 0.4 mm pitch.
			Updated Table 1-1, MachXO3L Family Selection Guide.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.