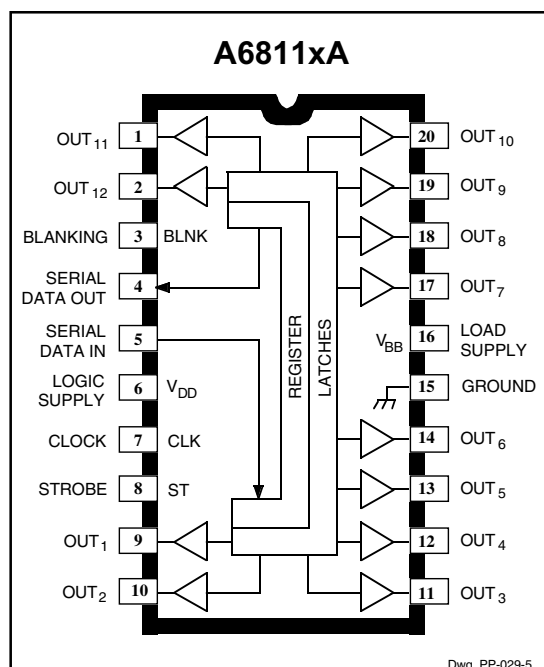


# 6811

Data Sheet  
26182-120

**PRELIMINARY INFORMATION**  
(subject to change without notice)  
May 15, 2000

## ***DABiC-IV, 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER***



### **ABSOLUTE MAXIMUM RATINGS** at $T_A = 25^\circ\text{C}$

Logic Supply Voltage, $V_{DD}$	7.0 V
Driver Supply Voltage, $V_{BB}$	60 V
Continuous Output Current Range, $I_{OUT}$	-40 mA to +15 mA
Input Voltage Range, $V_{IN}$	-0.3 V to $V_{DD} + 0.3$ V
Package Power Dissipation, $P_D$	See Graph
Operating Temperature Range, $T_A$	
(Suffix 'E-')	-40°C to +85°C
(Suffix 'S-')	-20°C to +85°C
Storage Temperature Range, $T_S$	-55°C to +125°C

*Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.*

The A6811- devices combine a 12-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6811- features an increased data input rate (compared with the older UCN/UCQ5811A) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 V or 5 V logic supply, typical serial-data input rates are up to 33 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6809- and A6810- (10 bits), A6812- (20 bits), and A6818- (32 bits).

The A6811- output source drivers are npn Darlington, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The pnp active pull-downs will sink at least 2.5 mA.

Two temperature ranges are available for optimum performance in commercial (suffix S-) or industrial (suffix E-) applications. Package styles are provided for through-hole DIP (suffix -A) and surface-mount SOIC or PLCC (suffix -LW or -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow all devices to source 25 mA from all outputs continuously at up to 83°C.

### **FEATURES**

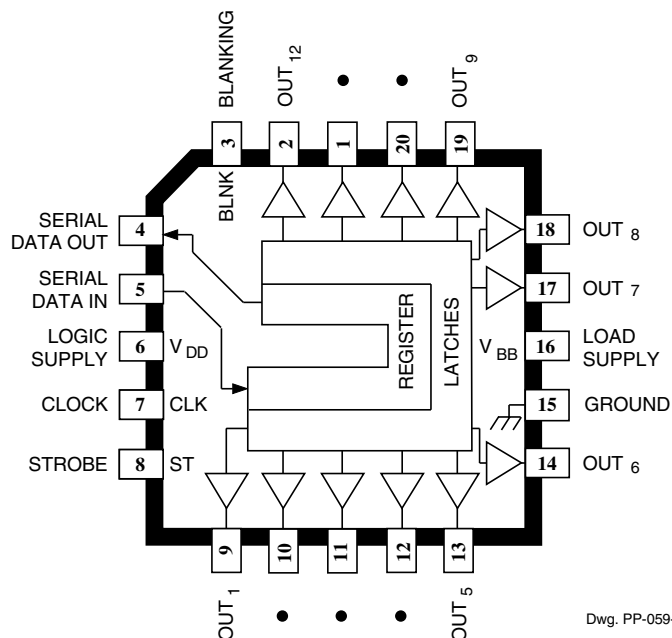
- Controlled Output Slew Rate
- High-Speed Data Storage
- 60 V Minimum Output Breakdown
- High Data Input Rate
- PNP Active Pull-Downs
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Improved Replacements for SN75512B, UCN5811-, and UCQ5811-

Complete part number includes a suffix to identify operating temperature range (E- or S-) and package type (-A, -EP, or -LW). Always order by complete part number, e.g., **A6811SLW**.

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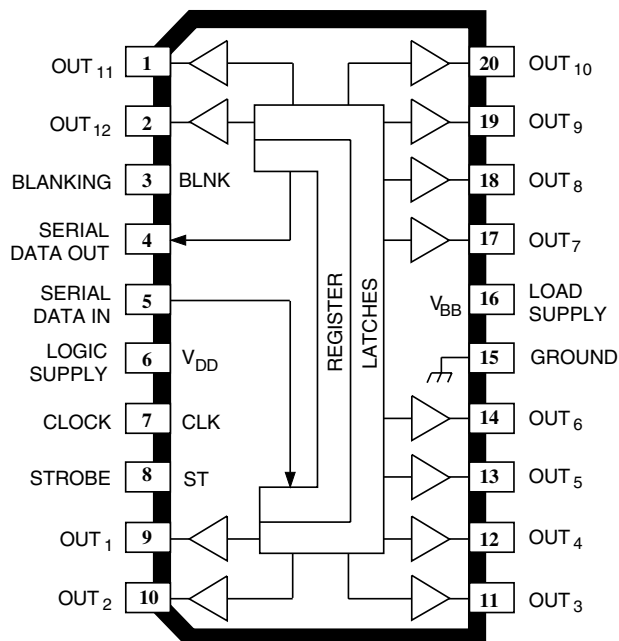
## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

**A6811xEP**



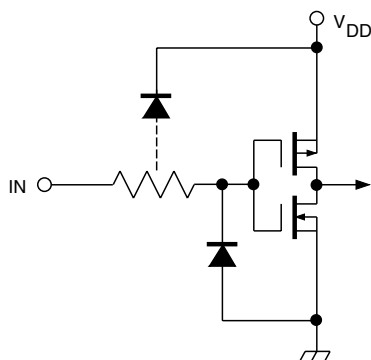
Dwg. PP-059-4

**A6811xLW**



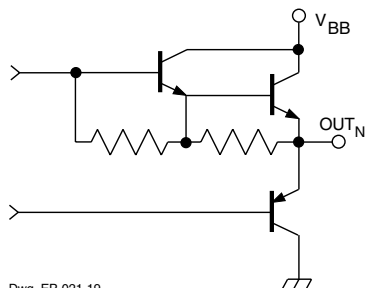
Dwg. PP-029-6

**TYPICAL INPUT CIRCUIT**

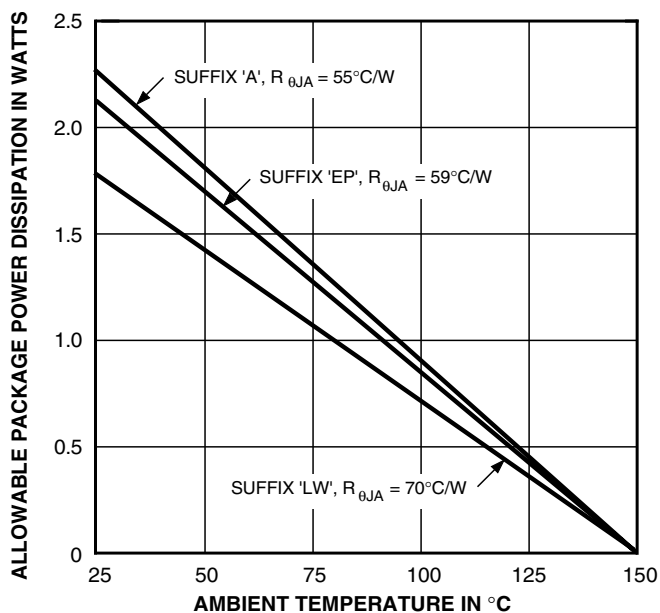


Dwg. EP-010-5

**TYPICAL OUTPUT DRIVER**



Dwg. EP-021-19

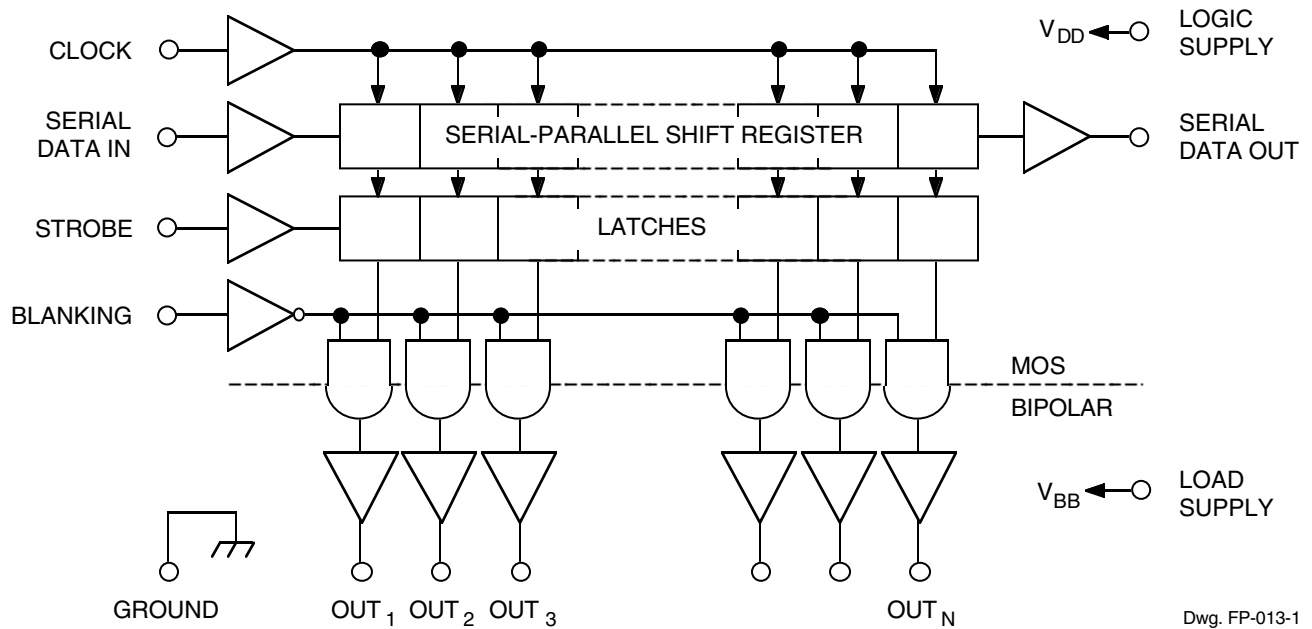


Dwg. GP-024-5

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## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

### FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013-1

### TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>
H		H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
L		L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
X		R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>	R <sub>N</sub>														
		X	X	X	...	X	X	X	L	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>							
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	P <sub>N</sub>	H	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	L	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>
											X	X	X	...	X	X	H	L	L	L	...	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

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## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

**ELECTRICAL CHARACTERISTICS** at  $T_A = +25^\circ\text{C}$  (A6811S-) or over operating temperature range (A6811E-),  $V_{BB} = 60\text{ V}$  unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ $V_{DD} = 3.3\text{ V}$			Limits @ $V_{DD} = 5\text{ V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 0\text{ V}$	—	<-0.1	-15	—	<-0.1	-15	$\mu\text{A}$
Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -25\text{ mA}$	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1\text{ mA}$	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	$V_{OUT} = 5\text{ V to } V_{BB}$	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	<0.01	1.0	—	<0.01	1.0	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN} = 0\text{ V}$	—	<-0.01	-1.0	—	<-0.01	-1.0	$\mu\text{A}$
Input Clamp Voltage	$V_{IK}$	$I_{IN} = -200\text{ }\mu\text{A}$	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\text{ }\mu\text{A}$	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200\text{ }\mu\text{A}$	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	$f_c$		10	33	—	10	33	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	1.7	3.5	—	1.7	3.5	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	$\mu\text{A}$
Blanking-to-Output Delay	$t_{dis(BQ)}$	$C_L = 30\text{ pF}$ , 50% to 50%	—	0.7	2.0	—	0.7	2.0	$\mu\text{s}$
	$t_{en(BQ)}$	$C_L = 30\text{ pF}$ , 50% to 50%	—	1.8	3.0	—	1.8	3.0	$\mu\text{s}$
Strobe-to-Output Delay	$t_{p(STH-QL)}$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	—	0.7	2.0	—	0.7	2.0	$\mu\text{s}$
	$t_{p(STH-QH)}$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	—	1.8	3.0	—	1.8	3.0	$\mu\text{s}$
Output Fall Time	$t_f$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	$\mu\text{s}$
Output Rise Time	$t_r$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	$\mu\text{s}$
Output Slew Rate	$dV/dt$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	4.0	—	20	4.0	—	20	V/ $\mu\text{s}$
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	$I_{OUT} = \pm 200\text{ }\mu\text{A}$	—	50	—	—	50	—	ns

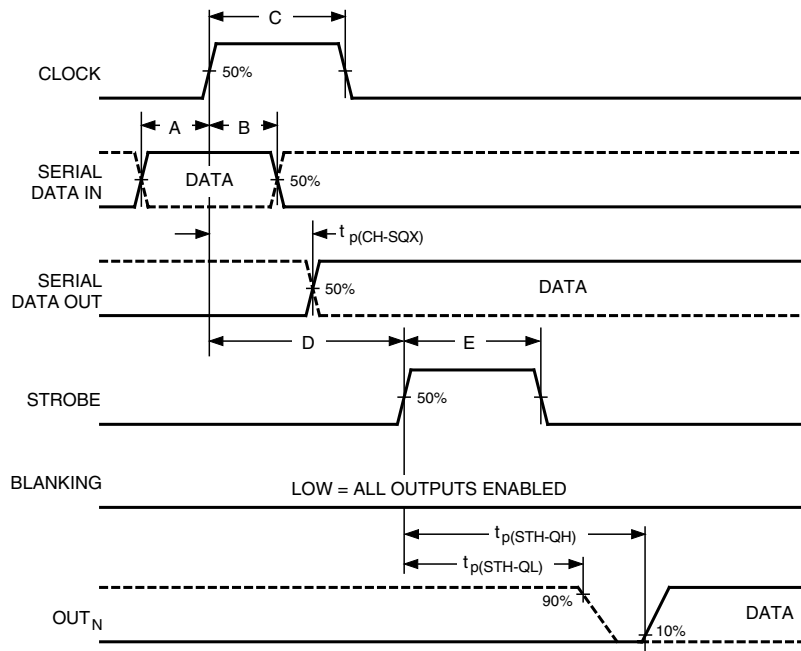
Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical data is for design information only and is at  $T_A = +25^\circ\text{C}$ .

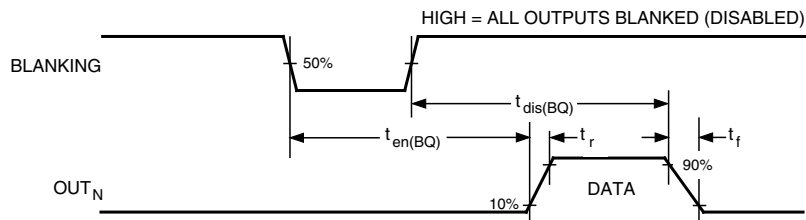
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## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

### TIMING REQUIREMENTS and SPECIFICATIONS (Logic Levels are $V_{DD}$ and Ground)



Dwg. WP-029



Dwg. WP-030

- A.** Data Active Time Before Clock Pulse  
(Data Set-Up Time),  $t_{su(D)}$  ..... **25 ns**
- B.** Data Active Time After Clock Pulse  
(Data Hold Time),  $t_{h(D)}$  ..... **25 ns**
- C.** Clock Pulse Width,  $t_w(CH)$  ..... **50 ns**
- D.** Time Between Clock Activation and Strobe,  $t_{su(C)}$  ..... **100 ns**
- E.** Strobe Pulse Width,  $t_w(STH)$  ..... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

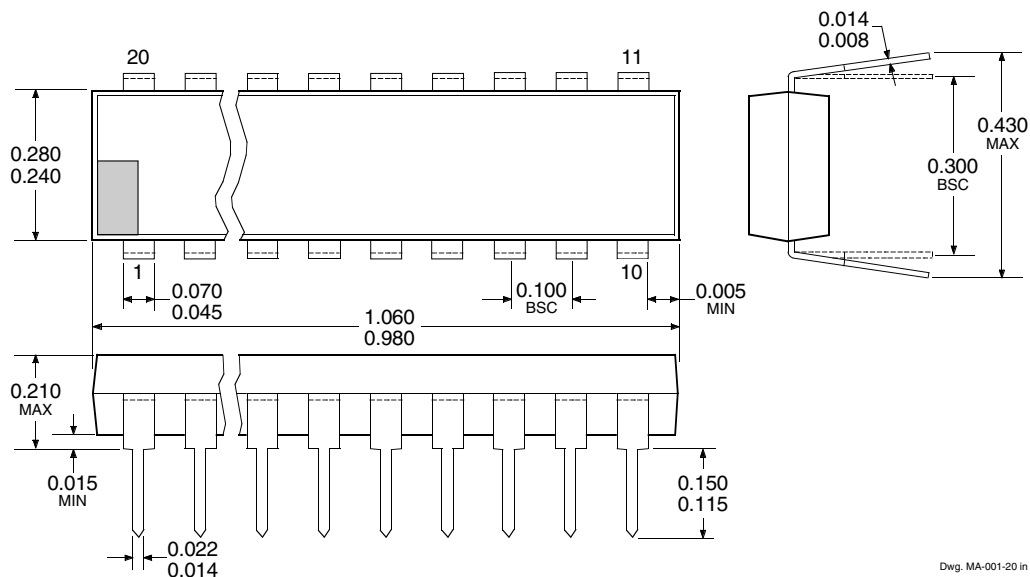
When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

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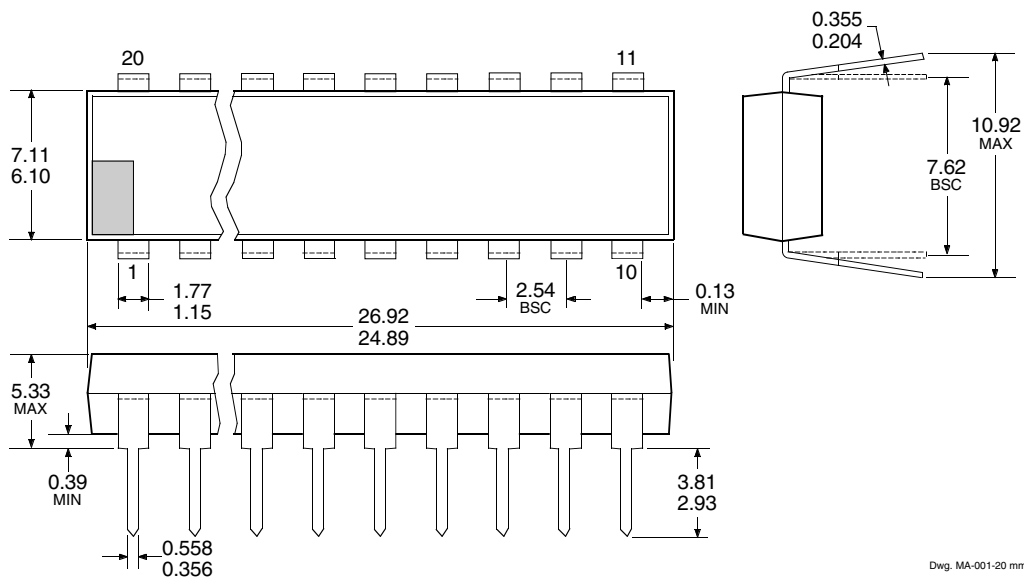
## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

### A6811EA & A6811SA

Dimensions in Inches  
(controlling dimensions)



Dimensions in Millimeters  
(for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Lead thickness is measured at seating plane or below.

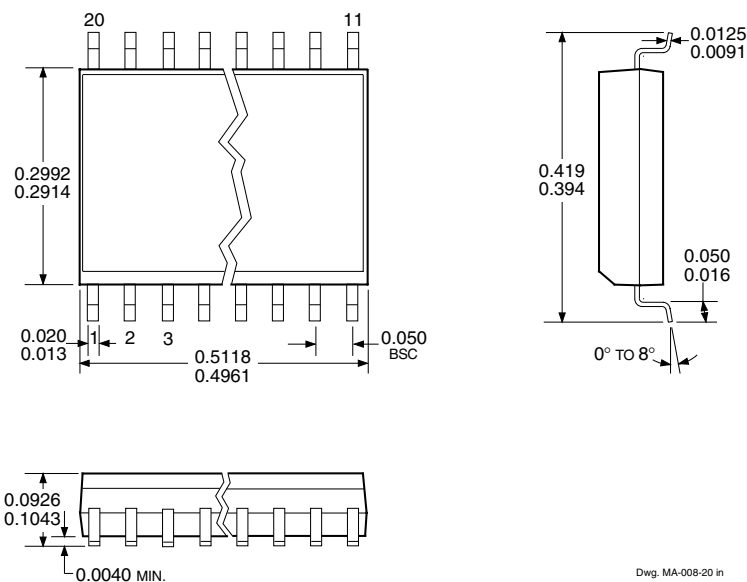


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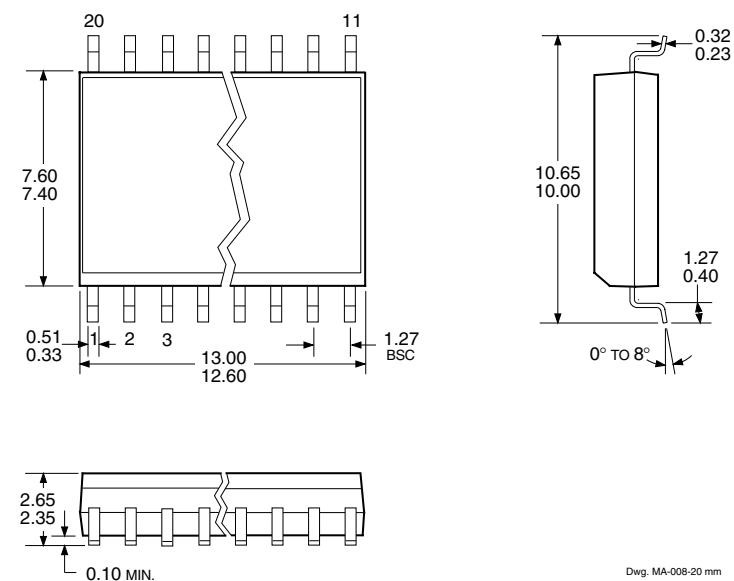
## 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

### A6811ELW & A6811SLW

Dimensions in Inches  
(for reference only)



Dimensions in Millimeters  
(controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.