DATA SHEET

TDA8920
2 × 80 W class-D power amplifier

Product specification
Supersedes data of 2002 Jun 06

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- High efficiency (~90%)
- Operating voltage from ±12.5 to ±30 V
- Very low quiescent current
- Low distortion
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Fixed gain of 30 dB in Single-Ended (SE) and 36 dB in Bridge-Tied Load (BTL)
- High output power
- Good ripple rejection
- Internal switching frequency can be overruled by an external clock
- No switch-on or switch-off plop noise
- Short-circuit proof across the load and to the supply lines
- Electrostatic discharge protection
- Thermally protected.

2 APPLICATIONS

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters).

3 GENERAL DESCRIPTION

The TDA8920 is a high efficiency class-D audio power amplifier with very low dissipation. The typical output power is 2 × 80 W. The device comes in a HSOP24 power package with a small internal heatsink. Depending on supply voltage and load conditions a very small or even no external heatsink is required. The amplifier operates over a wide supply voltage range from ±12.5 to ±30 V and consumes a very low quiescent current.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8920TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General; V_P = ±25 V						
V_P	operating supply voltage		±12.5	±25	±30	V
I_q	quiescent current	no load connected	–	55	75	mA
η	efficiency	P_o = 30 W; SE: R_L = 2 × 8 Ω; f_i = 1 kHz	–	90	–	%
Stereo single-ended configuration						
P_o	output power	R_L = 8 Ω; THD = 10%; V_P = ±25 V; note 1	36	39	–	W
		R_L = 4 Ω; THD = 10%; V_P = ±27 V; note 1	74	80	–	W
Mono bridge-tied load configuration						
P_o	output power	R_L = 4 Ω; THD = 10%; V_P = ±17 V; note 1	100	110	–	W
		R_L = 8 Ω; THD = 10%; V_P = ±25 V; note 1	128	140	–	W

Note

1. See also Section 16.5.

6 BLOCK DIAGRAM

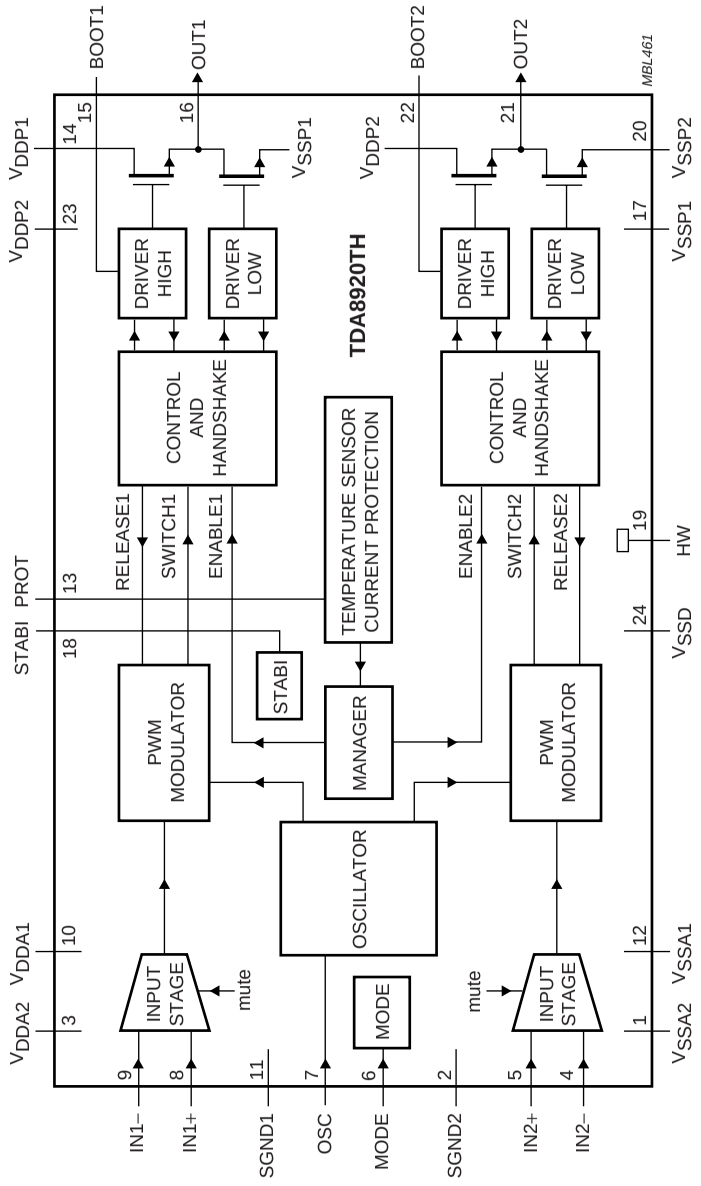
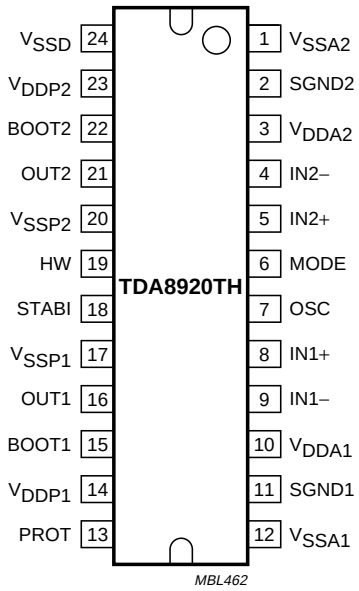


Fig.1 Block diagram.

(1) Pin 19 should be connected to pin 24 in the application.

7 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	1	negative analog supply voltage for channel 2
SGND2	2	signal ground channel 2
V_{DDA2}	3	positive analog supply voltage for channel 2
IN2–	4	negative audio input for channel 2
IN2+	5	positive audio input for channel 2
MODE	6	mode select input (standby/mute/operating)
OSC	7	oscillator frequency adjustment or tracking input
IN1+	8	positive audio input for channel 1
IN1–	9	negative audio input for channel 1
V_{DDA1}	10	positive analog supply voltage for channel 1
SGND1	11	signal ground for channel 1
V_{SSA1}	12	negative analog supply voltage for channel 1
PROT	13	time constant capacitor for protection delay
V_{DDP1}	14	positive power supply for channel 1
BOOT1	15	bootstrap capacitor for channel 1
OUT1	16	PWM output from channel 1
V_{SSP1}	17	negative power supply voltage for channel 1
STABI	18	decoupling internal stabilizer for logic supply
HW	19	handle wafer; must be connected to pin 24
V_{SSP2}	20	negative power supply voltage for channel 2
OUT2	21	PWM output from channel 2
BOOT2	22	bootstrap capacitor for channel 2
V_{DDP2}	23	positive power supply voltage for channel 2
V_{SSD}	24	negative digital supply voltage



(1) Pin 19 should be connected to pin 24 in the application.

Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The TDA8920 is a two channel audio power amplifier using class-D technology. A typical application diagram is illustrated in Fig.37. A detailed application reference design is given in Section 16.8. The audio input signal is converted into a digital Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side.

In this way a level shift is performed from the low power digital PWM signal (at logic levels) to a high power PWM signal which switches between the main supply lines.

A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeaker.

The TDA8920TH one-chip class-D amplifier contains high power D-MOS switches, drivers, timing and handshaking between the power switches and some control logic. For protection a temperature sensor and a maximum current detector are built-in.

The two audio channels of the TDA8920TH contain two PWMs, two analog feedback loops and two differential input stages. It also contains circuits common to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager.

The TDA8920TH contains two independent amplifier channels with high output power, high efficiency (90%), low distortion and a low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Stereo Single-Ended (SE) amplifiers.

The amplifier system can be switched in three operating modes with the MODE select pin:

- Standby mode; with a very low supply current
- Mute mode; the amplifiers are operational, but the audio signal at the output is suppressed
- Operating mode (amplifier fully operational) with output signal.

For suppressing plop noise the amplifier will remain, automatically, in the mute mode for approximately 150 ms before switching to operating mode; see Fig.4. In this time the coupling capacitors at the input are fully charged. An example of a switching circuit for driving the mode pin is illustrated in Fig.3.

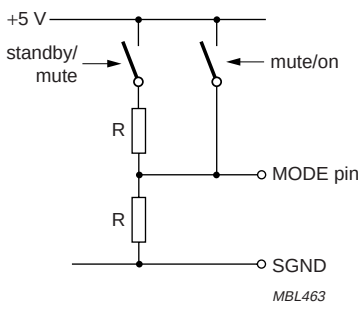
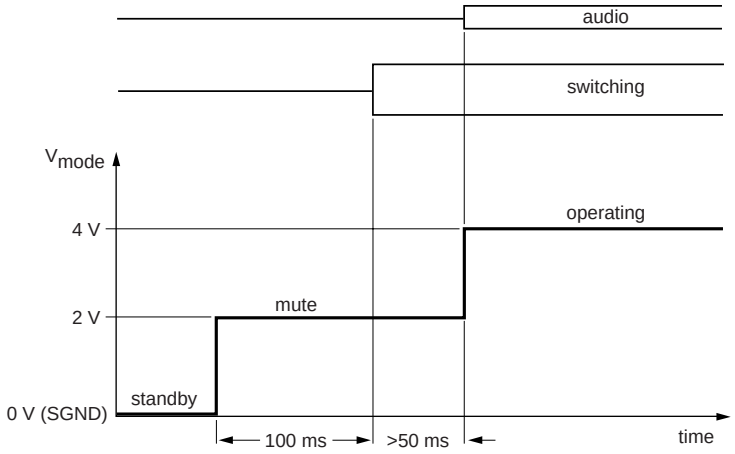


Fig.3 Example of mode select circuit.

When switching from standby to mute there is a delay of 100 ms before the output starts switching. The audio signal is available after the mode pin has been set to operating, but not earlier than 150 ms after switching to mute.



When switching from standby to operating there is a first delay of 100 ms before the outputs starts switching. The audio signal is available after a second delay of 50 ms.

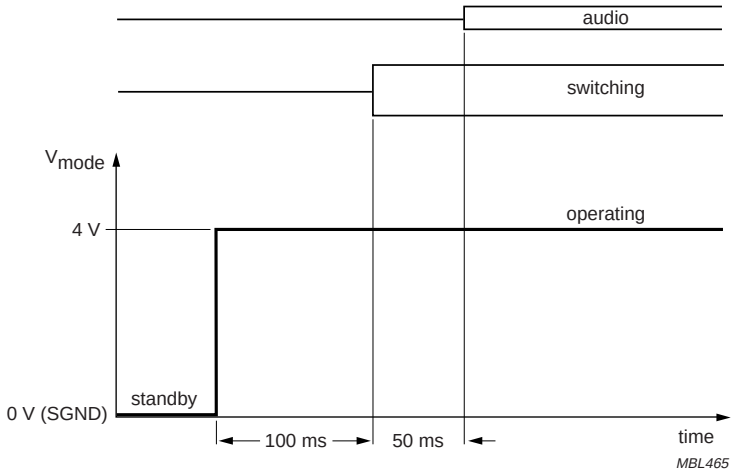


Fig.4 Timing on mode select input.

8.2 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 350 kHz. Using a 2nd-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC and V_{SSA}. With the resistor value given in the schematic diagram of the reference design, the carrier frequency is typical 350 kHz. The carrier frequency can be calculated using the following equation: $f_{OSC} = \frac{9 \times 10^9}{R_{OSC}} Hz$

If two or more class-D amplifiers are used in the same audio application, it is advisable to have all devices operating at the same switching frequency.

This can be realized by connecting all OSC pins together and feed them from a external central oscillator. Using an external oscillator it is necessary to force the OSC pin to a DC-level above SGND for switching from internal to external oscillator. In this case the internal oscillator is disabled and the PWM will be switched on the external frequency. The frequency range of the external oscillator must be in the range as specified in the switching characteristics; see Chapter 13.

Application in a practical circuit:

Internal oscillator: R_{osc} connected from pin OSC to V_{SS}

External oscillator: connect oscillator signal between pin OSC and SGND; delete R_{OSC} and C_{OSC}.

8.3 Protections

Temperature, supply voltage and short-circuit protections sensors are included on the chip. In the event that the maximum current or maximum temperature is exceeded the system will shut down.

8.3.1 Over-temperature

If the junction temperature (T_j) exceeds 150 °C, then the power stage will shut down immediately. The power stage will start switching again if the temperature drops to approximately 130 °C, thus there is a hysteresis of approximately 20 °C.

8.3.2 Short-circuit across the loudspeaker terminals and to supply lines

When the loudspeaker terminals are short-circuited or if one of the demodulated outputs of the amplifier is short-circuited to one of the supply lines this will be detected by the current protection. If the output current exceeds the maximum output current of 7.5 A, then the power stage will shut down within less than 1 µs and the high current will be switched off. In this state the dissipation is very low. Every 100 ms the system tries to restart again. If there is still a short-circuit across the loudspeaker load or to one of the supply lines, the system is switched off again as soon as the maximum current is exceeded. The average dissipation will be low because of this low duty cycle.

8.3.3 Start-up safety test

During the start-up sequence, when the mode pin is switched from standby to mute, the condition at the output terminals of the power stage are checked. In the event of a short-circuit at one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the systems waits for open-circuit outputs. Because the test is done before enabling the power stages, no large currents will flow in the event of a short-circuit. This system protects for short-circuits at both sides of the output filter to both supply lines. When there is a short-circuit from the power PWM output of the power stage to one of the supply lines (before the demodulation filter) it will also be detected by the 'start-up safety test'. Practical use of this test feature can be found in detection of short-circuits on the printed-circuit board.

Remark: this test is only operational prior to or during the start-up sequence, and not during normal operation.

During normal operation the maximum current protection is used to detect short-circuits across the load and with respect to the supply lines.

8.3.4 Supply voltage alarm

If the supply voltage falls below ±12.5 V the undervoltage protection is activated and system shuts down correctly. If the internal clock is used this switch-off will be silent and without plop noise. When the supply voltage rises above the threshold level the system is restarted again after 100 ms. If the supply voltage exceeds ±32 V the overvoltage protection is activated and the power stages shut down. They are re-enabled as soon as the supply voltage drops below the threshold level.

An additional balance protection circuit compares the positive (V_{DD}) and the negative (V_{SS}) supply voltages and is triggered if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. An expression for the unbalanced threshold level is as follows: $V_{unb,thr} \sim 0.15 \times (V_{DD} + V_{SS})$.

Example: with a symmetrical supply of ±30 V the protection circuit will be triggered if the unbalance exceeds approximately 9 V; see also Section 16.7.

8.4 Differential audio inputs

For a high common mode rejection ratio and a maximum of flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels can be inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier and with the same loudspeaker impedance an approximately four times higher output power can be obtained. The input configuration for mono BTL application is illustrated in Fig.5; for more information see Chapter 16.

In the stereo single-ended configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

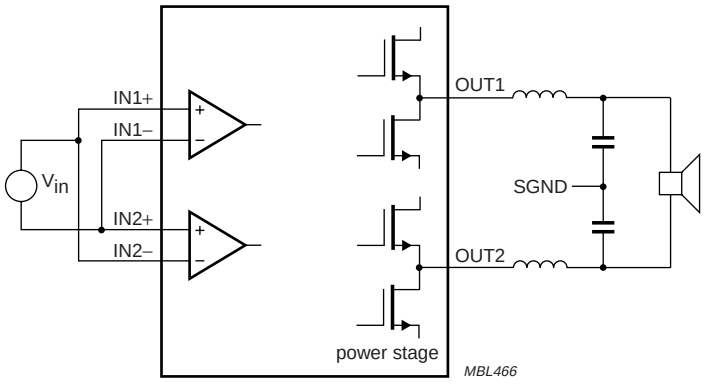


Fig.5 Input configuration for mono BTL application.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	±30	V
V_{ms}	mode select switch input voltage	with respect to SGND	–	5.5	V
V_{sc}	short-circuit voltage of output pins		–	±30	V
I_{ORM}	repetitive peak current in output pin	note 1	–	7.5	A
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
$V_{es(HBM)}$	electrostatic discharge voltage (HBM)	note 2			
		all pins with respect to V_{DD} (class 1a)	−1500	+1500	V
		all pins with respect to SGND (class 1a)	−1500	+1500	V
		all pins with respect to V_{SS} (class 1a)	−1500	+1500	V
		all pins (except pin 19) with respect to each other (class 1a)	−1500	+1500	V
		pin 19 (HW) with respect to all other pins	−500	+500	V
$V_{es(MM)}$	electrostatic discharge voltage (MM)	note 3			
		all pins with respect to V_{DD} (class B)	−250	+250	V
		all pins with respect to SGND (class B)	−250	+250	V
		all pins with respect to V_{SS} (class A1)	−150	+150	V
		all pins with respect to each other (class A1)	−100	+100	V

Notes

1. See also Section 16.6.
2. Human Body Model (HBM); R_S = 1500 Ω; C = 100 pF.
3. Machine Model (MM); R_S = 10 Ω; C = 200 pF; L = 0.75 mH.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	note 1	1.3	K/W

Note

1. See also Section 16.5.

11 QUALITY SPECIFICATION

In accordance with *"SNW-FQ611-part D"* if this type is used as an audio amplifier (except for ESD; see also Chapter 9).

12 STATIC CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	±12.5	±25	±30	V
I_q	quiescent current	no load connected	–	55	75	mA
I_{stb}	standby current		–	100	500	µA
Mode select input; pin MODE						
V_{ms}	input voltage	note 2	0	–	5.5	V
I_{ms}	input current	V_{ms} = 5.5 V	–	–	1000	µA
V_{stb}	input voltage in mode select for standby mode	notes 2 and 3	0	–	0.8	V
V_{mute}	input voltage in mode select for mute mode	notes 2 and 3	2.2	–	3.0	V
V_{on}	input voltage in mode select for on mode	notes 2 and 3	4.2	–	5.5	V
Audio inputs; pins IN2–, IN2+, IN1+ and IN1–						
V_I	DC input voltage	note 2	–	0	–	V
Amplifier outputs; pins OUT1 and OUT2						
$\lvert V_{OOSE} \rvert$	output offset voltage	SE; on and mute	–	–	150	mV
$\lvert \Delta V_{OOSE} \rvert$	variation of output offset voltage	SE; on ↔ mute	–	–	80	mV
$\lvert V_{OOBTL} \rvert$	output offset voltage	BTL; on and mute	–	–	215	mV
$\lvert \Delta V_{OOBTL} \rvert$	variation of output offset voltage	BTL; on ↔ mute	–	–	115	mV
Stabilizer; pin STABI						
$V_{o(stab)}$	stabilizer output voltage	mute and operating; note 4	11	13	15	V
Temperature protection						
T_{prot}	temperature protection activation		150	–	–	°C
T_{hys}	hysteresis on temperature protection		–	20	–	°C

Notes

1. The circuit is DC adjusted at V_P = ±12.5 to ±30 V.
2. With respect to SGND (0 V).
3. The transition regions between standby, mute and on contain hysteresis (see Fig.6).
4. With respect to V_{SS1}.

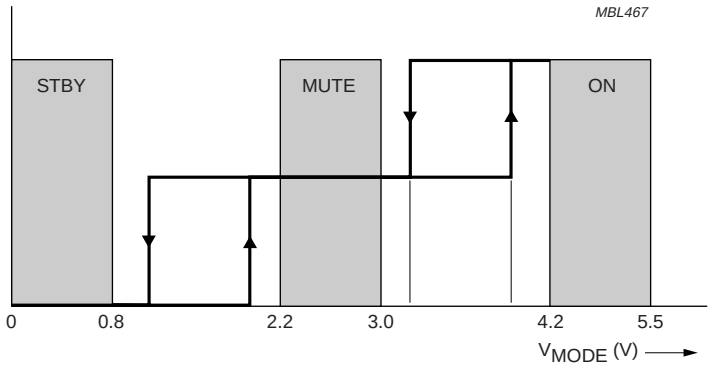


Fig.6 Mode select pin behaviour.

13 SWITCHING CHARACTERISTICS

V_{DD} = ±25 V; T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching frequency						
f_{osc}	typical internal oscillator frequency	R_{OSC} = 30.0 kΩ; see Section 16.11	290	317	344	kHz
$f_{osc(int)}$	internal oscillator frequency range	note 1	210	–	600	kHz
V_{OSC}	voltage at OSC pin	external oscillator or frequency tracking	SGND + 4.5	SGND + 5	SGND + 6	V
$V_{OSC(trip)}$	trip level at OSC pin for tracking	external oscillator or frequency tracking	–	SGND + 2.5	–	V
f_{track}	frequency range for tracking	external oscillator or frequency tracking	210	–	600	kHz
$V_{P(OSC)(ext)}$	minimum symmetrical supply voltage for external oscillator application	external oscillator	15	–	–	V

Note

1. Frequency set with R_{OSC}, according to formula in Chapter 8.

14 DYNAMIC AC CHARACTERISTICS (STEREO AND DUAL SE APPLICATION)

V_P = ±25 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_{sL} < 0.1 Ω (note 1); T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	R_L = 8 Ω; V_P = ±20 V; THD = 0.5%; note 2	18	20	–	W
		R_L = 8 Ω; V_P = ±20 V; THD = 10%; note 2	23	25	–	W
		R_L = 8 Ω; V_P = ±25 V; THD = 0.5%; note 2	28	30	–	W
		R_L = 8 Ω; V_P = ±25 V; THD = 10%; note 2	36	39	–	W
		R_L = 4 Ω; V_P = ±25 V; THD = 0.5%; note 2	51	55	–	W
		R_L = 4 Ω; V_P = ±25 V; THD = 10%; note 2	65	70	–	W
		R_L = 4 Ω; V_P = ±27 V; THD = 0.5%; note 2	60	65	–	W
		R_L = 4 Ω; V_P = ±27 V; THD = 10%; note 2	74	80	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.02	0.05	%
		f_i = 10 kHz	–	0.15	–	%
$G_{v(cl)}$	closed-loop voltage gain		29	30	31	dB
η	efficiency	P_o = 30 W; SE: R_L = 2 × 8 Ω; f_i = 1 kHz; note 4	85	90	–	%
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 5	–	55	–	dB
		on; f_i = 1 kHz; note 6	40	50	–	dB
		mute; f_i = 100 Hz; note 5	–	55	–	dB
		standby; f_i = 100 Hz; note 5	–	80	–	dB
$\lvert Z_i \rvert$	input impedance		45	68	–	kΩ
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; note 7	–	200	400	μV
		on; R_s = 10 kΩ; note 8	–	230	–	μV
		mute; note 9	–	220	–	μV
α_{cs}	channel separation	note 10	–	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB
$V_{o(mute)}$	output signal in mute	note 11	–	–	400	μV
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)	–	75	–	dB

Notes

1. R_{sL} = series resistance of inductor of low-pass LC filter in the application.
2. Output power is measured indirectly; based on R_{DSon} measurement.
3. Total harmonic distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a lower order low-pass filter a significantly higher value is found, due to the switching frequency outside the audio band. Maximum limit is guaranteed but may not be 100% tested.
4. Output power measured across the loudspeaker load.
5. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_s = 0 Ω.
6. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_s = 0 Ω.
7. B = 22 Hz to 22 kHz; R_s = 0 Ω; maximum limit is guaranteed but may not be 100% tested.
8. B = 22 Hz to 22 kHz; R_s = 10 kΩ.
9. B = 22 Hz to 22 kHz; independent of R_s.

10. P_o = 1 W; R_s = 0 Ω; f_t = 1 kHz.
11. $V_i = V_{i(max)}$ = 1 V (RMS); maximum limit is guaranteed but may not be 100% tested.

15 DYNAMIC AC CHARACTERISTICS (MONO BTL APPLICATION)

V_P = ±25 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_{sL} < 0.1 Ω (note 1); T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	R_L = 8 Ω; V_P = ±25 V; THD = 0.5%; note 2	100	110	–	W
		R_L = 8 Ω; V_P = ±25 V; THD = 10%; note 2	128	140	–	W
		R_L = 8 Ω; V_P = ±21 V; THD = 0.5%; note 2	73	79	–	W
		R_L = 8 Ω; V_P = ±21 V; THD = 10%; note 2	92	100	–	W
		R_L = 4 Ω; V_P = ±17 V; THD = 0.5%; note 2	66	75	–	W
		R_L = 4 Ω; V_P = ±17 V; THD = 10%; note 2	100	110	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.015	0.05	%
		f_i = 10 kHz	–	0.02	–	%
$G_{v(cl)}$	closed-loop voltage gain		35	36	37	dB
η	efficiency	P_o = 140 W; f_i = 1 kHz; note 4	85	89	–	%
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 5	–	49	–	dB
		on; f_i = 1 kHz; note 6	36	44	–	dB
		mute; f_i = 100 Hz; note 5	–	49	–	dB
		standby; f_i = 100 Hz; note 5	–	80	–	dB
$\lvert Z_i \rvert$	input impedance		22	34	–	kΩ
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; note 7	–	280	560	μV
		on; R_s = 10 kΩ; note 8	–	300	–	μV
		mute; note 9	–	280	–	μV
$V_{o(mute)}$	output signal in mute	note 10	–	–	500	μV
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)	–	75	–	dB

Notes

1. R_{sL} = series resistance of inductor of low-pass LC filter in the application.
2. Output power is measured indirectly; based on R_{DSon} measurement.
3. Total harmonic distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low order low-pass filter a significant higher value will be found, due to the switching frequency outside the audio band. Maximum limit is guaranteed but may not be 100% tested.
4. Output power measured across the loudspeaker load.
5. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_s = 0 Ω.
6. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_s = 0 Ω.
7. B = 22 Hz to 22 kHz; R_s = 0 Ω; maximum limit is guaranteed but may not be 100% tested.
8. B = 22 Hz to 22 kHz; R_s = 10 kΩ.
9. B = 22 Hz to 22 kHz; independent of R_s.
10. $V_i = V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz; maximum limit is guaranteed but may not be 100% tested.

16 APPLICATION INFORMATION

16.1 BTL application

When using the system in the mono BTL application (for more output power), the inputs of both channels must be connected in parallel; the phase of one of the inputs must be inverted; see Fig.5. In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

16.2 MODE pin

For correct operation the switching voltage at the mode pin should be debounced. If the mode pin is driven by a mechanical switch an appropriate debouncing low-pass filter should be used. If the mode pin is driven by an electronic circuit or microcontroller then it should remain at the mute voltage level for at least 100 ms before switching back to the standby voltage level.

16.3 Output power estimation

The output power in several applications (SE and BTL) can be estimated using the following expressions:

$$\text{SE: } P_{out\_1\%} = \frac{\left[\frac{R_L}{R_L + 0.6} \times V_P \times (1 - t_{min} \times f_{osc})\right]^2}{2 \times R_L}$$

$$\text{Maximum current: } I_{out^\wedge} = \frac{V_P \times (1 - t_{min} \times f_{osc})}{R_L + 0.6}$$

should not exceed 7.5 A.

$$\text{BTL: } P_{out\_1\%} = \frac{\left[\frac{R_L}{R_L + 1.2} \times 2V_P \times (1 - t_{min} \times f_{osc})\right]^2}{2 \times R_L}$$

$$\text{Maximum current: } I_{out^\wedge} = \frac{2V_P \times (1 - t_{min} \times f_{osc})}{R_L + 1.2}$$

should not exceed 7.5 A.

Legend:

R_L = load impedance

f_{osc} = oscillator frequency

t_{min} = minimum pulse width (typical 190 ns)

V_P = single-sided supply voltage (so if supply ±30 V symmetrical → V_P = 30 V)

$P_{out\_1\%}$ = output power just at clipping

$P_{out\_10\%}$ = output power at THD = 10%

$P_{out\_10\%} = 1.25 \times P_{out\_1\%}$.

16.4 External clock

The minimum required symmetrical supply voltage for external clock application is ±15 V (equally the minimum asymmetrical supply for applications with an external clock is 30 V).

When using an external clock the following accuracy of the duty cycle of the external clock has to be taken into account; 47.5% < DC, external clock < 52.5%.

A possible solution for an external clock oscillator circuit is illustrated in Fig.7.

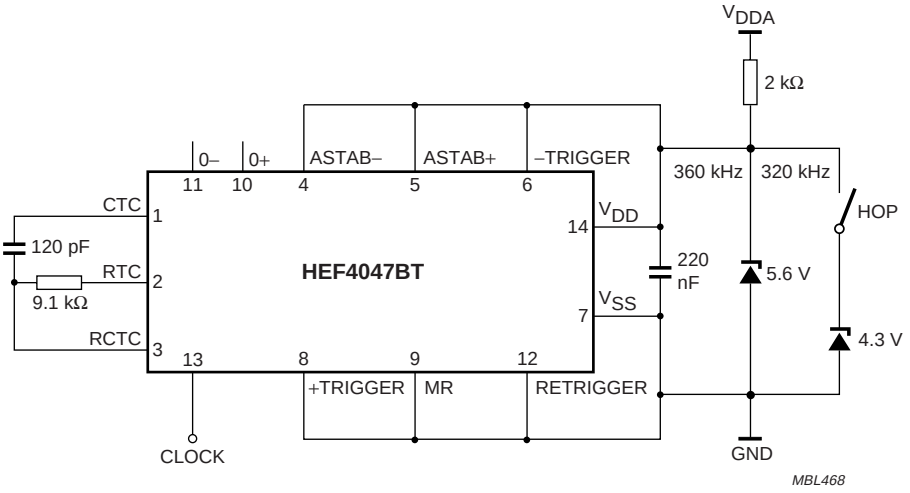


Fig.7 External oscillator circuit.

16.5 Heatsink requirements

In some applications it may be necessary to connect an external heatsink to the TDA8920TH. The determining factor is the 150 °C maximum junction temperature [$T_{j(max)}$] which cannot be exceeded. The expression below shows the relationship between the maximum allowable power dissipation and the total thermal resistance from junction to ambient:

$$R_{th(j-a)} = \frac{T_{j(max)} - T_A}{P_{diss}}$$

P_{diss} is determined by the efficiency (η) of the 1-chip class-D amplifier. The efficiency measured in the TDA8920TH as a function of output power is given in Fig.18. The power dissipation can be derived as function of output power; see Fig.17.

The derating curves (given for several values of the $R_{th(j-a)}$) are illustrated in Fig.8. A maximum junction temperature T_j = 150 °C is taken into account. From Fig.8 the maximum allowable power dissipation for a given heatsink size can be derived or the required heatsink size can be determined at a required dissipation level.

Example 1:

P_{out} = 2 × 30 W into 8 Ω

$T_{j(max)}$ = 150 °C

T_{amb} = 60 °C

$P_{diss(tot)}$ = 6 W (from Fig.17)

The required $R_{th(j-a)}$ = 15 K/W can be calculated

The $R_{th(j-a)}$ of TDA8920 in free air is 35 K/W; the $R_{th(j-c)}$ of TDA8920 is 1.3 K/W, thus a heatsink of 13.7 K/W is required for this example.

In actual applications, other factors such as the average power dissipation with music source (as opposed to a continuous sine wave) will determine the size of the heatsink required.

Example 2:

P_{out} = 2 × 75 W into 4 Ω

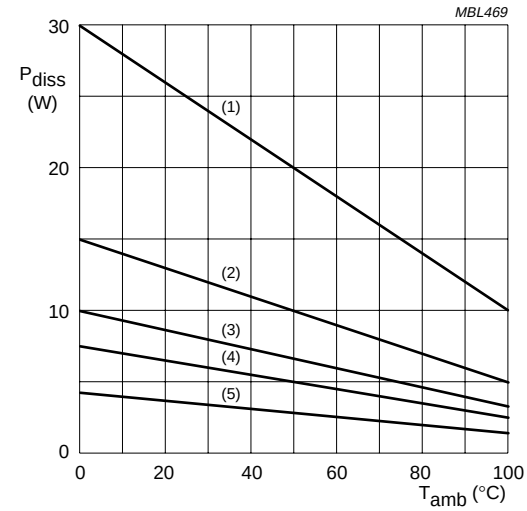
$T_{j(max)}$ = 150 °C

T_{amb} = 60 °C

$P_{diss(tot)}$ = 17.5 W (from Fig.17)

The required $R_{th(j-a)}$ = 5.14 K/W

The $R_{th(j-a)}$ of TDA8920TH in free air is 35 K/W; the $R_{th(j-c)}$ of TDA8920TH is 1.3 K/W, so a heatsink of 3.84 K/W is required for this example.



(1) $R_{th(j-a)}$ = 5 K/W. (4) $R_{th(j-a)}$ = 20 K/W.
(2) $R_{th(j-a)}$ = 10 K/W. (5) $R_{th(j-a)}$ = 35 K/W.
(3) $R_{th(j-a)}$ = 15 K/W.

Fig.8 Derating curves for power dissipation as a function of maximum ambient temperature.

16.6 Output current limiting

To guarantee the robustness of the class-D amplifier the maximum output current which can be delivered by the output stage is limited. An overcurrent protection is included for each output power switch. When the current flowing through any of the power switches exceeds a defined internal threshold (e.g. in case of a short-circuit to the supply lines or a short-circuit across the load), the amplifier will shut down immediately and an internal timer will be started. After a fixed time (e.g. 100 ms) the amplifier is switched on again. If the requested output current is still too high the amplifier will switch-off again. Thus the amplifier will try to switch to the operating mode every 100 ms. The average dissipation will be low in this situation because of this low duty cycle. If the overcurrent condition is removed the amplifier will remain operating.

Because the duty cycle is low the amplifier will be switched off for a relatively long period of time which will be noticed as a so-called audio-hole; an audible interruption in the output signal.

To trigger the maximum current protection in the TDA8920, the required output current must exceed 7.5 A. This situation occurs in case of:

- Short-circuits from any output terminal to the supply lines (V_{DD} or V_{SS})
- Short-circuit across the load or speaker impedances or a load impedance below the specified values of 4 and 8 Ω.

Even if load impedances are connected to the amplifier outputs which have an impedance rating of 4 Ω, this impedance can be lower due to the frequency characteristic of the loudspeaker; practical loudspeaker impedances can be modelled as an RLC network which will have a specific frequency characteristic: the impedance at the output of the amplifier will vary with the input frequency. A high supply voltage in combination with a low impedance will result in large current requirements.

Another factor which must be taken into account is the ripple current which will also flow through the output power switches. This ripple current depends on the inductor values which are used, supply voltage, oscillator frequency, duty factor and minimum pulse width. The maximum available output current to drive the load impedance can be calculated by subtracting the ripple current from the maximum repetitive peak current in the output pin, which is 7.5 A for the TDA8920TH.

As a rule of thumb the following expressions can be used to determine the minimum allowed load impedance without generating audio holes:

$$Z_L \geq \frac{V_P(1 - t_{min} f_{osc})}{I_{ORM} - I_{ripple}} - 0.6 \quad \text{SE application.}$$

$$Z_L \geq \frac{2V_P(1 - t_{min} f_{osc})}{I_{ORM} - I_{ripple}} - 1.2 \quad \text{BTL application.}$$

Legend:

Z_L = load impedance

f_{osc} = oscillator frequency

t_{min} = minimum pulse width (typical 190 ns)

V_P = single-sided supply voltage
(so if the supply = ±30 V symmetrical → V_P = 30 V)

I_{ORM} = maximum repetitive peak current in output pin; see also Chapter 9

I_{ripple} = ripple current.

16.7 Pumping effects

The TDA8920 class-D amplifier is supplied by a symmetrical voltage (e.g V_{DD} = +25 V, V_{SS} = −25 V). When the amplifier is used in a Single-Ended (SE) configuration a so-called ‘pumping effect’ can occur. During one switching interval energy is taken from one supply (e.g. V_{DD}), while a part of that energy is delivered back to the other supply line (e.g. V_{SS}) and visa versa. When the voltage supply source cannot sink energy the voltage across the output capacitors of that voltage supply source will increase: the supply voltage is pumped to higher levels.

The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Capacitor value present on supply lines
- Source/sink currents of other channels.

The pumping effect should not cause a malfunction of either the audio amplifier and/or the voltage supply source. For instance, this malfunction can be caused by triggering of the undervoltage or overvoltage protection or unbalance protection of the amplifier.

16.8 Reference design

The reference design for the single-chip class-D audio amplifier for TDA8920TH is illustrated in Fig.9. The Printed-Circuit Board (PCB) layout is shown in Fig.10. The Bill Of Materials (BOM) is given in Table 1.

16.9 PCB information for HSOP24 encapsulation

The size of the printed-circuit board is 74.3 × 59.10 mm, dual sided 35 μm copper with 121 metallized through holes.

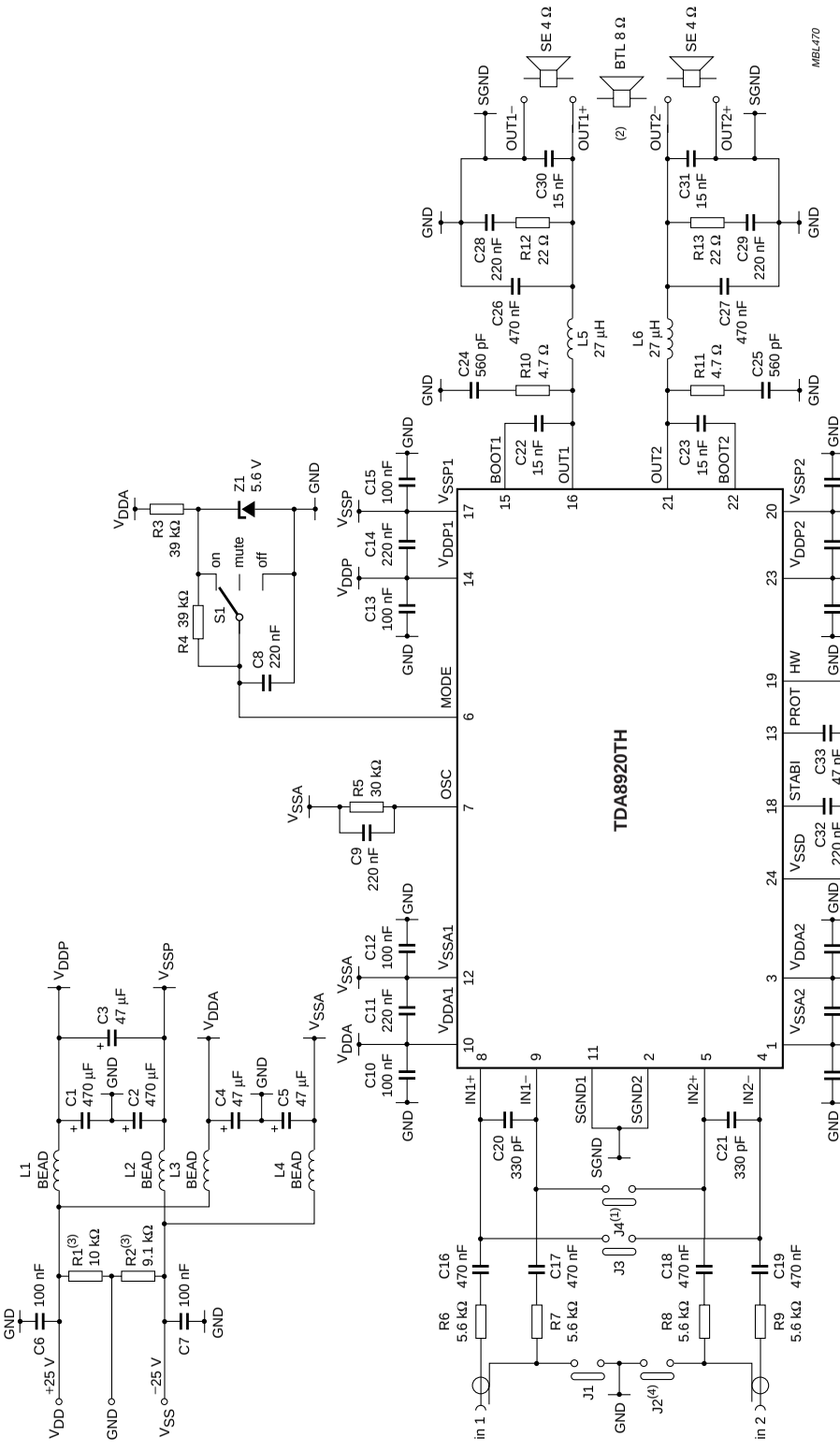
The standard configuration is a symmetrical supply (typical ±25 V) with stereo SE outputs (typical 2 × 4 Ω).

The PCB is also suitable for mono BTL configuration (1 × 8 Ω) also for symmetrical supply and for asymmetrical supply.

It is possible to use several different output filter inductors such as 16RHBP or EP13 types to evaluate the performance against the price or size.

16.10 Classification

The application shows optimized signal and EMI performance.



(1) BTL: remove in2, R8, R9, C18, C19, C21 and close J3 and J4.

(2) BTL: connect loudspeaker between OUT1+ and OUT2−.

(3) BTL: R1 and R2 are only required when an asymmetrical supply is used (V_{SS} = 0 V).

(4) In case of HUM close J1 and J2.

(5) Every decoupling to ground (plane) must be made as close as possible to the pin.

(6) To handle 20 Hz under all conditions in stereo SE mode, the external power supply needs to have a capacitance of at least 4700 µF per supply line; V_P = ±27 V (max).

Fig.9 Single-chip class-D audio amplifier application diagram.

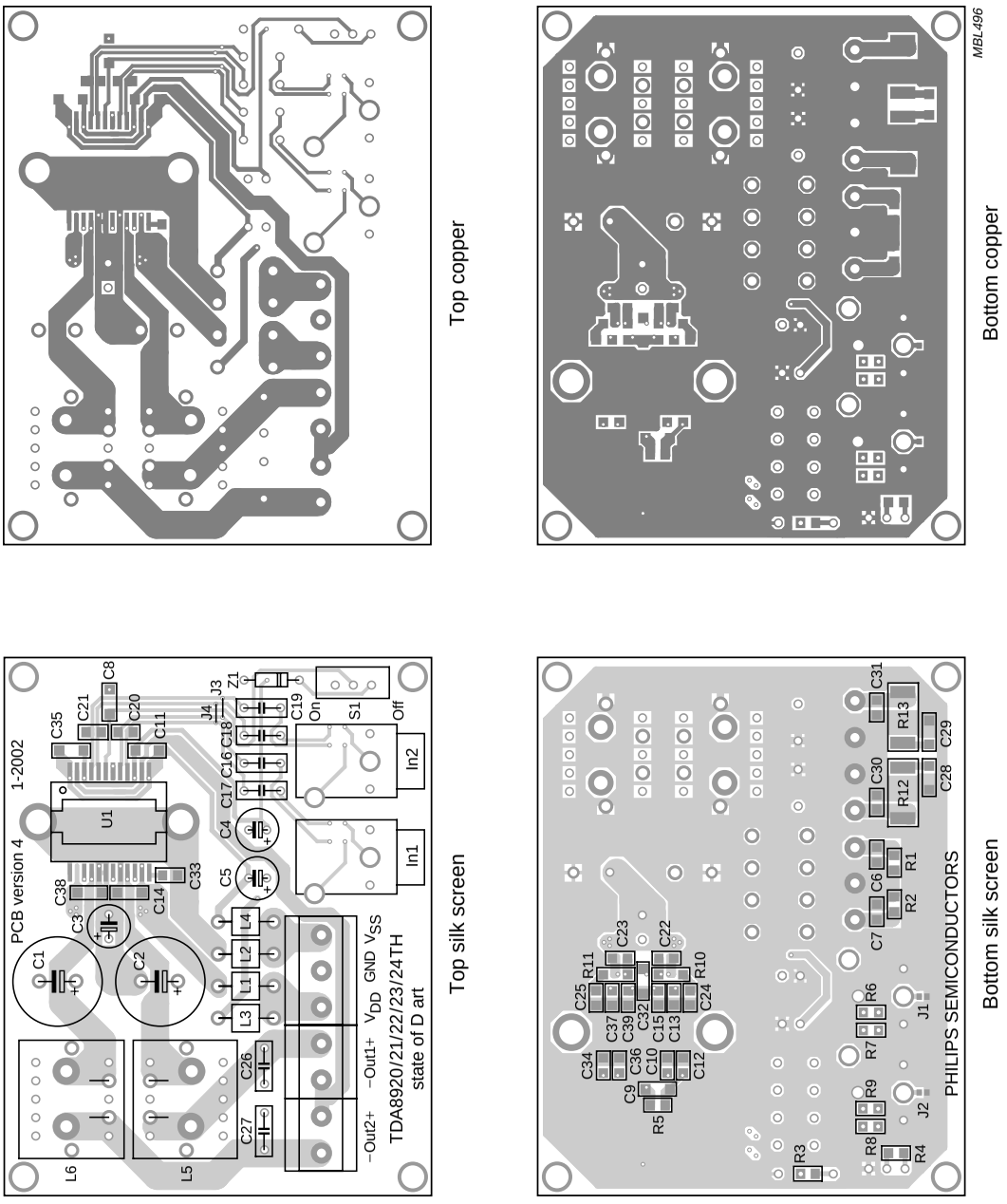


Fig.10 Printed-circuit board layout for the TDA8920TH.

16.11 Reference design: bill of materials

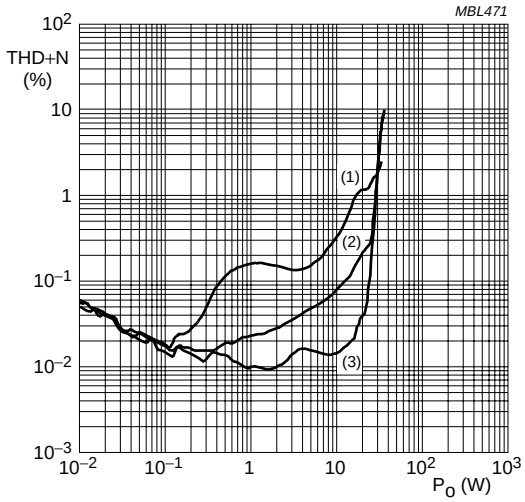
Table 1 Single-chip class-D audio amplifier printed-circuit board (version 4; 01-2002) for TDA8920TH (see Figs 9 and 10)

BOM ITEM	QUANTITY	REFERENCE	PART	DESCRIPTION
1	1	U1	TDA8920TH	Philips Semiconductors B.V.
2	2	in1 and in2	cinch inputs	Farnell 152-396
3	2	out1 and out2	output connector	Augat 5KEV-02
4	1	V_{DD}, GND and V_{SS}	supply connector	Augat 5KEV-03
5	2	L6 and L5	27 μH	EP13 or 16RHBP
6	4	L1, L2, L3 and L4	BEAD	Murata BL01RN1-A62
7	1	S1	PCB switch	Knitter ATE1E M-O-M
8	1	Z1	5V6	BZX 79C5V6 DO-35
9	2	C1 and C2	470 μF/35 V	Panasonic M series ECA1VM471
10	3	C3, C4 and C5	47 μF 63 V	Panasonic NHG series ECA1JHG470
11	6	C16, C17, C18, C19, C26 and C27	470 nF 63 V	MKT EPCOS B32529- 0474- K
12	9	C8, C9, C11, C14, C28, C29, C32, C35 and C38	220 nF 63 V	SMD 1206
13	10	C6, C7, C10, C12, C13, C15, C34, C36, C37 and C39	100 nF 50 V	SMD 0805
14	2	C20 and C21	330 pF 50 V	SMD 0805
15	4	C22, C23, C30 and C31	15 nF 50 V	SMD 0805
16	2	C24, C25	560 pF 100 V	SMD 0805
17	1	C33	47 pF 25V	SMD 0805
18	2	R4 and R3	39 kΩ 0.1 W	SMD 0805
19	1	R5	30 kΩ 0.1 W	SMD 1206
20	1	R1	10 kΩ 0.1 W; optional	SMD 0805
21	1	R2	9.1 kΩ 0.1 W; optional	SMD 0805
22	4	R6, R7, R8 and R9	5.6 kΩ 0.1 W	SMD 0805
23	2	R13 and R12	22 Ω 1 W	SMD 2512
24	2	R10 and R11	4.7 Ω 0.25 W	SMD 1206
25	2	J1 and J2	solder dot jumpers for ground reference in case of HUM (60 Hz noise)	
26	2	J3 and J4	wire jumpers for BTL application	
27	1	heatsink	30 mm SK400; OK for maximum music dissipation; 1/8 Prated (2 × 75 W/8) in 2 × 4 Ω at T_{amb} = 70 °C	
28	1	printed-circuit board material	1.6 mm thick epoxy FR4 material, double sided 35 μm copper; clearances 300 μm; minimum copper track 400 μm	

16.12 Curves measured in the reference design

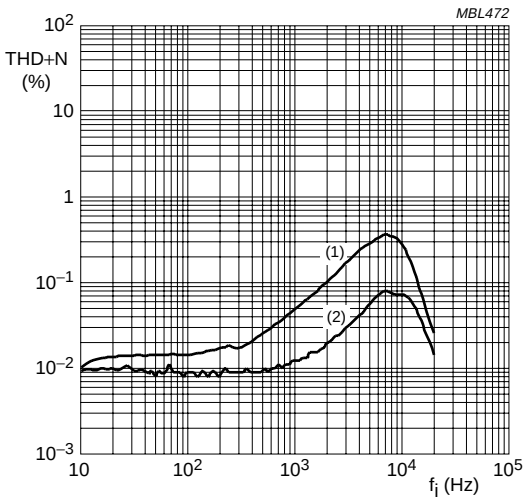
The curves illustrated in Figs 19 and 20 are measured with a restive load impedance. Spread in RI (e.g. due to the frequency characteristics of the loudspeaker) can trigger the maximum current protection circuit; see Section 16.6.

The curves illustrated in Figs 29 and 30 show the effects of supply pumping when only one single-ended channel is driven with a low frequency signal; see Section 16.7.



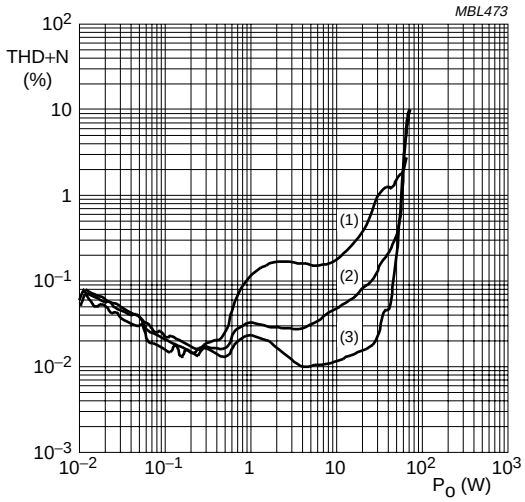
2 × 8 Ω SE; V_P = ±25 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.11 THD + N as a function of output power.



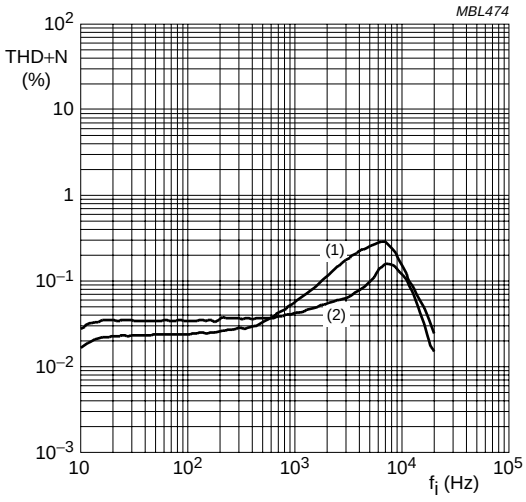
2 × 8 Ω SE; V_P = ±25 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.12 THD + N as a function of input frequency.



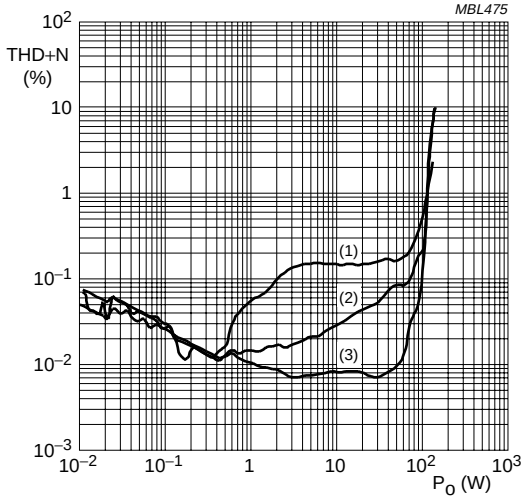
2 × 4 Ω SE; V_P = ±25 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.13 THD + N as a function of output power.



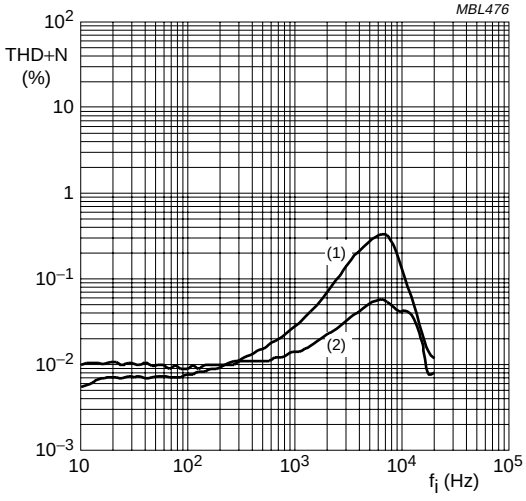
2 × 4 Ω SE; V_P = ±25 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.14 THD + N as a function of input frequency.



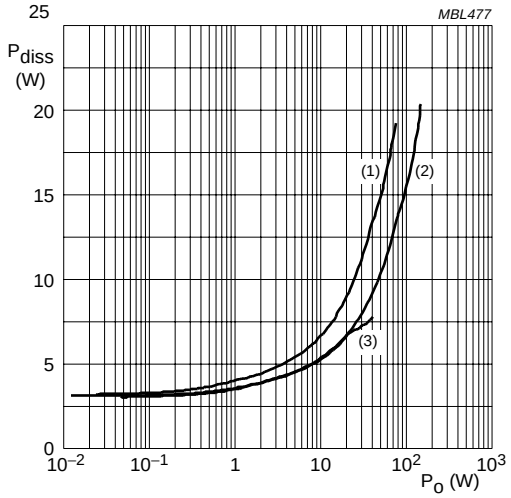
1 × 8 Ω BTL; V_P = ±25 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.15 THD + N as a function of output power.



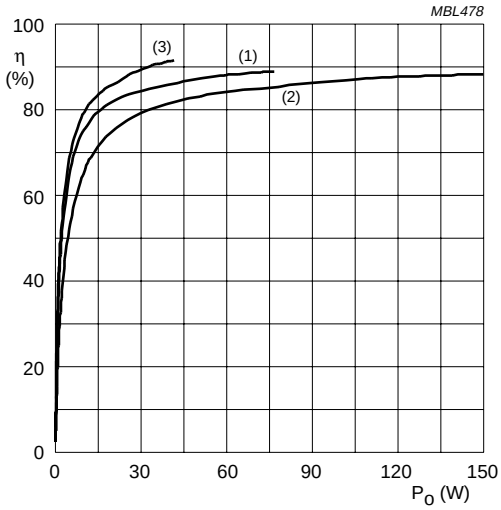
1 × 8 Ω BTL; V_P = ±25 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.16 THD + N as a function of input frequency.



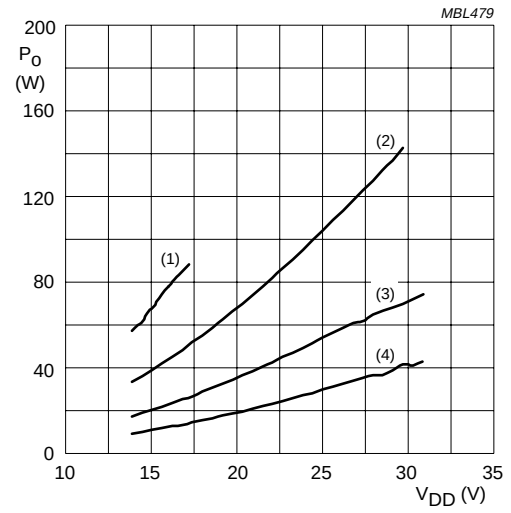
V_P = ±25 V; f_i = 1 kHz.
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.17 Power dissipation as a function of output power.



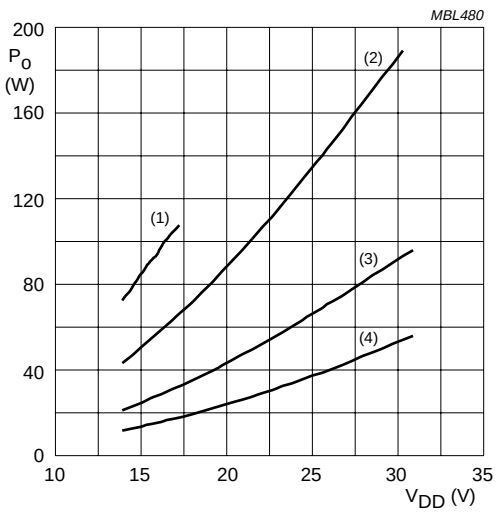
V_P = ±25 V; f_i = 1 kHz.
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.18 Efficiency as a function of output power.



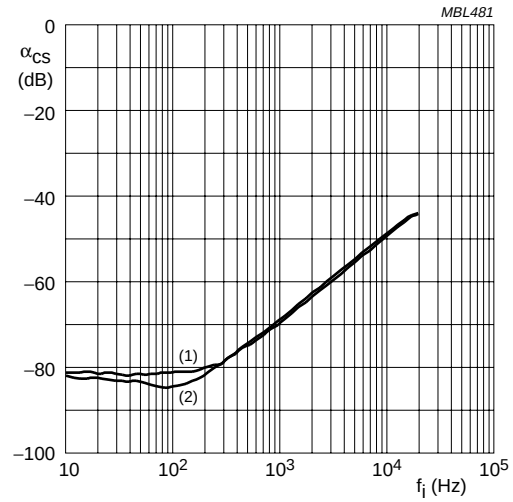
THD + N = 0.5%; f = 1 kHz.
(1) 1 × 4 Ω BTL.
(2) 1 × 8 Ω BTL.
(3) 2 × 4 Ω SE.
(4) 2 × 8 Ω SE.

Fig.19 Output power as a function of supply voltage.



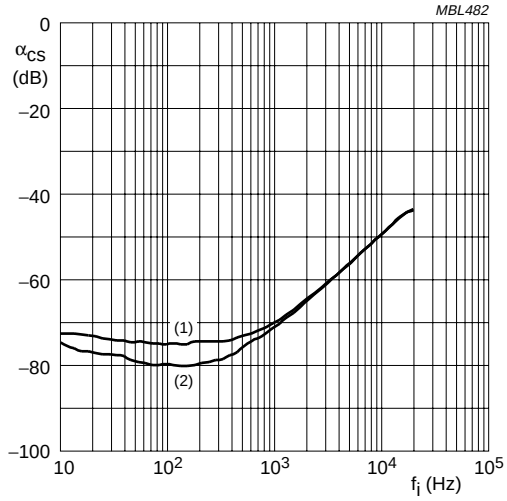
THD + N = 10%; f = 1 kHz.
(1) 1 × 4 Ω BTL.
(2) 1 × 8 Ω BTL.
(3) 2 × 4 Ω SE.
(4) 2 × 8 Ω SE.

Fig.20 Output power as a function of supply voltage.



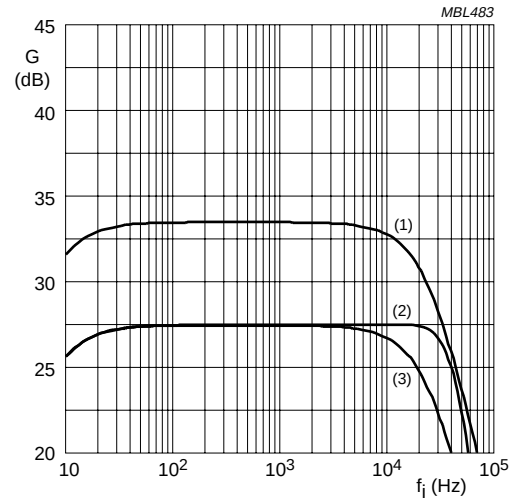
$2 \times 8\ \Omega$ SE; $V_P = \pm 25$ V.
(1) $P_{out} = 1$ W.
(2) $P_{out} = 10$ W.

Fig.21 Channel separation as a function of input frequency.



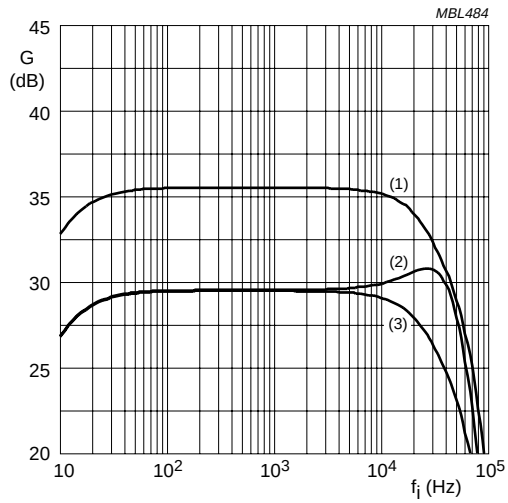
$2 \times 4\ \Omega$ SE; $V_P = \pm 25$ V.
(1) $P_{out} = 1$ W.
(2) $P_{out} = 10$ W.

Fig.22 Channel separation as a function of input frequency.



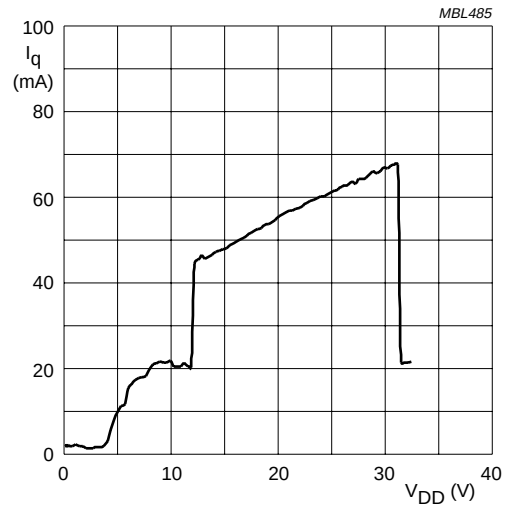
$V_P = \pm 25$ V; $V_i = 100$ mV; $R_s = 10\ k\Omega$; $C_i = 330$ pF.
(1) $1 \times 8\ \Omega$ BTL.
(2) $2 \times 8\ \Omega$ SE.
(3) $2 \times 4\ \Omega$ SE.

Fig.23 Gain as a function of input frequency.



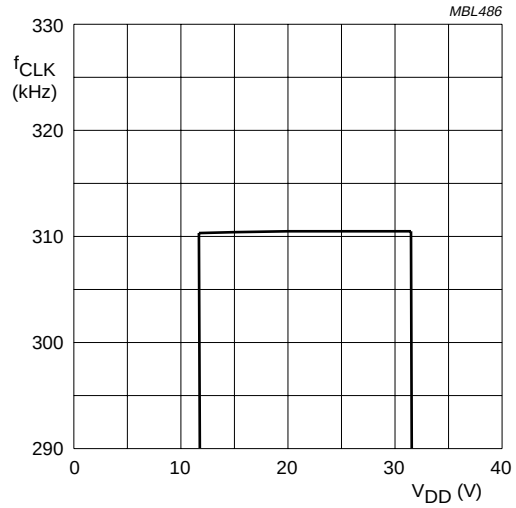
$V_P = \pm 25$ V; $V_i = 100$ mV; $R_s = 0\ k\Omega$.
(1) $1 \times 8\ \Omega$ BTL.
(2) $2 \times 8\ \Omega$ SE.
(3) $2 \times 4\ \Omega$ SE.

Fig.24 Gain as a function of input frequency.



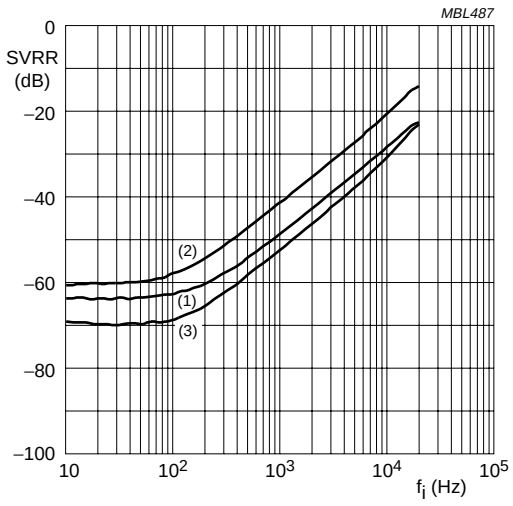
R_L is open-circuit.

Fig.25 Quiescent current as a function of supply voltage.



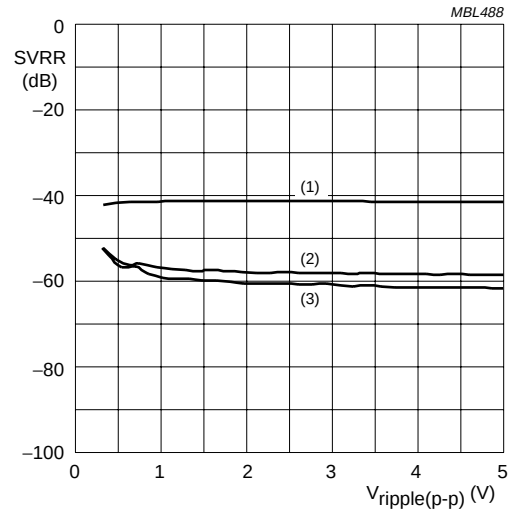
R_L is open-circuit.

Fig.26 Clock frequency as a function of supply voltage.



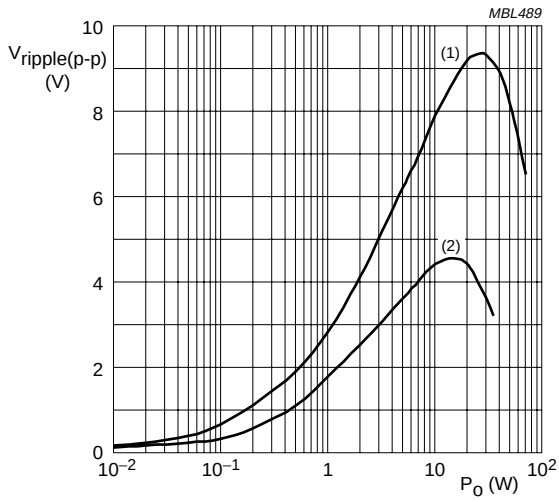
V_P = ±25 V; V_{ripple} = 2 V (p-p) with respect to ground.
(1) Both supply lines in anti-phase.
(2) Both supply lines in phase.
(3) One supply line rippled.

Fig.27 SVRR as a function of input frequency.



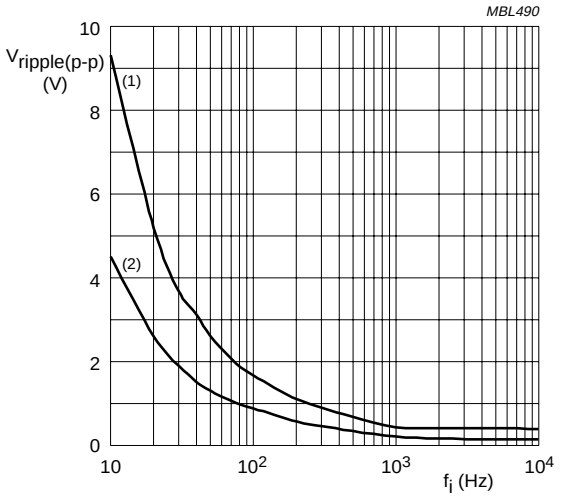
V_P = ±25 V; $V_{ripple\ (P-P)}$ with respect to ground.
(1) f_{ripple} = 1 kHz.
(2) f_{ripple} = 100 Hz.
(3) f_{ripple} = 10 Hz.

Fig.28 SVRR as a function of $V_{ripple(p-p)}$.



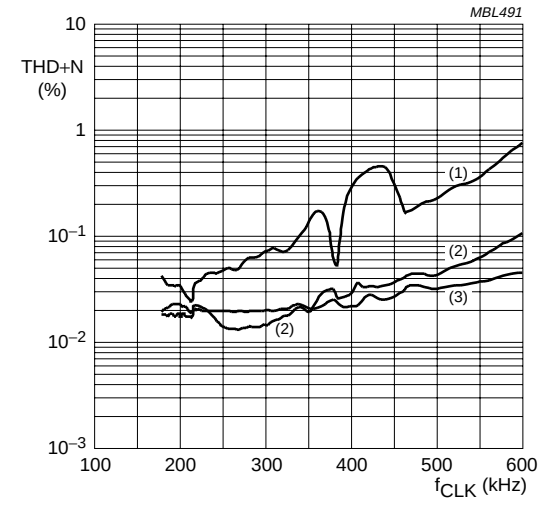
V_P = ±25 V; 3000 μF per supply line; f = 10 Hz.
(1) 1 × 4 Ω SE.
(2) 1 × 8 Ω SE.

Fig.29 Supply voltage ripple as a function of output power.



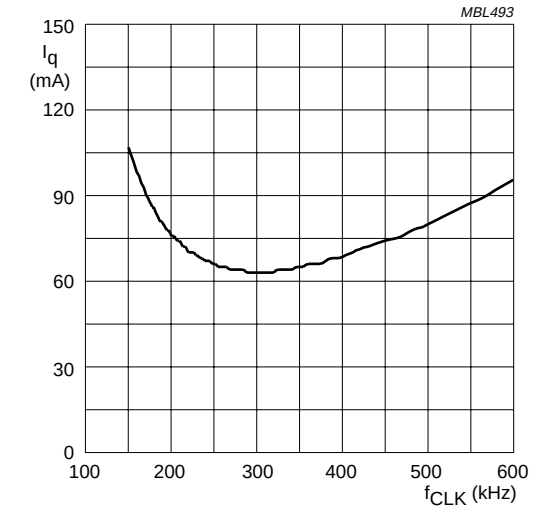
V_P = ±25 V; 3000 μF per supply line.
(1) P_{out} = 30 W into 1 × 4 Ω SE.
(2) P_{out} = 15 W into 1 × 8 Ω SE.

Fig.30 Supply voltage ripple as a function of input frequency.



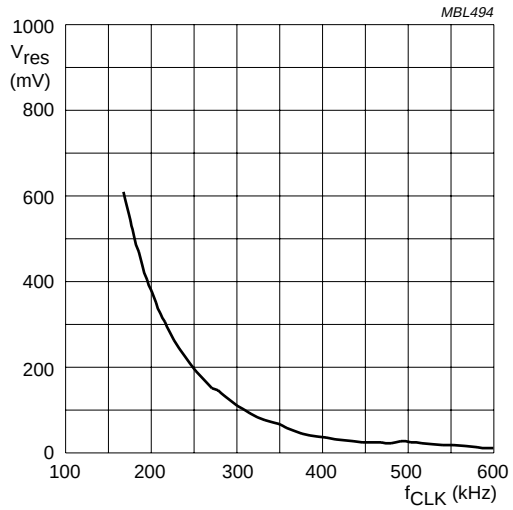
V_P = ±25 V; P_o = 1 W into 8 Ω.
(1) 10 Hz.
(2) 1 kHz.
(3) 100 Hz.

Fig.31 THD + N as a function of clock frequency.



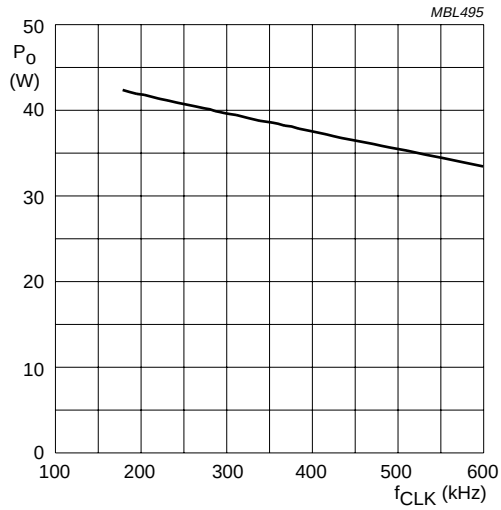
V_P = ±25 V; R_L is open-circuit.

Fig.32 Quiescent current as a function of clock frequency.



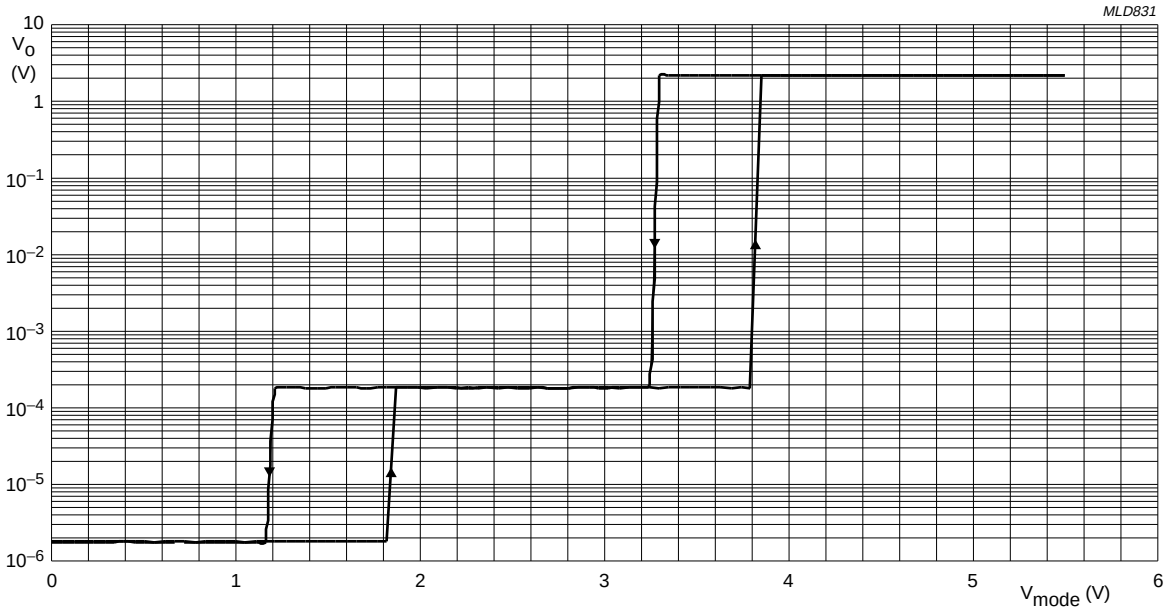
V_P = ±25 V; R_L = 8 Ω.

Fig.33 PWM residual voltage as a function of clock frequency.



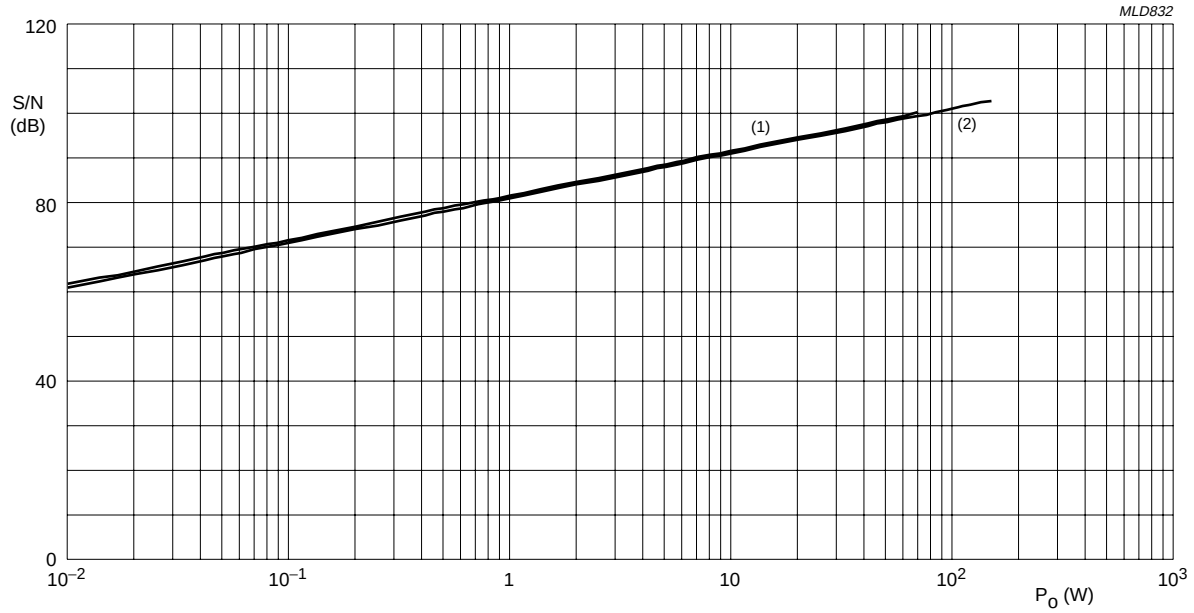
V_P = ±25 V; R_L = 8 Ω; f = 1 kHz; THD + N = 10%.

Fig.34 Output power as a function of clock frequency.



V_i = 100 mV; f = 1 kHz.

Fig.35 Output voltage as a function of mode voltage.



V_P = ±25 V; R_s = 10 kΩ.
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.

Fig.36 Signal-to-noise ratio as a function of output power.

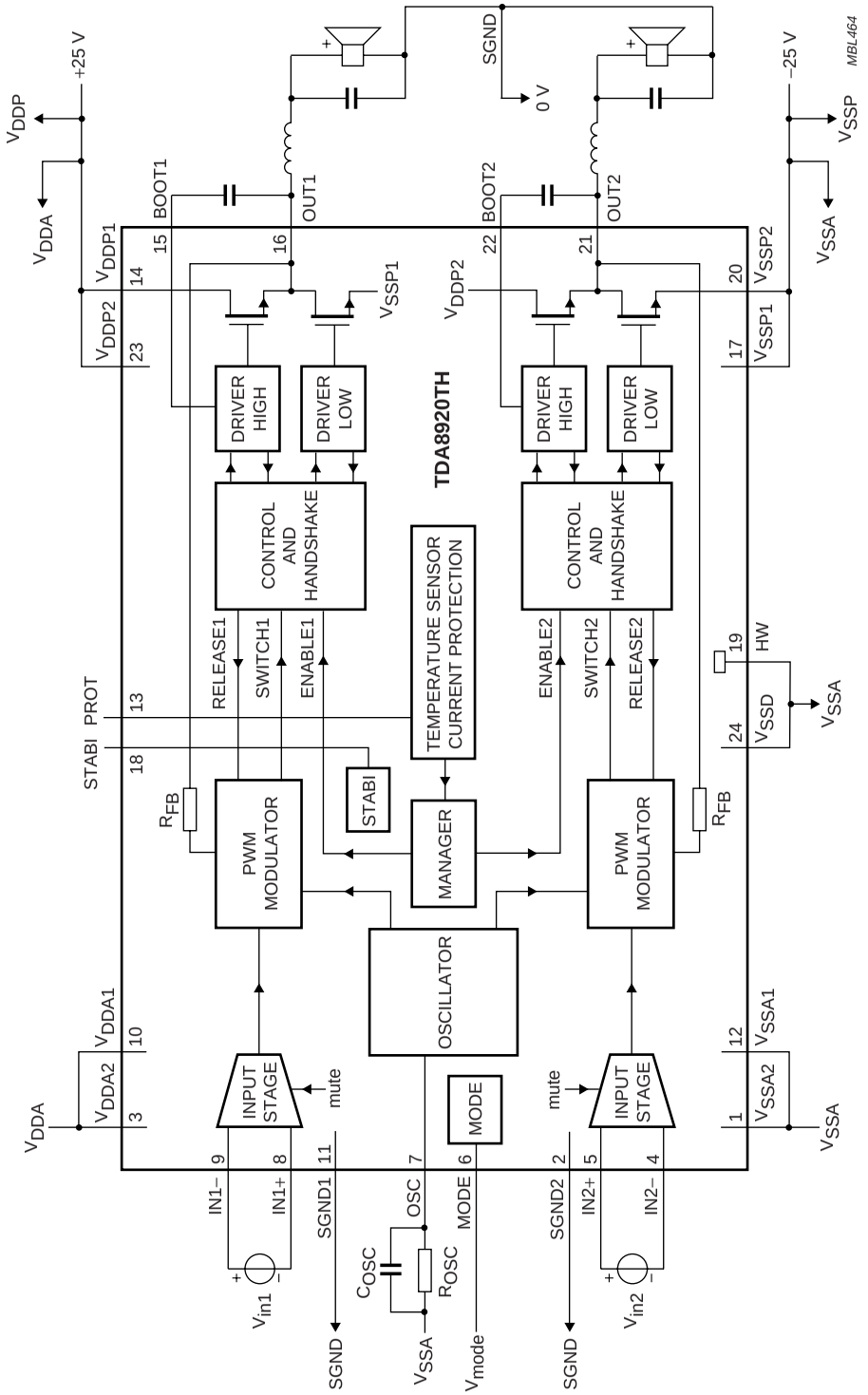
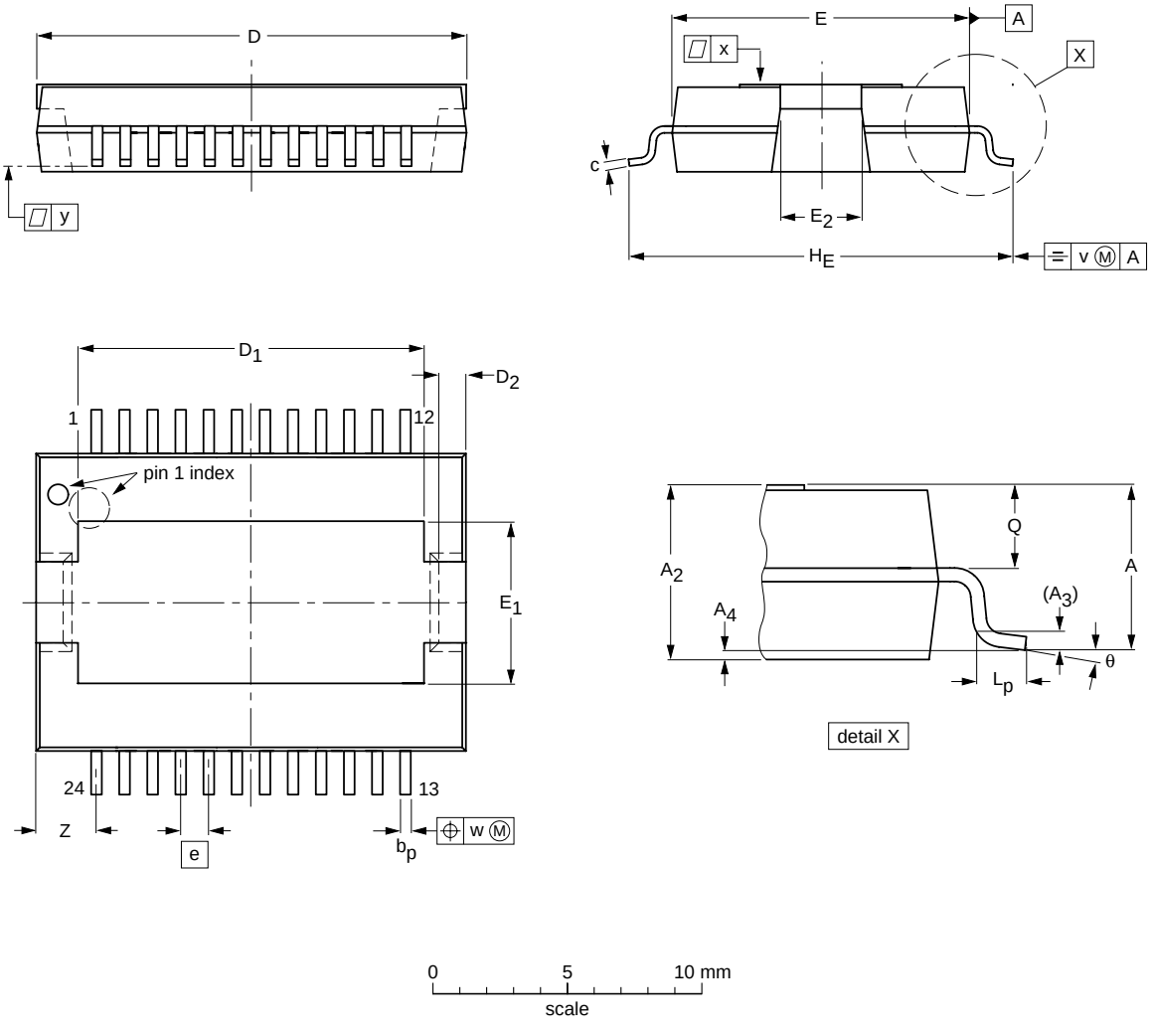


Fig.37 Typical application schematic of TDA8920TH.

17 PACKAGE OUTLINE

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						02-01-30

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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