



## MIC4126/27/28

### Dual 1.5A-Peak Low-Side MOSFET Drivers in Advanced Packaging

## General Description

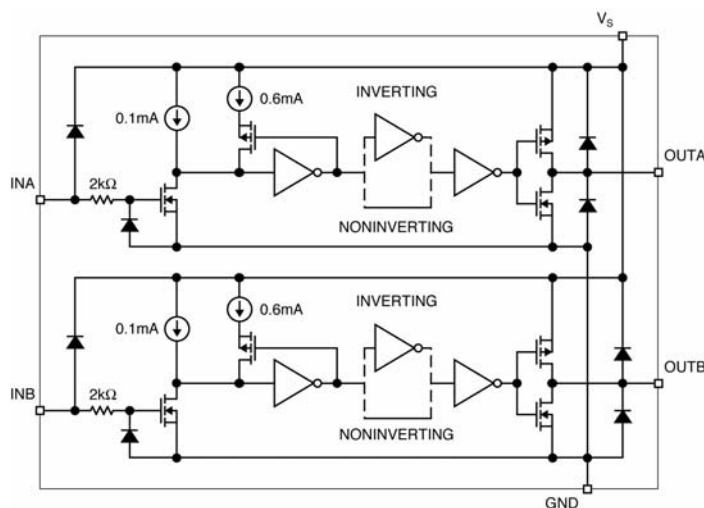
The MIC4126, MIC4127, and MIC4128 family are highly-reliable dual 1.5A low-side MOSFET drivers fabricated on Micrel's BiCMOS/DMOS process. The devices feature low power consumption and high efficiency. The MIC4126/27/28 translate TTL or CMOS input logic levels to output voltage levels that swing within 25mV of the positive supply or ground whereas comparable bipolar devices are capable of swinging only to within 1V of the supply. The MIC4126/7/8 is available in three configurations: dual inverting, dual non-inverting, and complimentary output.

The MIC4126/27/28 offer pin-compatible as well as smaller footprint replacements for the MIC4426/27/28 with improved packaging and electrical performance. The MIC4126/27/28 are available in exposed pad, EPAD, SOIC-8L and MSOP-8L options as well as a small-size 3mm x 3mm MLF™-8L option. The devices have an input operating range of 4.5V to 20V.

Primarily intended for driving power MOSFETs, MIC4426/7/8 drivers are suitable for driving other loads (capacitive, resistive, or inductive) which require low-impedance, high peak current, and fast switching time. The devices can withstand up to 500mA of reverse current (either polarity) without latching and up to 5V noise spikes (either polarity) on ground pins.

Data sheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

## Functional Diagram



MIC4126/27/28 Block Diagram

## Features

- Dual 1.5A-peak drivers
- 4.5V to 20V operating range
- Exposed backside pad packaging reduces heat
  - ePAD SOIC-8L ( $\theta_{JA} = 58^{\circ}\text{C/W}$ )
  - ePAD MSOP-8L ( $\theta_{JA} = 60^{\circ}\text{C/W}$ )
  - 3mm x 3mm MLF™-8L ( $\theta_{JA} = 60^{\circ}\text{C/W}$ )
- Bipolar/CMOS/DMOS construction
  - 25mV maximum output offset from supply or ground
- Latch-up protection to >200mA reverse current
- Switches 1000pF in 25ns
- Logic-input threshold independent of supply voltage
- Logic-input protection to -5V
- 6pF typical equivalent input capacitance
- Dual inverting, dual non-inverting, and complementary configurations
- -40°C to +125°C operating junction temperature range

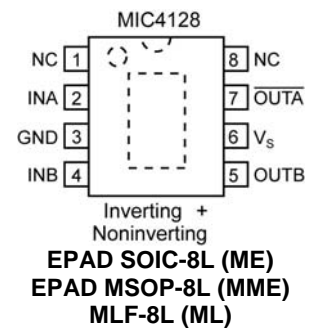
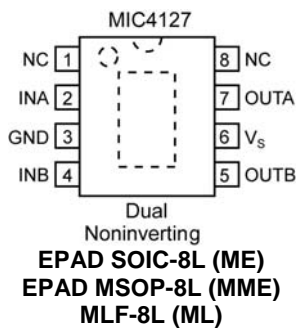
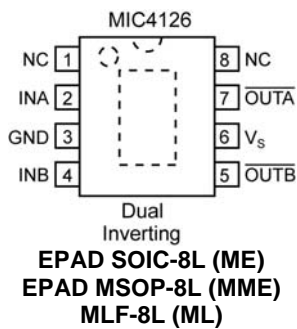
## Applications

- DC/DC converters
- Motor drivers
- Clock line driver

## Ordering Information

Part Number	Configuration	Package	Junction Temp. Range <sup>(1)</sup>	Lead Finish
MIC4126YME	Dual Inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4126YMME	Dual Inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4126YML	Dual Inverting	8-lead MLF	–40° to +125°C	Pb-Free
MIC4127YME	Dual Non-inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4127YMME	Dual Non-inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4127YML	Dual Non-inverting	8-lead MLF	–40° to +125°C	Pb-Free
MIC4128YME	Inverting + Non-inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4128YMME	Inverting + Non-inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4128YML	Inverting + Non-inverting	8-lead MLF	–40° to +125°C	Pb-Free

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Function
1, 8	NC	Not internally connected
2	INA	Control Input A: TTL/CMOS compatible logic input
3	GND	Ground
4	INB	Control Input B: TTL/CMOS compatible logic input.
5	OUTB	Output B: CMOS totem-pole output.
6	V <sub>S</sub>	Supply Input: +4.5V to +20V
7	OUTA	Output A: CMOS totem-pole output.
EP	GND	Ground, backside pad.

**Absolute Maximum Ratings <sup>(1)</sup>**

Supply Voltage ( $V_S$ ) ..... +24V  
 Input Voltage ( $V_{IN}$ ) .....  $V_S + 0.3V$  to GND – 5V  
 Junction Temperature ( $T_J$ ) ..... 150°C  
 Storage Temperature ..... –65°C to +150°C  
 Lead Temperature (10 sec.) ..... 300°C  
 ESD Rating, **Note 3**

**Operating Ratings <sup>(2)</sup>**

Supply Voltage ( $V_S$ ) ..... +4.5V to +20V  
 Temperature Range ( $T_J$ ) ..... –40°C to +125°C  
 Package Thermal Resistance  
   3X3 MLF™  $\theta_{JA}$  ..... 60°C/W  
   EPAD MSOP-8L  $\theta_{JA}$  ..... 60°C/W  
   EPAD SOIC-8L  $\theta_{JA}$  ..... 58°C/W

**Electrical Characteristics <sup>(4)</sup>**

4.5V  $\leq V_S \leq 20V$ ; Input voltage slew rate  $>1V/\mu s$ ;  $C_{OUT} = 1000pF$ .  $T_A = 25^\circ C$ , **bold** values indicate full specified temperature range; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Input</b>						
$V_{IH}$	Logic 1 Input Voltage		2.4 <b>2.4</b>	1.4 <b>1.6</b>		V
$V_{IL}$	Logic 0 Input Voltage			1.1 <b>1.3</b>	0.8 <b>0.8</b>	V
$I_{IN}$	Input Current	$0 \leq V_{IN} \leq V_S$	–1		1	$\mu A$
<b>Output</b>						
$V_{OH}$	High Output Voltage		<b><math>V_S - 0.025</math></b>			V
$V_{OL}$	Low Output Voltage				<b>0.025</b>	V
$R_O$	Output Resistance	$I_{OUT} = 10mA$ , $V_S = 20V$		6 <b>8</b>	10 <b>12</b>	$\Omega$
$I_{PK}$	Peak Output Current			<b>1.5</b>		A
I	Latch-Up Protection	Withstand reverse current	<b>&gt;200</b>			mA
<b>Switching Time</b>						
$t_R$	Rise Time	Test Figure 1		13 <b>20</b>	30 <b>40</b>	ns
$t_F$	Fall Time	Test Figure 1		15 <b>18</b>	25 <b>40</b>	ns
$t_{D1}$	Delay Time	Test Figure 1		37 <b>43</b>	50 <b>60</b>	ns
$t_{D2}$	Delay Time	Test Figure 1		40 <b>45</b>	60 <b>70</b>	ns
<b>Power Supply</b>						
$I_S$	Power Supply Current	$V_{INA} = V_{INB} = 3.0V$		1.4 <b>1.5</b>	4.5 <b>8</b>	mA
$I_S$	Power Supply Current	$V_{INA} = V_{INB} = 0.0V$		0.18 <b>0.19</b>	0.4 <b>0.6</b>	mA

**Notes:**

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5k $\Omega$  in series with 100pF.
- Specification for packaged product only.

## Test Circuit

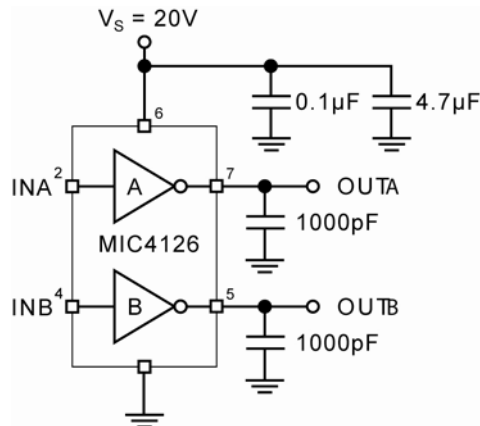


Figure 1a. Inverting Configuration

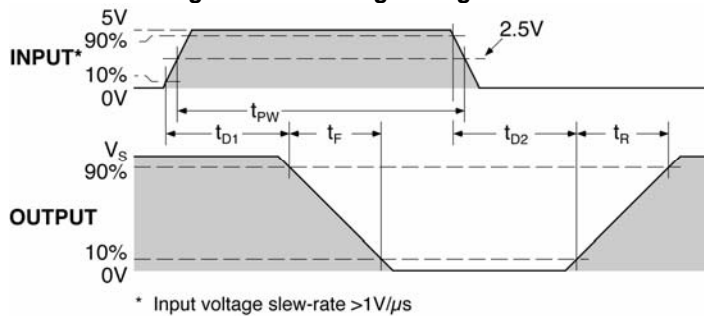


Figure 1b. Inverting Timing

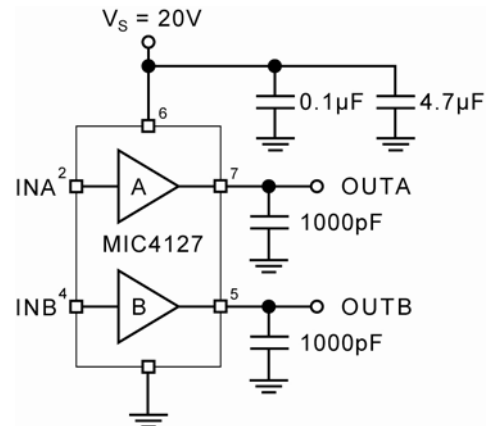


Figure 2a. Non-inverting Configuration

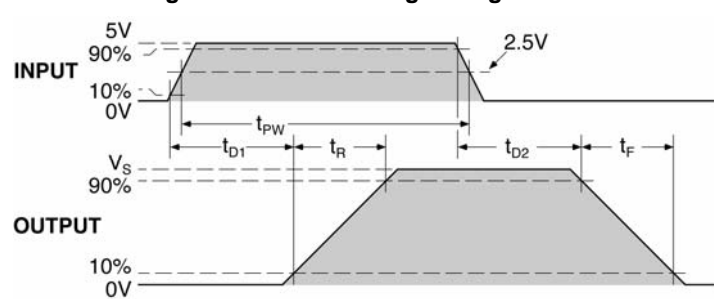
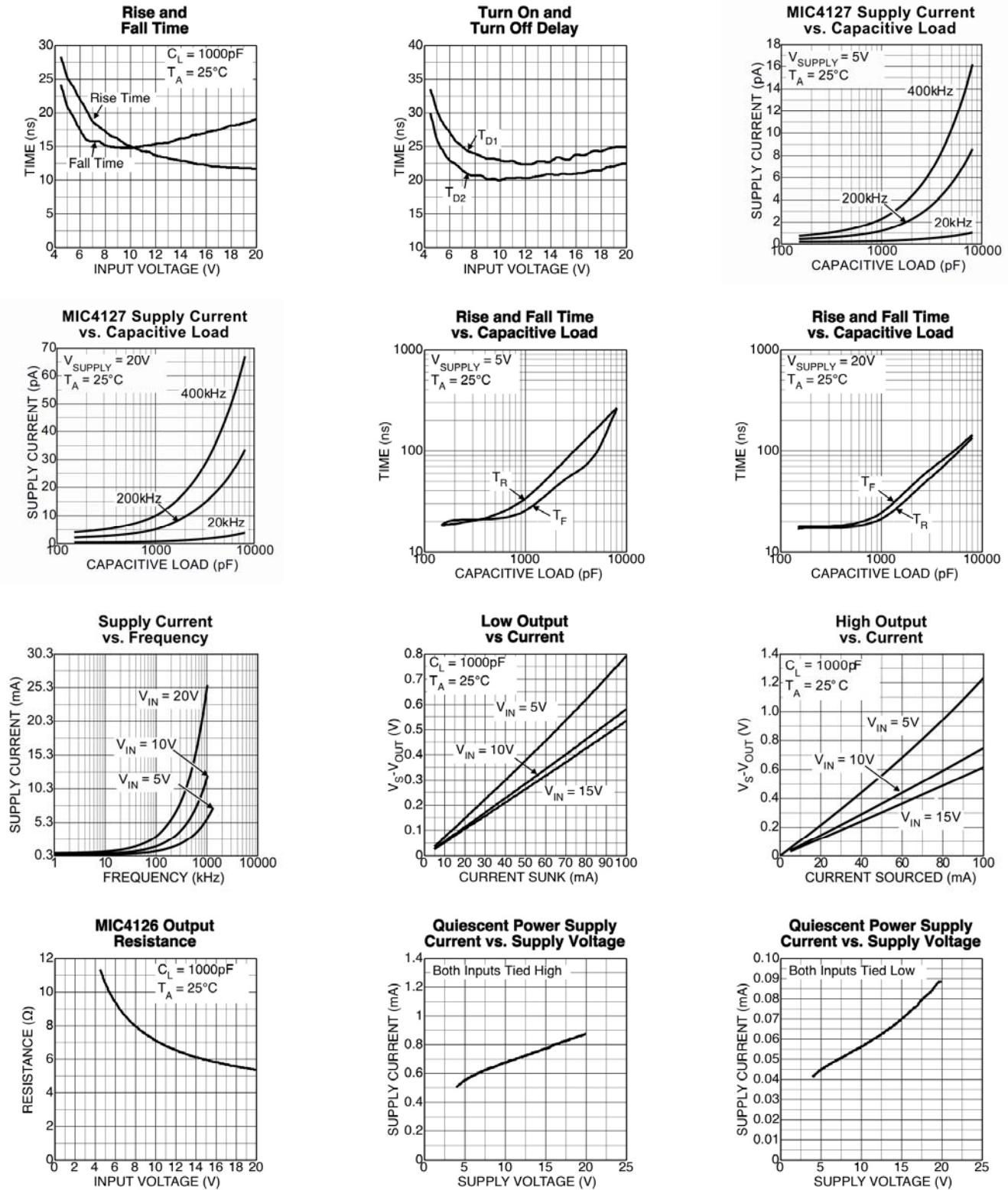


Figure 2b. Non-inverting Timing

## Typical Characteristics



## Application Information

### Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load by 16V in 25ns requires 0.8A from the supply input.

To guarantee low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (< 0.5") should be used. A 1.0μF film capacitor in parallel with one or two 0.1μF ceramic MLC capacitors normally provides adequate bypassing.

### Grounding

When using the inverting drivers in the MIC4126 or MIC4128, individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed. The voltage drop that occurs between the driver's ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

The E-pad and MLF packages have an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

### Control Input

Unused driver inputs must be connected to logic high (which can be  $V_S$ ) or ground. For the lowest quiescent current (< 500μA), connect unused inputs-to-ground. A logic-high signal will cause the driver to draw up to 9mA.

The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to  $V_S$  as a logic high and draws less than 1μA within this range.

### Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value

for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation ( $P_L + P_T$ ).

#### Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver's output resistance is:

$$P_L = I_L^2 R_O$$

For capacitive loads, the dissipation in the driver is:

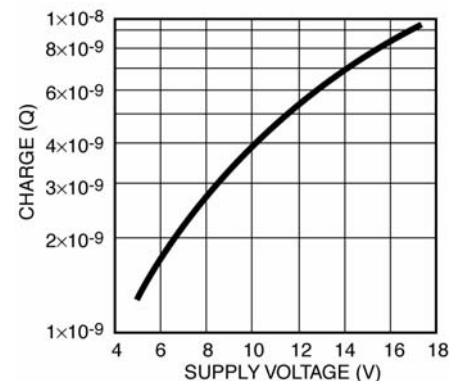
$$P_L = f C_L V_S^2$$

#### Transition Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

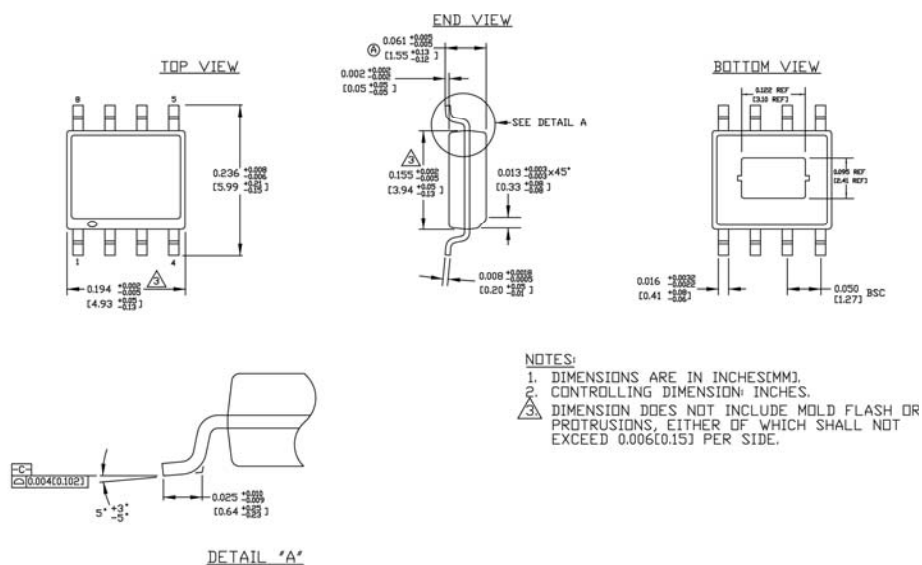
$$P_T = 2 f V_S Q$$

Charge (Q) is read from the following graph:

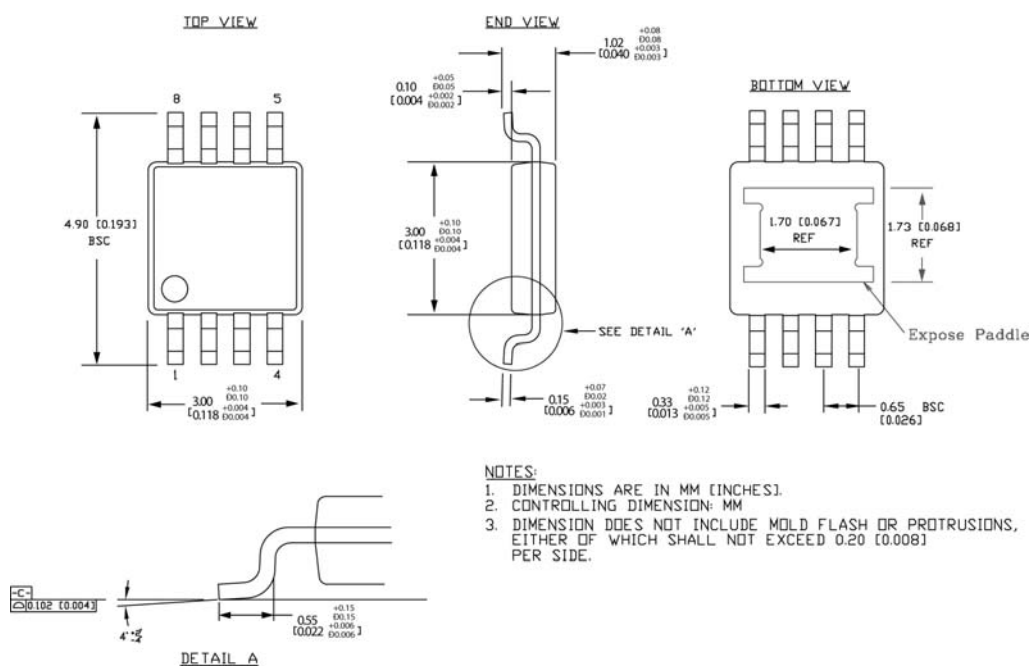


**Crossover Energy Loss per Transition**

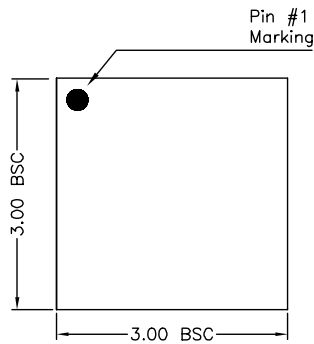
## Package Information



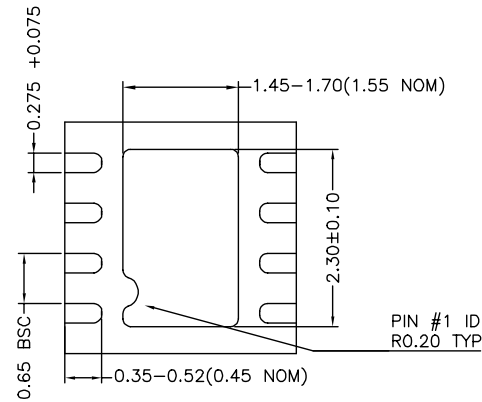
### 8-Pin Exposed Pad SOIC (M)



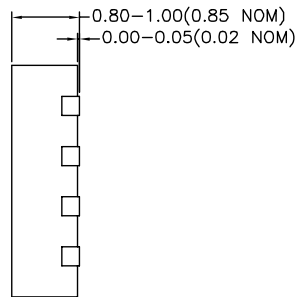
### 8-Pin Exposed Pad MSOP (MM)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

**8-Pin MLF (ML)**

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