Ordering number : EN6201B

LB1876

Monolithic Digital IC

For Polygon Mirror Motors

3-phase Brushless Motor Driver

ON Semiconductor®

http://onsemi.com

Overview

The LB1876 is a driver for polygon mirror motors such as used in laser printers and similar equipment.
It incorporates all necessary circuitry (speed control + driver) on a single chip. Direct PWM drive enables drive with low power loss.

Features

- 3-phase bipolar drive
- Direct PWM drive technique
- Built-in lower side output diode
- Output current limiter
- Reference clock input circuit (FG frequency equivalent)
- PLL speed control circuit
- Phase lock detector output (with masking function)
- Built-in protection circuitry includes current limiter, restraint protection, overheat protection, low-voltage protection, etc.
- Brake method switching circuit (free-run or reverse torque)
- 5V regulator output
- Power save function

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		30	V
Maximum output current	I_O max	t ≤ 500ms	2.5	A
Allowable power dissipation	Pd max1	Independent IC	0.9	W
	Pd max2	Mounted on a specified board*	2.1	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

*Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage range	V_{CC}		9.5 to 28	V
5V regulated output current	I_{REG}		0 to -20	mA
LD pin voltage	V_{LD}		0 to 28	V
FGS pin voltage	V_{FGS}		0 to 28	V
LD pin output current	I_{LD}		0 to 15	mA
FGS pin output current	I_{FGS}		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CC}1$			17	22	mA
	$I_{CC}2$	Quiescent Current		3.6	5.0	mA
5V Regulated Output						
Output voltage	VREG		4.65	5.0	5.35	V
Voltage fluctuation	$\Delta V_{REG}1$	V_{CC} = 9.5 to 28V		50	100	mV
Load fluctuation	$\Delta V_{REG}2$	I_O = -5 to -20mA		30	100	mV
Temperature coefficient	$\Delta V_{REG}3$	Design target value*		0		mV/°C
Output Block						
Output saturation voltage	$V_O$sat1	I_O = 1.0A, V_O(SINK) + V_O(SOURCE)		2.0	2.5	V
	$V_O$sat2	I_O = 2.0A, V_O(SINK) + V_O(SOURCE)		2.6	3.2	V
Output leak current	$I_O$leak				100	µA
Lower side diode forward voltage	V_D1	I_D = -1.0A		1.2	1.5	V
	V_D2	I_D = -2.0A		1.5	1.9	V
Hall Amplifier Block						
Input bias current	I_{HB}		-2	-0.5		µA
Common mode input voltage range	V_{ICM}		0		V_{REG}-2.0	V
Hall input sensitivity	V_{IN}(HA)		80			mVp-p
Hysteresis width	ΔV_{IN}(HA)		15	24	42	mV
Input voltage L → H	V_{SLH}			12		mV
Input voltage H → L	V_{SHL}			-12		mV
FG/Schmitt Block						
Input bias current	I_B(FGS)		-2	-0.5		µA
Common mode input voltage range	V_{ICM}(FGS)		0		V_{REG}-2.0	V
Input sensitivity	V_{IN}(FGS)		80			mVp-p
Hysteresis width	ΔV_{IN}(FGS)		15	24	42	mV
Input voltage L → H	V_{SLH}(FGS)			12		mV
Input voltage H → L	V_{SHL}(FGS)			-12		mV
PWM Oscillator						
Output High level voltage	V_{OH}(PWM)		2.5	2.8	3.1	V
Output Low level voltage	V_{OL}(PWM)		1.2	1.5	1.8	V
External capacitor charge current	I_{CHG}	V_{PWM} = 2V	-125	-95	-75	µA
Oscillator frequency	f(PWM)	C = 3000pF		22		kHz
Amplitude	V(PWM)		1.05	1.27	1.50	Vp-p
FGS Output						
Output saturation voltage	V_{OL}(FGS)	I_{FGS} = 7mA		0.15	0.5	V
Output leak current	I_L(FGS)				10	µA
CSD Oscillator						
Output High level voltage	V_{OH}(CSD)		2.65	3.0	3.3	V
Output Low level voltage	V_{OL}CSD)		0.75	0.9	1.1	V
Amplitude	V(CSD)		1.75	2.1	2.3	Vp-p
External capacitor charge current	$I_{CHG}1$		-13.5	-9	-5.5	µA
External capacitor discharge current	$I_{CHG}2$		5.5	9	13.5	µA
Oscillator frequency	f(CSD)	C = 0.068µF		30		Hz

*Design target value, Do not measurement.

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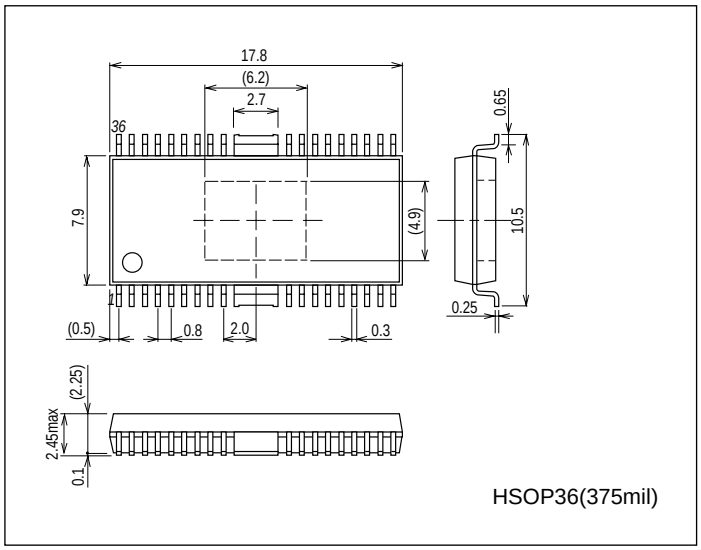
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Phase Comparator Output						
Output High level voltage	V_{PDH}	I_{OH} = -100µA	V_{REG}-0.2	V_{REG}-0.1		V
Output Low level voltage	V_{PDL}	I_{OH} = 100µA		0.2	0.3	V
Output source current	I_{PD}^{+}	V_{PD} = V_{REG}/2			-0.5	mA
Output sink current	I_{PD}^{-}	V_{PD} = V_{REG}/2	1.5			mA
Phase Lock Detector Output						
Output saturation voltage	V_{OL}(LD)	I_{LD} = 10mA		0.15	0.5	V
Output leak current	I_L(LD)	V_O = V_{CC}			10	µA
Error Amplifier						
Input offset voltage	V_{IO}(ER)	Design target value*	-10		+10	mV
Input bias current	I_B(ER)		-1		+1	µA
Output High level voltage	V_{OH}(ER)	I_{OH} = -500µA	V_{REG}-1.2	V_{REG}-0.9		V
Output Low level voltage	V_{OL}(ER)	I_{OL} = 500µA		0.9	1.2	V
DC bias level	V_B(ER)		-5%	V_{REG}/2	+5%	V
Current Limiter						
Drive gain	G_{DF}1	In phase lock mode	0.4	0.5	0.6	times
	G_{DF}2	In unlock mode	0.8	1.0	1.2	times
Limiter voltage	V_{RF}	V_{CC} - VM	0.45	0.5	0.55	V
Thermal Shutdown Operation						
Operating temperature	TSD	Design target value* (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value* (junction temperature)		40		°C
Low Voltage Protection						
Operating voltage	V_{SD}		8.1	8.5	8.9	V
Hysteresis	ΔV_{SD}		0.2	0.35	0.5	V
CLD Circuit						
External capacitor charge current	I_{CLD}		-6	-4.3	-3	V
Operating voltage	V_H(CLD		3.25	3.5	3.75	V
CLK Pin						
External input frequency	f_I(CKIN)		0.1		10	kHz
High level input voltage	V_{IH}(CKIN)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(CKIN)		0		1.5	V
Input open voltage	V_{IO}(CKIN)		V_{REG}-0.5		V_{REG}	V
Hysteresis width	V_{IS}(CKIN)		0.35	0.5	0.65	V
High level input current	I_{IH}(CKIN)	V_{CKIN} = V_{REG}	-10	0	+10	µA
Low level input current	I_{IL}(CKIN)	V_{CKIN} = 0V	-280	-210		µA
S/S Pin						
High level input voltage	V_{IH}(SS)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(SS)		0		1.5	V
Input open voltage	V_{IO}(SS)		V_{REG}-0.5		V_{REG}	V
Hysteresis width	V_{IS}(SS)		0.35	0.5	0.65	V
High level input current	I_{IH}(SS)	$V_{S/S}$ = V_{REG}	-10	0	+10	µA
Low level input current	I_{IL}(SS)	$V_{S/S}$ = 0V	-280	-210		µA
LDSEL Pin						
High level input voltage	$V_{IH}(LD_{SEL})$		3.5		V_{REG}	V
Low level input voltage	$V_{IL}(LD_{SEL})$		0		1.5	V
Input open voltage	$V_{IO}(LD_{SEL})$		V_{REG}-0.5		V_{REG}	V
High level input current	$I_{IH}(LD_{SEL})$	V_{LDSEL} = V_{REG}	-10	0	+10	µA
Low level input current	$I_{IL}(LD_{SEL})$	V_{LDSEL} = 0V	-280	-210		µA
BRSEL Pin						
High level input voltage	$V_{IH}(BR_{SEL})$		3.5		V_{REG}	V
Low level input voltage	$V_{IL}(BR_{SEL})$		0		1.5	V
Input open voltage	$V_{IO}(BR_{SEL})$		V_{REG}-0.5		V_{REG}	V
High level input current	$I_{IH}(BR_{SEL})$	V_{BRSEL} = V_{REG}	-10	0	+10	µA
Low level input current	$I_{IL}(BR_{SEL})$	V_{BRSEL} = 0V	-280	-210		µA

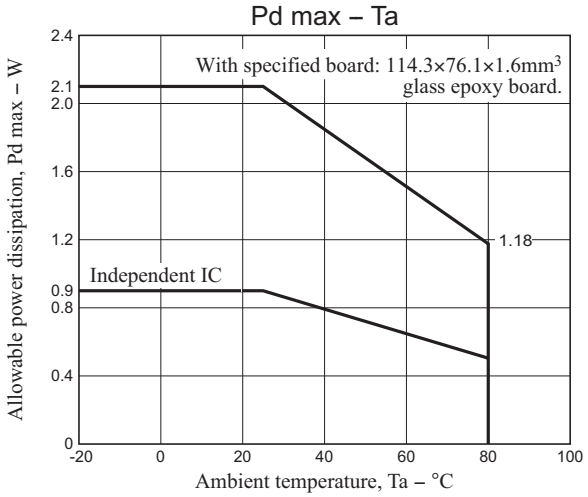
*Design target value, Do not measurement.

Package Dimensions

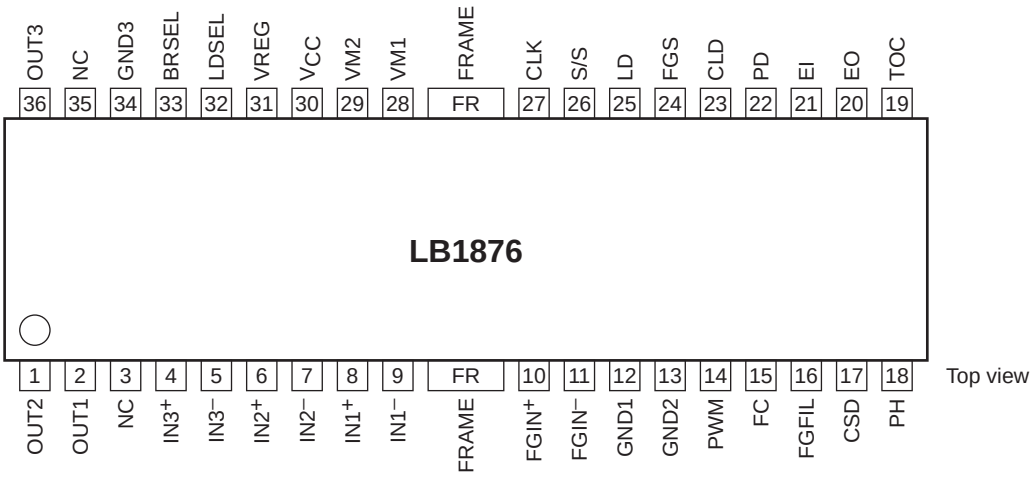
unit : mm (typ)

3235A





Pin Assignment

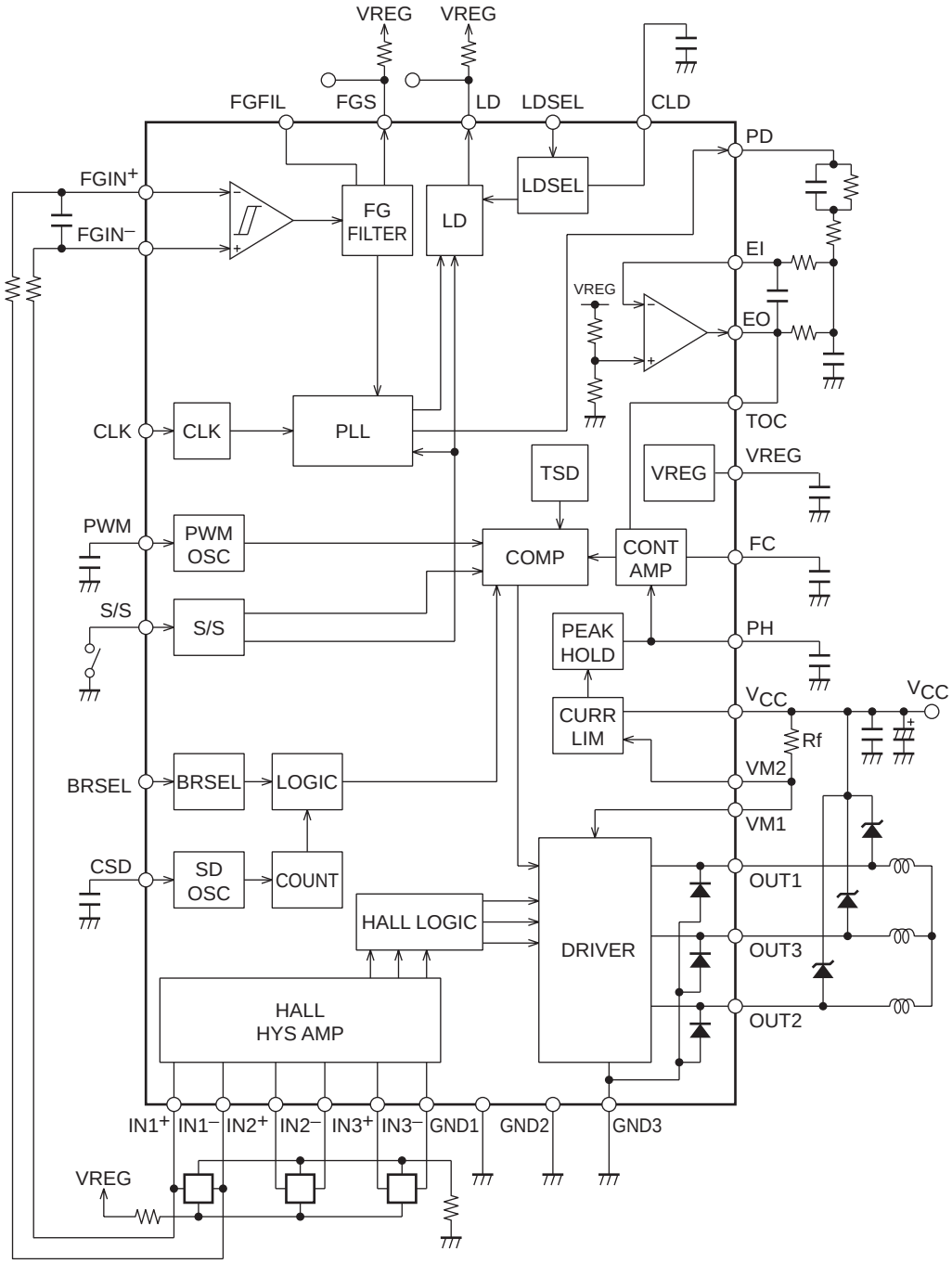


3-phase Logic Truth Table

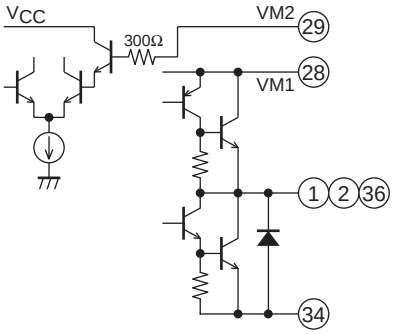
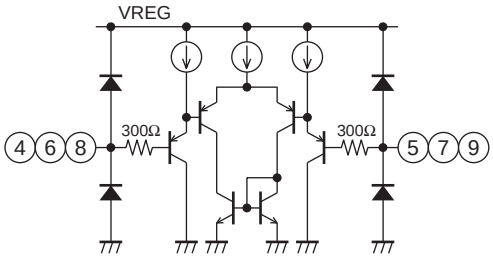
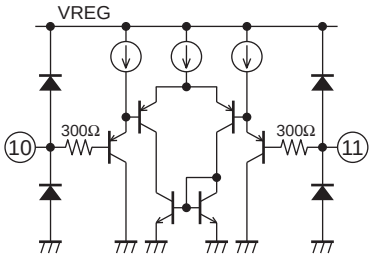
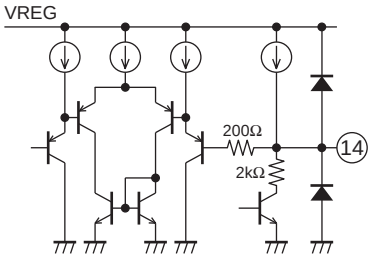
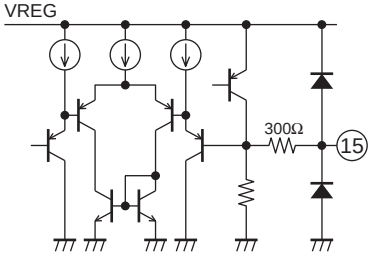
IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

IN = "H" indicates the $IN^+ > IN^-$ condition.

Block Diagram



Pin Function

Pin No.	Pin name	Function	Equivalent curcuit
2 1 36	OUT1 OUT2 OUT3	Motor drive output pins. PWM controls duty cycle ratio by lower transistors. Connect Schottky diodes between the outputs and V_{CC}.	
34	GND3	Output block ground.	
28 29	VM1 VM2	Output block power supply and output current detection. VM1 and VM2 are short-circuited and used. Connect low-resistance resistors Rf between these pins and V_{CC}. The output current is limited to the current value set by $I_{OUT} = V_{REF}/Rf$.	
3 35	NC NC	Since these are not connected internally, they can be used for wiring.	
8 9 6 7 4 5	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall device input pins. These inputs return a high level when $IN^+ > IN^-$ and a low level when $IN^- > IN^+$. A Hall signal amplitude of at least 100mVp-p (differential) is desirable. Insert a capacitor between IN^+ and IN^- if noise on the Hall signal is a problem.	
10 11	$FGIN^+$ $FGIN^-$	FG comparator input pins. If noise on the FG signal is a problem, insert either a capacitor or a filter consisting of a capacitor and a resistor.	
12	GND1	Control circuit block ground.	
13	GND2	Sub-ground.	
14	PWM	PWM oscillation frequency setting pin. Connect a capacitor between this pin and ground. A capacitance of 1800pF for C sets the frequency to approximately 37kHz.	
15	FC	Current control circuit frequency characteristics compensation pin. Insert a capacitor (on the order of 0.01 to 0.1μF) between this pin and ground. The output duty is determined by the ratio of the voltage on this pin and the PWM oscillator waveform.	

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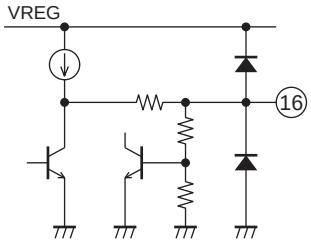
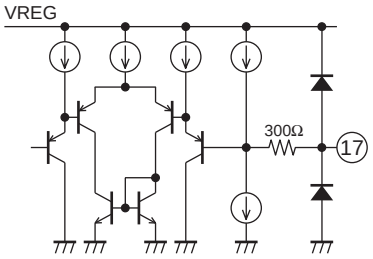
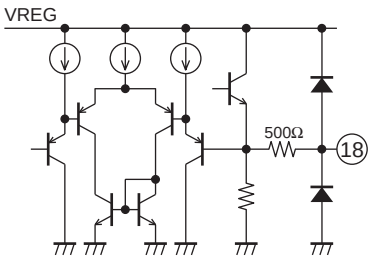
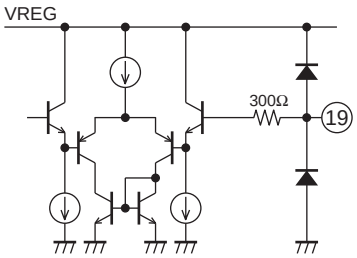
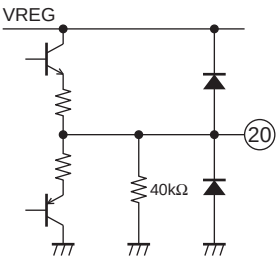
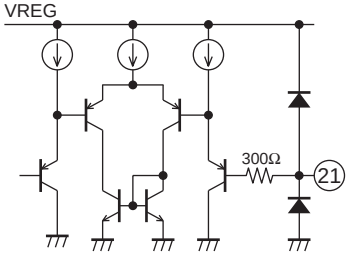
Pin No.	Pin name	Function	Equivalent curcuit
16	FGFIL	FG filter pin. If noise on the FG signal is a problem, insert a capacitor (under about 2200pF) between this pin and ground.	
17	CSD	Restraint protection circuit operating time setting pin/reset pulse setting pin. A protection operating time of about 8 seconds can be set by connecting a capacitor (about 0.068μF) between this pin and ground. If the protection circuit is not used, connect a capacitor and resistor (about 4700pF, 220kΩ) in parallel between this pin and ground.	
18	PH	RF waveform smoothing pin. If noise on the RF signal is a problem, insert a capacitor between this pin and ground.	
19	TOC	Torque specifying input pin. Normally, this pin is connected to the EO pin. When the TOC voltage falls, the on duty of the lower side transistor increases.	
20	EO	Error amplifier output pin.	
21	EI	Error amplifier input pin.	

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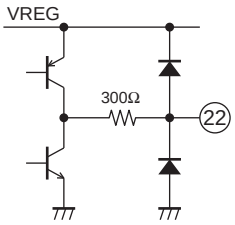
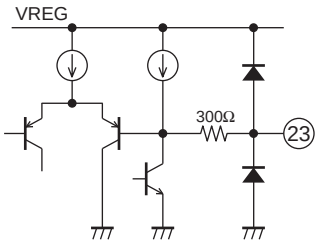
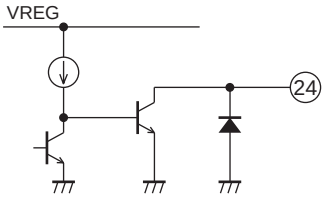
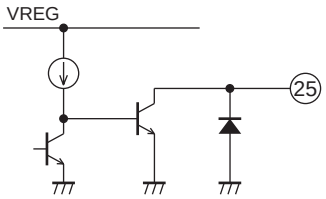
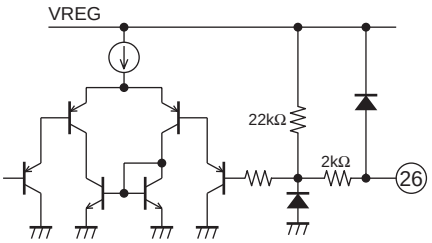
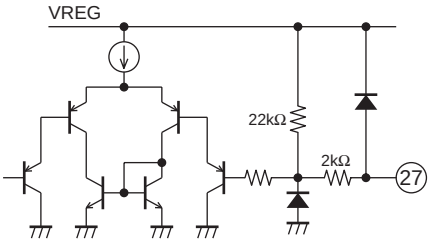
Pin No.	Pin name	Function	Equivalent curcuit
22	PD	Phase comparator output pin. The phase error is converted to a pulse duty and output from this pin.	
23	CLD	Phase lock signal mask time setting pin. A mask time of about 90ms can be set by inserting a capacitor (about 0.1μF) between this pin and ground. Leave this pin open if there is no need to mask.	
24	FGS	FG Schmitt output pin. Open collector output.	
25	LD	Phase lock detection output pin. Open collector output. Turns on (goes low) when phase lock is detected.	
26	S/S	Start/stop control pin. Low: 0 to 1.5V High: 3.5V to VREG Hysteresis: About 0.5V Apply a low level to start; this pin goes high when open.	
27	CLK	Clock input pin. Low: 0 to 1.5V High: 3.5V to VREG Hysteresis: About 0.5 V f_{CLK} = 10kHz maximum If there is noise on the clock signal, remove that noise with a capacitor.	
30	V_{CC}	Power supply pin Insert a capacitor between this pin and ground to prevent noise from entering the IC. (Use a value of 20 or 30μF or higher.)	

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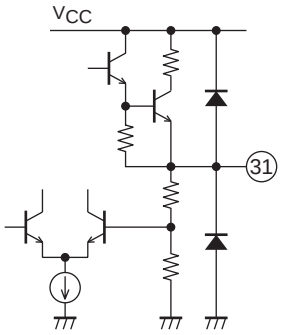
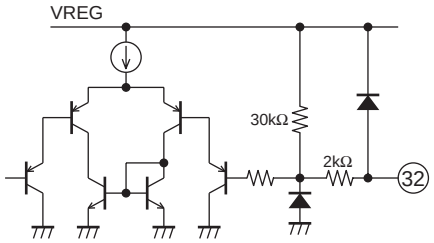
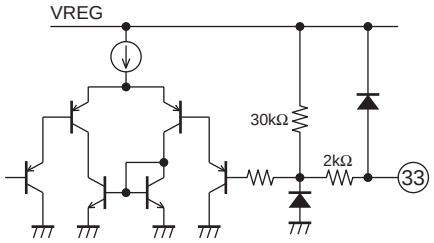
Pin No.	Pin name	Function	Equivalent curcuit
31	VREG	Stabilized power supply output (5V output) pin. Insert a capacitor between this pin and ground for stabilization. (About 0.1μF.)	
32	LDSEL	Phase lock signal mask switching pin. Low: 0 to 1.5V High: 3.5V to VREG When open, this pin goes to the high level. When low, transient unlock signals (short high-level periods on the LD output) are masked, and when high, transient lock signals (short low-level periods on the LD output) are masked.	
33	BRSEL	Braking control pin. Low: 0 to 1.5V High: 3.5V to VREG When open, this pin goes to the high level. When low, reverse torque control is applied and when high, the circuit operates in free-running mode. An external Schottky barrier diode is required on the low side output when reverse torque control is applied.	
–	FRAME	The FRAME pin is connected internally to the metal frame at the base of the IC. Electrically, both the FRAME pin and the metal frame are left open. To improve thermal dissipation, provide a corresponding land on the PCB and solder the FRAME pin to that land.	

LB1876 Overview

1. Speed control circuit

This IC provides high-precision, low-jitter, and stable motor rotation since it adopts a PLL speed control technique. This PLL circuit compares the phases of the edges on the CLK signal (falling edges) and the FG signal (falling edges on the $FGIN^+$, FGS output) and controls the speed using that error output.

The FG servo frequency during control operation is the same as the clock frequency.

$$f_{FG}(servo) = f_{CLK}$$

2. Output drive circuit

To reduce power loss in the output, this IC adopts a direct PWM drive technique. The output transistors are always saturated when on, and the motor drive power is controlled by changing the output on duty. Since the lower side transistor is used for the output PWM switching, Schottky diodes must be inserted between the outputs and V_{CC}. (This is because if the diodes used do not have a short reverse recovery time, instantaneous through currents will flow when the lower side transistor turns on.)

The diodes between the outputs and ground are built in. However, if problems (such as waveform disruption during lower side kickback) occur for large output currents, attach external rectifying diodes or Schottky diodes. If reverse control mode is selected for braking and problems such as incorrect operation or excess heat generation due to the reverse recovery time of the lower side diode causes a problem, add an external Schottky diode.

3. Current control circuit

The current control circuit controls the current (limits the peak current) to the current determined by $I = V_{RF}/Rf$ (V_{RF} = 0.5V typ., Rf: current detection resistor). The limiting operation consists of reducing the output on duty to suppress the current.

The current control circuit detects the diode reverse recovery current due to the PWM operation, and has an operating delay (about 3μ s) to prevent incorrect current limiting operation. If the motor coils have a relatively low resistance, or relatively low inductance, the changes in current flow at startup (the state where the motor presents no back electromotive force) will be rapid. As a result, the current limiter may operate at currents in excess of the set current due to this delay. In such cases, the current limit value must be set so as to take the current increase due to the delay into account.

4. Power saving circuit

This IC goes to the power saving state, which reduces power consumption, in the stopped state. Power is reduced in the power saving state by cutting the bias current to most of the circuit blocks in the IC. However, the 5 V regulator circuit does operate and provide its output in the power saving state.

5. Reference clock

The externally input clock signal must be free of chattering and other noise. The input circuit does have hysteresis, but if problems occur, the clock signal must be input through a capacitor or other noise reduction circuit.

If the IC is set to the start state with no reference clock input, and if the constraint protection circuit is operated, after the motor rotates a certain amount, the drive will be turned off. However, if the constraint protection circuit is not operated, and furthermore, if reverse control mode is selected during braking, the motor will run backwards at increasing speed. A workaround will be required in this case. (This problem occurs because the constraint protection circuit oscillator signal is used for clock cutoff protection.)

6. PWM frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$f_{PWM} \approx 1/(15000 \times C)$$

If an 1800pF capacitor is used, the frequency will be about 37kHz. If the PWM frequency is too low, the motor will emit audible switching noise, and if it is too high, the power loss will increase. A frequency in the range 15 to 50kHz is desirable. The capacitor ground must be connected as close as possible to the IC control block ground (the GND1 pin) to minimize the influence of the output on this circuit.

7. Hall sensor input signals

Input signals with amplitudes greater than the input circuit hysteresis (42mV maximum) must be provided to the Hall inputs. Input amplitudes of over 100mV are desirable to minimize the influence of noise. If the output waveform is disturbed by noise (at phase switching), insert capacitors across the input to prevent this.

8. FG input signal

Normally, one of the Hall sensor signals is input as an FG signal. If noise on the FG input is a problem, insert either a capacitor or a filter consisting of a capacitor and a resistor. Although it is possible to exclude noise from the FG signal by inserting a capacitor between the FGFIL pin and ground, if this pin's waveform is smoothed excessively, the circuit may not be able to operate normally. Therefore, if a capacitor is used here, its value must be held to under 2200pF. If the position of the capacitor's ground lead is inappropriate, problems due to noise may become more likely to occur. Select the position carefully.

9. Constraint protection circuit

This IC includes a built-in constraint protection circuit to protect the IC and the motor during motor constraint. In the start state, when the LD output is high for a fixed period (the unlocked state), the lower side transistor turns off. The time is set by the capacitor connected to the CSD pin.

Set time (seconds) ≈ 120 × C (μF)

If a 0.068μF capacitor is used, the protection time will be about 8 seconds. The set time must have a value that provides an adequate margin relative to the motor start time. The protection circuit does not operate during braking implemented by switching the clock frequency. Either switch to the stop state or turn off the power and restart to clear the constraint protection state.

Since the CSD pin also functions as the initial reset pulse generation pin, if connected to ground the logic circuits will be reset and speed control operation will not be possible. Therefore, if constraint protection is not used, connect CSD to ground through a resistor of about 220kΩ and a capacitor of about 4700pF in parallel.

10. Phase lock signal

(1) Phase lock range

Since this IC does not have a counter in the speed control system, the speed error range in the phase locked state cannot be determined solely by the IC's characteristics. (This is because of the influence of the acceleration of the changes in the FG frequency.) If it is necessary to stipulate this for the motor, it will be necessary to measure this with the actual motor. Since it is easier for speed errors to occur in the state where the FG acceleration is large, the largest speed errors are thought to occur during lock pull-in at startup and when unlocked due to clock frequency switching.

(2) Phase lock signal mask function

When the LDSEL pin is set high or left open, transient lock signals (short low-level periods on the LD output) is masked. This function masks short low-level periods due to hunting during pull-in and allows a stable lock signal to be output. However, the lock signal is delayed by amount of masking time.

When the LDSEL pin is set low, transient unlock signals (short high-level periods on the LD output) is masked. This function prevents short period high-level signals from being output.

The mask time is set with the capacitor connected between the CLD pin and ground.

Mask time (seconds) ≈ 0.9 × C (μF)

A mask time of about 90ms can be set by using a capacitor of about 0.1μF. If complete masking is required, the mask time must be set large enough to provide ample margin. If masking is not required, leave the CLD pin open.

11. Power supply stabilization

Since this IC provides a large output current and adopts a switching drive technique, it can easily disrupt the power supply line voltage. Therefore, capacitors with ample capacitance must be inserted between the V_{CC} pins and ground. If reverse control mode is selected during braking, the circuit will return current to the power supply. This means that the power supply lines are even more susceptible to disruption. Since the power supply is most easily influenced during lock pull-in at high motor speeds, this case requires particular care. Select capacitor values that are fully adequate for this case.

If diodes are inserted in the power supply lines to prevent damage if the power supply is connected with reverse polarity, the power supply voltage will be even more susceptible to disruption, and even larger capacitors must be used.

12. VREG stabilization

Insert a capacitor of at least 0.1μF to stabilize VREG, which is the control circuit power supply. The capacitor ground must be connected as close as possible to the IC control block ground (the GND1 pin).

13. Error amplifier circuit components

Locate the error amplifier components as close to the IC as possible to minimize the influence of noise on this circuit. Locate this circuit as far from the motor as possible.

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