MICROCHIP

25AA080A/B, 25LC080A/B

8K SPI™ Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25LC080A	2.5-5.5V	16 Byte	I, E	P, SN, ST, MS
25AA080A	1.8-5.5V	16 Byte	I	P, SN, ST, MS
25LC080B	2.5-5.5V	32 Byte	I, E	P, SN, ST, MS
25AA080B	1.8-5.5V	32 Byte	I	P, SN, ST, MS

Features

- Max. clock 10 MHz
- Low-power CMOS technology
- 1024 x 8-bit organization
- 16 byte page ('A' version devices)
- 32 byte page ('B' version devices)
- Write cycle time: 5 ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2 or all of array
- Built-in write protection
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential read
- High reliability
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature ranges supported;
  - Industrial (I):   -40°C to +85°C
  - Automotive (E):   -40°C to +125°C

Pin Function Table

| Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
Vcc	Supply Voltage

Description

The Microchip Technology Inc. 25AA080A/B, 25LC080A/B (25XX080A/B[*]) are 8 Kbit Serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface™ (SPI™) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts.

The 25XX080A/B is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, and 8-lead TSSOP. Pb-free (Pure Matte Sn) finish is also available.

Package Types (not to scale)
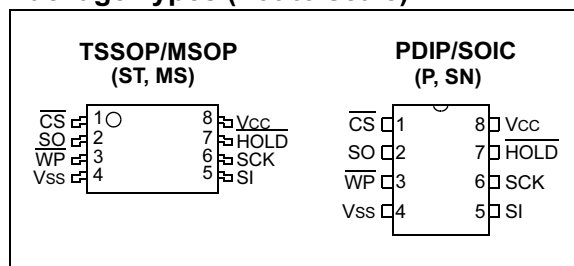
SPI is a registered trademark of Motorola Semiconductor.

*25XX080A/B is used in this document as a generic part number for the 25AA080A/B, 25LC080A/B.

25XX080A/B

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [†]

V_{CC}..7.0V

All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC} +1.0V

Storage temperature ....-65°C to 150°C

Ambient temperature under bias...-65°C to 125°C

ESD protection on all pins ....4 kV

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† NOTICE**:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_{AMB} = -40°C to +125°C V_{CC} = 2.5V to 5.5V				
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions	
D001	V_{IH1}	High-level input voltage	2.0	V_{CC} +1	V	$V_{CC} \geq 2.7V$ **(Note)**	
D002	V_{IH2}		0.7 V_{CC}	V_{CC} +1	V	$V_{CC}< 2.7V$ **(Note)**	
D003	V_{IL1}	Low-level input voltage	-0.3	0.8	V	$V_{CC} \geq 2.7V$ **(Note)**	
D004	V_{IL2}		-0.3	0.2 V_{CC}	V	$V_{CC} < 2.7V$ **(Note)**	
D005	V_{OL}	Low-level output voltage	—	0.4	V	I_{OL} = 2.1 mA	
D006	V_{OL}		—	0.2	V	I_{OL} = 1.0 mA, $V_{CC} < 2.5V$	
D007	V_{OH}	High-level output voltage	V_{CC} -0.5	—	V	I_{OH} = -400 μA	
D008	I_{LI}	Input leakage current		±1	μA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} TO V_{CC}	
D009	I_{LO}	Output leakage current		±1	μA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} TO V_{CC}	
D010	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_{AMB} = 25°C, CLK = 1.0 MHz, V_{CC} = 5.0V **(Note)**	
D011	I_{CC} Read	Operating Current	— —	6 2.5	mA mA	V_{CC} = 5.5V; F_{CLK} = 10.0 MHz; SO = Open V_{CC} = 2.5V; F_{CLK} = 5.0 MHz; SO = Open	
D012	I_{CC} Write		— —	3	mA	V_{CC} = 5.5V	
D013	I_{CCS}	Standby Current	— —	5 1	μA μA	$\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS}, T_{AMB} = -40°C TO +125°C $\overline{CS}$ = V_{CC} = 2.5V, Inputs tied to V_{CC} or V_{SS}, T_{AMB} = -40°C TO +85°C	

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2:   AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T$_{AMB}$ = -40°C to +85°C V$_{CC}$ = 1.8V to 5.5V Automotive (E): T$_{AMB}$ = -40°C to +125°C V$_{CC}$ = 2.5V to 5.5V			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	F$_{CLK}$	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
2	T$_{CSS}$	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
3	T$_{CSH}$	$\overline{CS}$ Hold Time	100 200 250	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
4	T$_{CSD}$	$\overline{CS}$ Disable Time	50	—	ns	—
5	Tsu	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
6	T$_{HD}$	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
7	T$_R$	CLK Rise Time	—	500	ns	**(Note 1)**
8	T$_F$	CLK Fall Time	—	500	ns	**(Note 1)**
9	T$_{HI}$	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
10	T$_{LO}$	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
11	T$_{CLD}$	Clock Delay Time	50	—	ns	—
12	T$_{CLE}$	Clock Enable Time	50	—	ns	—
13	T$_V$	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
14	T$_{HO}$	Output Hold Time	0	—	ns	(Note 1)
15	T$_{DIS}$	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V **(Note 1)** 2.5V ≤ V$_{CC}$ < 4.5V **(Note 1)** 1.8V ≤ V$_{CC}$ < 2.5V **(Note 1)**
16	T$_{HS}$	$\overline{HOLD}$ Setup Time	20 40 80	— — —	ns ns ns	4.5V ≤ V$_{CC}$ ≤ 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

3: T$_{WC}$ begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.
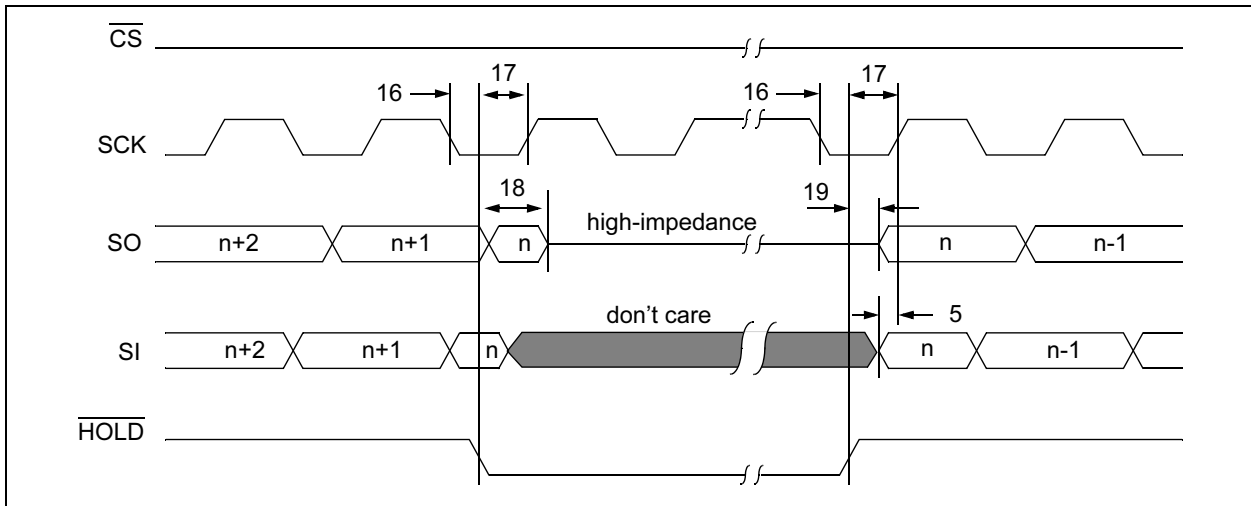
25XX080A/B

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

	AC CHARACTERISTICS		Industrial (I): T$_{AMB}$ = -40°C to +85°C V$_{CC}$ = 1.8V to 5.5V				Automotive (E): T$_{AMB}$ = -40°C to +125°C V$_{CC}$ = 2.5V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions	
17	T$_{HH}$	HOLD Hold Time	20	—	ns	4.5V ≤ V$_{CC}$ ≤ 5.5V	
			40	—	ns	2.5V ≤ V$_{CC}$ < 4.5V	
			80	—	ns	1.8V ≤ V$_{CC}$ < 2.5V	
18	T$_{HZ}$	HOLD Low to Output High-Z	30	—	ns	4.5V ≤ V$_{CC}$ ≤ 5.5V **(Note 1)**	
			60	—	ns	2.5V ≤ V$_{CC}$ < 4.5V **(Note 1)**	
			160	—	ns	1.8V ≤ V$_{CC}$ < 2.5V **(Note 1)**	
19	T$_{HV}$	HOLD High to Output Valid	30	—	ns	4.5V ≤ V$_{CC}$ ≤ 5.5V	
			60	—	ns	2.5V ≤ V$_{CC}$ < 4.5V	
			160	—	ns	1.8V ≤ V$_{CC}$ < 2.5V	
20	T$_{WC}$	Internal Write Cycle Time	—	5	ms	**(Note 3)**	
21	—	Endurance	1,000,000	—	E/W Cycles	**(Note 2)**	

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

3: T$_{WC}$ begins on the rising edge of CS after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-3: AC TEST CONDITIONS

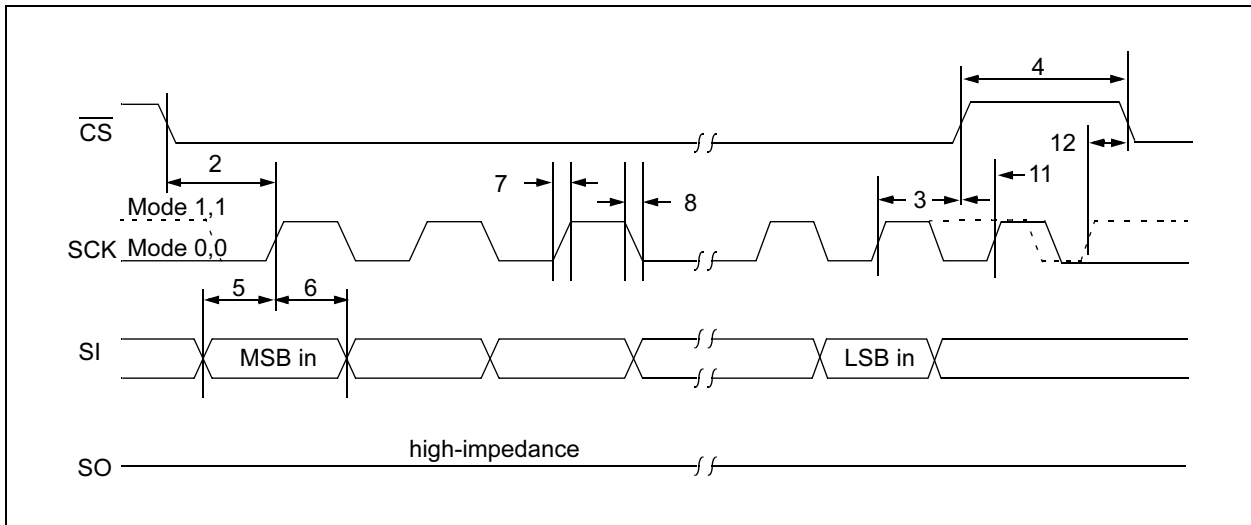| AC Waveform:	
V$_{LO}$ = 0.2V	—
V$_{HI}$ = V$_{CC}$ - 0.2V	**(Note 1)**
V$_{HI}$ = 4.0V	**(Note 2)**
Timing Measurement Reference Level	
Input	0.5 V$_{CC}$
Output	0.5 V$_{CC}$

Note 1: For V$_{CC}$ ≤ 4.0V
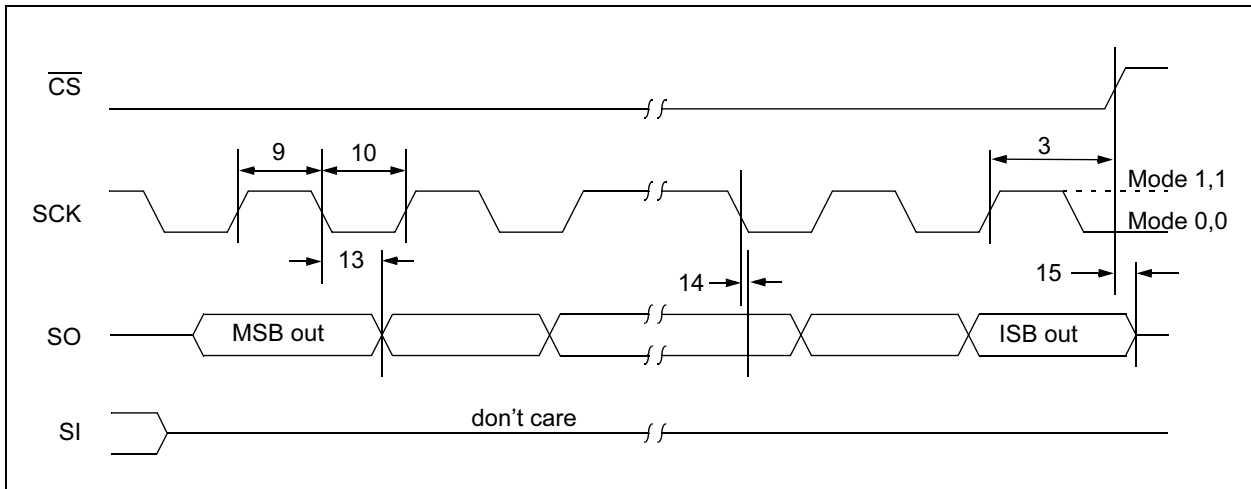
2: For V$_{CC}$ > 4.0V

FIGURE 1-1: **HOLD TIMING**

FIGURE 1-2: **SERIAL INPUT TIMING**

FIGURE 1-3: **SERIAL OUTPUT TIMING**

25XX080A/B

2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25XX080A/B are 1024 byte Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) Port of many of today's popular microcontroller families, including Microchip's PICmicro® microcontrollers. It may also interface with microcontrollers that do not have a built-in Synchronous Serial Port by using discrete I/O lines programmed properly with the software.

The 25XX080A/B contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The CS pin must be low and the HOLD pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after CS goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25XX080A/B in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

2.2 Read Sequence

The device is selected by pulling CS low. The 8-bit read instruction is transmitted to the 25XX080A/B followed by the 16-bit address, with the six MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (03FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the CS pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25XX080A/B, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting CS low and then clocking out the proper instruction into the 25XX080A/B. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without CS being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the CS low, issuing a WRITE instruction, followed by the 16-bit address, with the six MSBs of the address being don't care bits, and then the data to be written. Up to 16 bytes (25XX080A) or 32 bytes (25XX080B) of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the CS must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If CS is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the Status Register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.
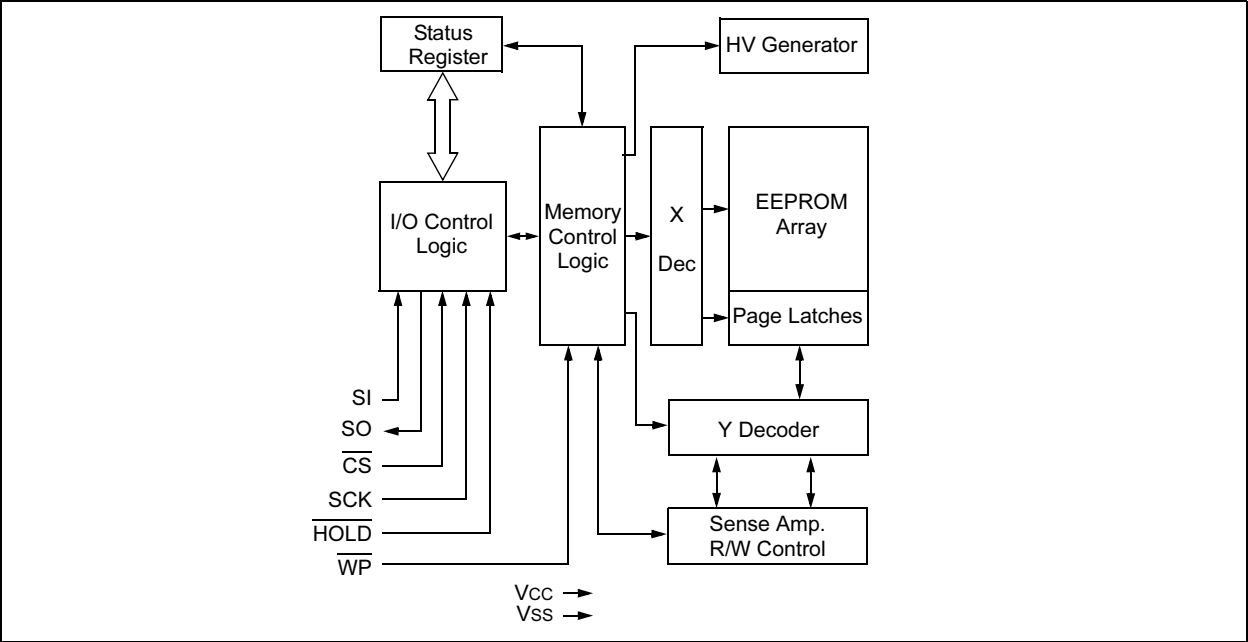
Block Diagram


TABLE 2-1:   INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register

FIGURE 2-1:   READ SEQUENCE
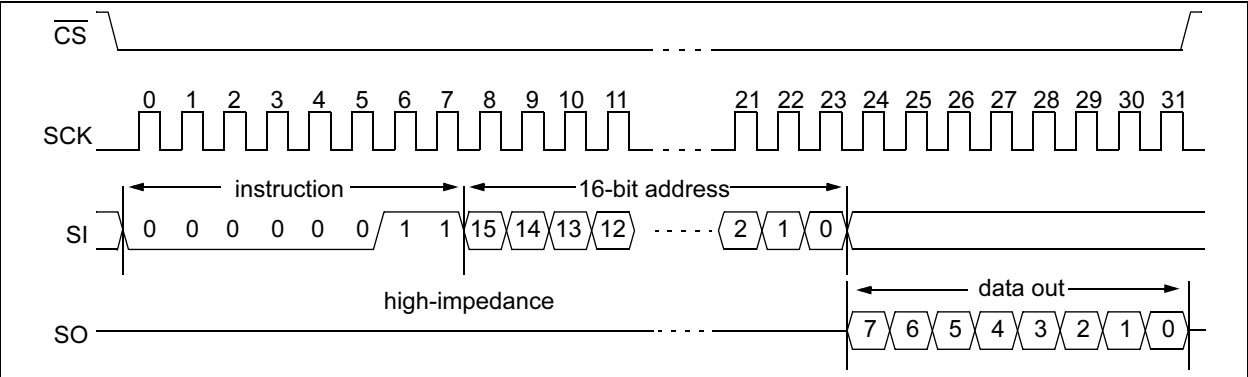
FIGURE 2-2: BYTE WRITE SEQUENCE
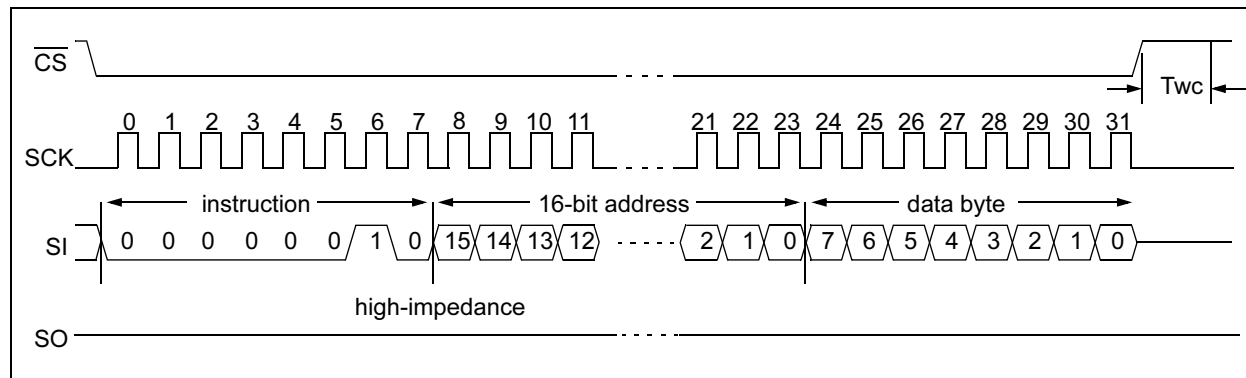
FIGURE 2-3: PAGE WRITE SEQUENCE
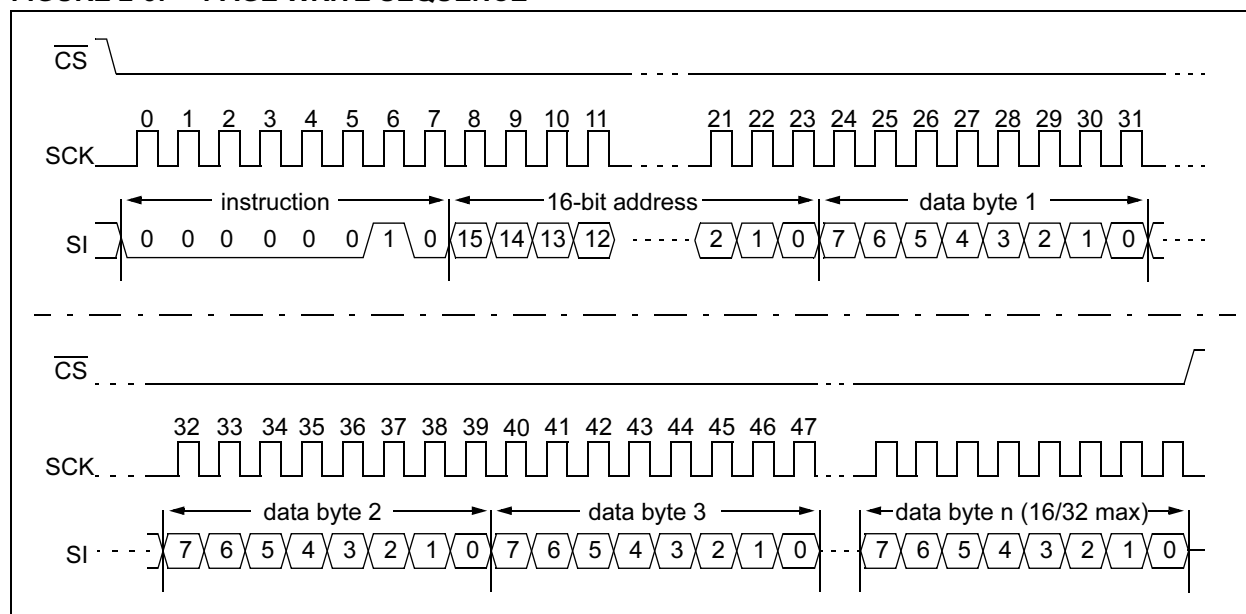
2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX080A/B contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.
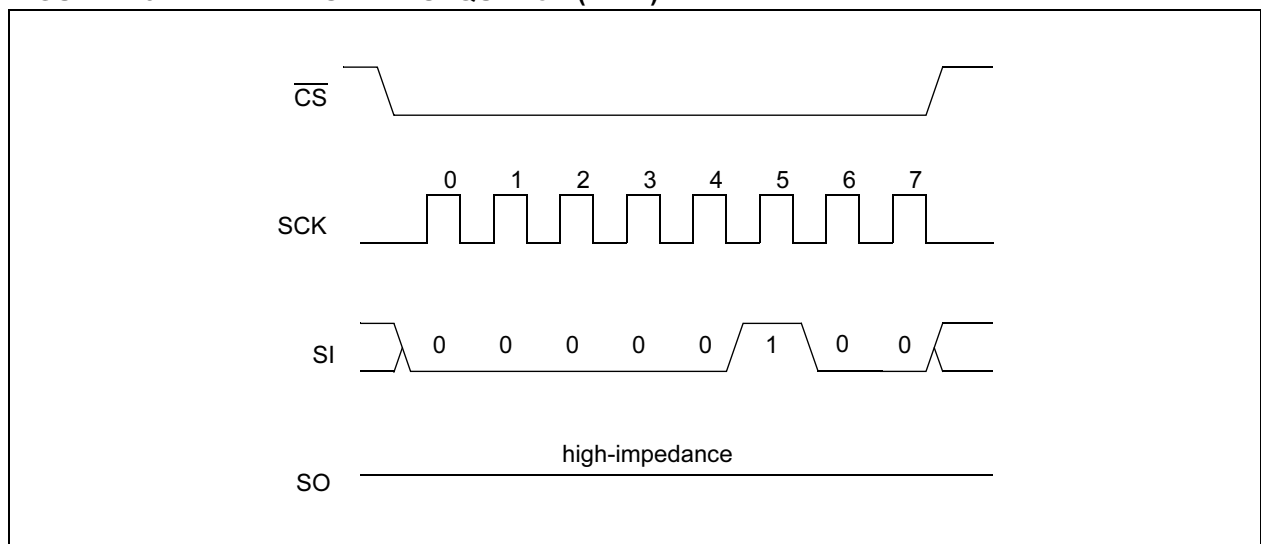
The following is a list of conditions under which the write enable latch will be reset:

• Power-up
• WRDI instruction successfully executed
• WRSR instruction successfully executed
• WRITE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)
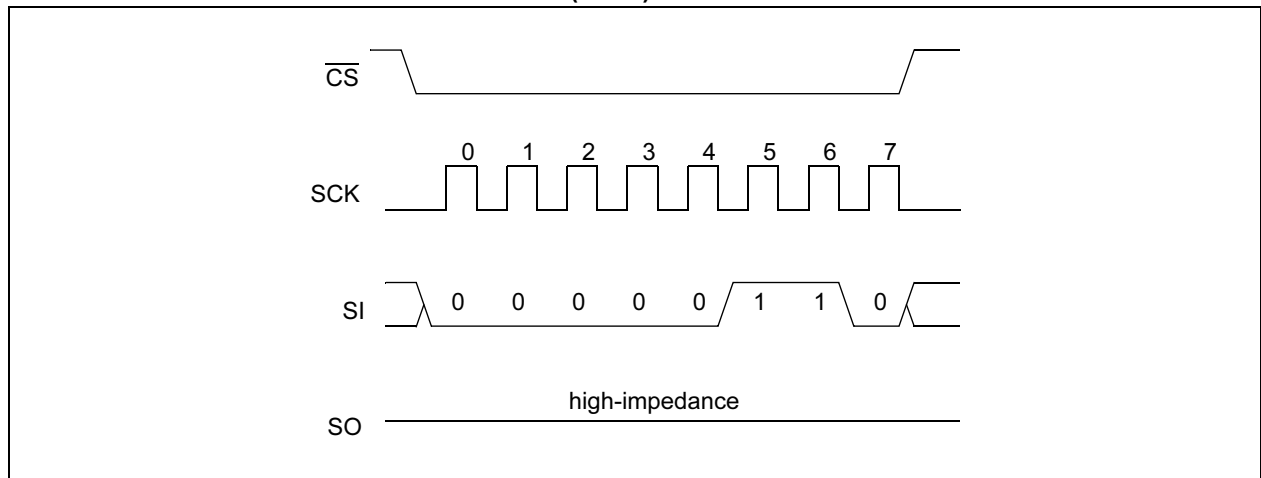
FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)

25XX080A/B

2.5 Read Status Register Instruction (`RDSR`)

The Read Status Register instruction (`RDSR`) provides access to the Status Register. The Status Register may be read at any time, even during a write cycle. The Status Register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	–	–	–	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

The **Write-In-Process (WIP)** bit indicates whether the 25XX080A/B is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read only. When set to a '1', the latch allows writes to the array or the Status Register, when set to a '0', the latch prohibits writes to the array or the Status Register. The state of this bit can always be updated via the `WREN` or `WRDI` commands regardless of the state of write protection on the Status Register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the `WRSR` instruction, which is in Figure 2-7. These bits are nonvolatile and are shown in Table 2-3.

See Figure 2-6 for the `RDSR` timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (`RDSR`)
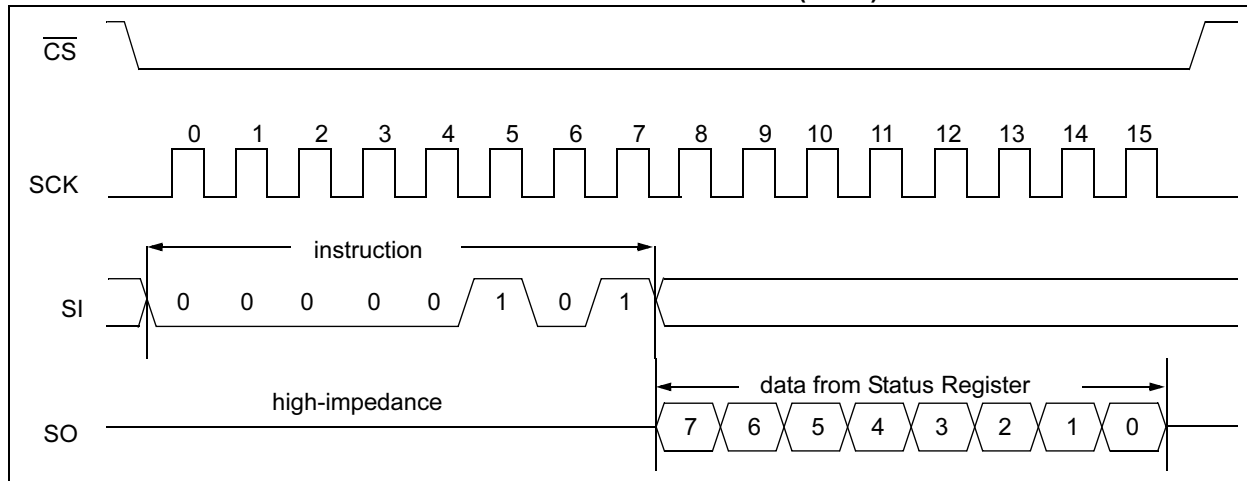
2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the Status Register as shown in Table 2-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the Status Register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 2-3.

The Write-Protect Enable (WPEN) bit is also a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the Status Register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the Status Register are disabled. See Table 2-4 for a matrix of functionality on the WPEN bit.

See Figure 2-7 for the WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (0300h - 03FFh)
1	0	upper 1/2 (0200h - 03FFh)
1	1	all (0000h - 03FFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)
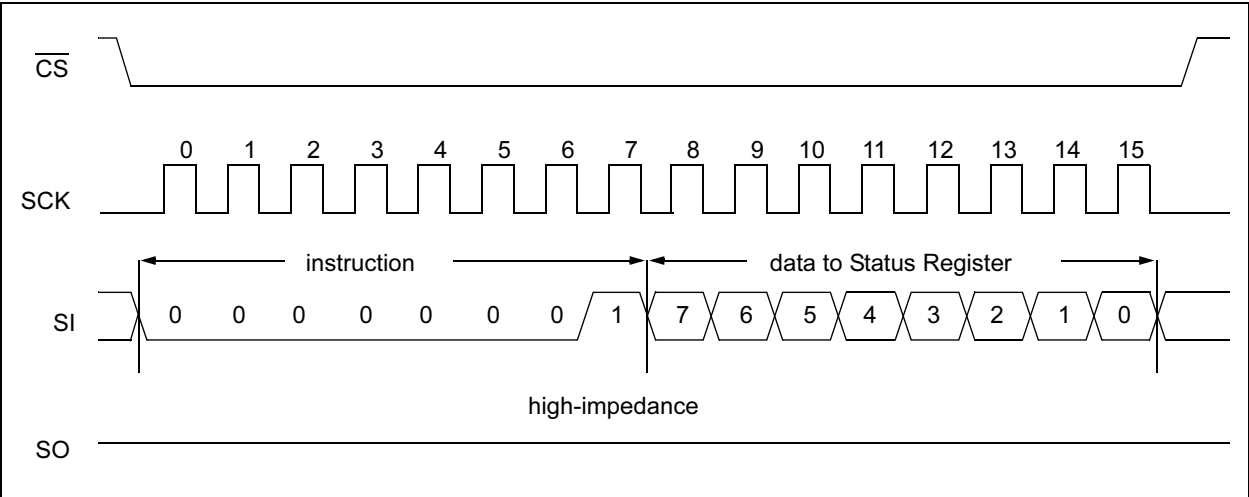
2.7   Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

• The write enable latch is reset on power-up
• A write enable instruction must be issued to set the write enable latch
• After a byte write, page write or Status Register write, the write enable latch is reset
• $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
• Access to the array during an internal write cycle is ignored and programming is continued

2.8   Power-On State

The 25XX080A/B powers on in the following state:

• The device is in low-power Standby mode ($\overline{CS}$ = 1)
• The write enable latch is reset
• SO is in high-impedance state
• A high-to-low-level transition on $\overline{CS}$ is required to enter active state

TABLE 2-4:   WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	Status Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

3.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1:   PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{WP}$	3	Write-Protect Pin
Vss	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
Vcc	8	Supply Voltage

3.1   Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2   Serial Output (SO)

The SO pin is used to transfer data out of the 25XX080A/B. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3   Write-Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the Status Register to prohibit writes to the nonvolatile bits in the Status Register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the Status Register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the nonvolatile bits in the Status Register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a Status Register write sequence will disable writing to the Status Register. If an internal write cycle has already begun, WP going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the Status Register is low. This allows the user to install the 25XX080A/B in a system with $\overline{WP}$ pin grounded and still be able to write to the Status Register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

3.4   Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5   Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX080A/B. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.6   Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25XX080A/B while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX080A/B must remain selected during this sequence. The SI, SCK and SO pins are in a high impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.
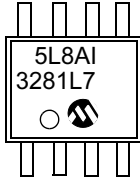
25XX080A/B

4.0 PACKAGING INFORMATION

4.1 Package Marking Information
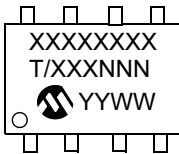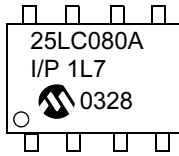
8-Lead MSOP (150 mil)

```
XXXXXXT
YWWNNN
 ○ (M)
```

Example:

```
5L8AI
3281L7
 ○ (M)
```
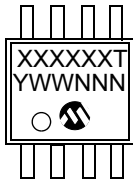
MSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
25AA080A	5A8A	G5A8A
25AA080B	5A8B	G5A8B
25LC080A	5L8A	G5L8A
25LC080B	5L8B	G5L8B

8-Lead PDIP

```
XXXXXXXX
T/XXXNNN
 ○ (M) YYWW
```

Example:

```
25LC080A
I/P 1L7
 ○ (M) 0328
```

8-Lead SOIC

```
XXXXXXXX
T/XXYYWW
 ○ (M) NNN
```

Example:

```
25LC080A
I/SN 0328
 ○ (M) 1L7
```

8-Lead TSSOP

```
 ○ XXXX
   TYWW
(M) NNN
```

Example:

```
 ○ 5L8A
   I328
(M) 1L7
```
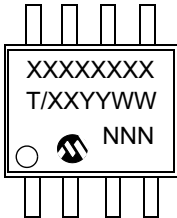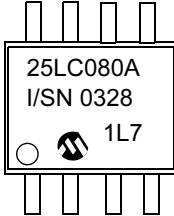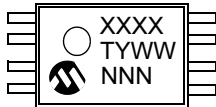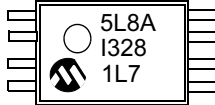
TSSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
25AA080A	5A8A	NA8A
25AA080B	5A8B	NA8B
25LC080A	5L8A	NL8A
25LC080B	5L8B	NL8B

Legend:
	XX...X	Part number
	T	Temperature (I, E)
	Blank	Commercial
	YY	Year code (last 2 digits of calendar year) except TSSOP and MSOP which use only the last 1 digit
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: Custom marking available.

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8-Lead Plastic Micro Small Outline Package (MS) (MSOP)
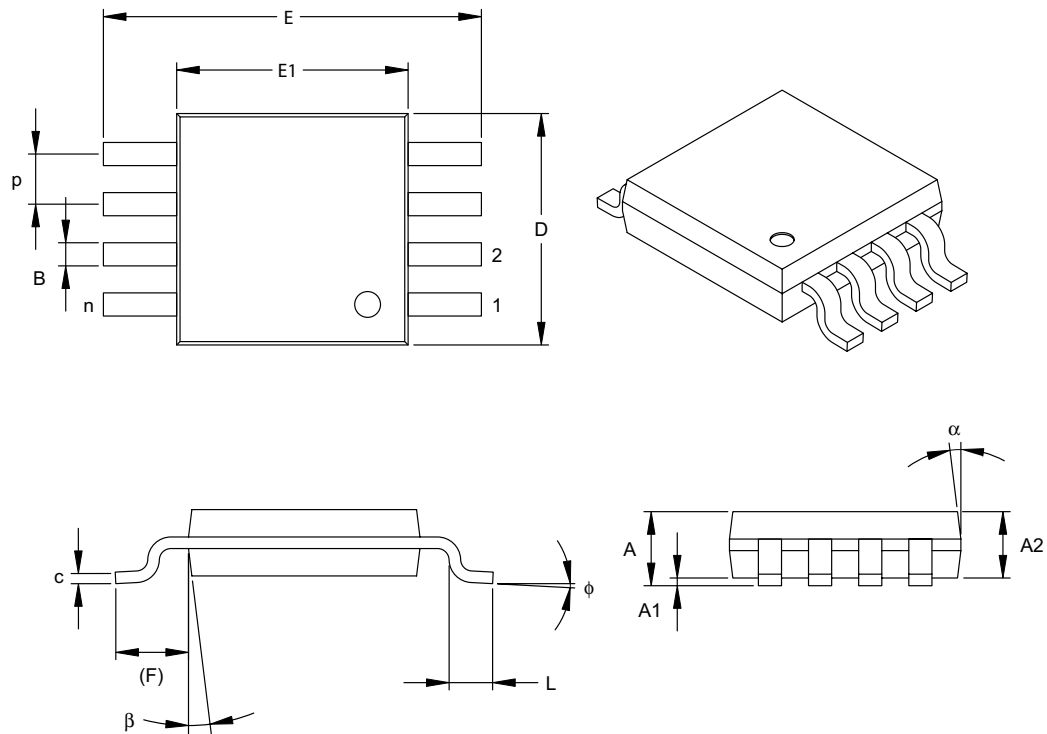
	Units		INCHES			MILLIMETERS*	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

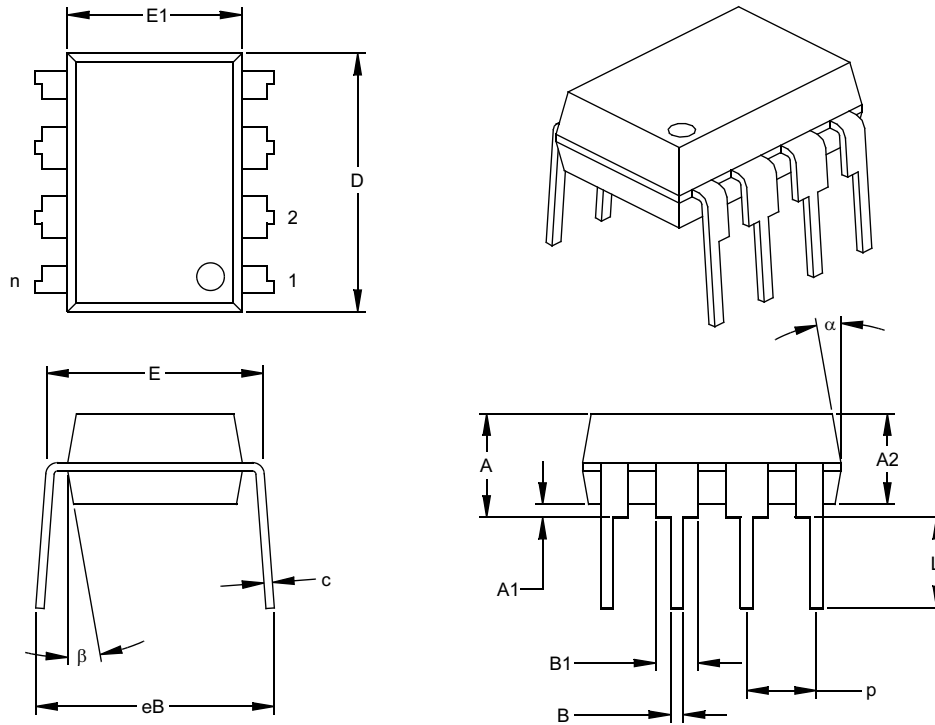*Controlling Parameter

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

25XX080A/B

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)
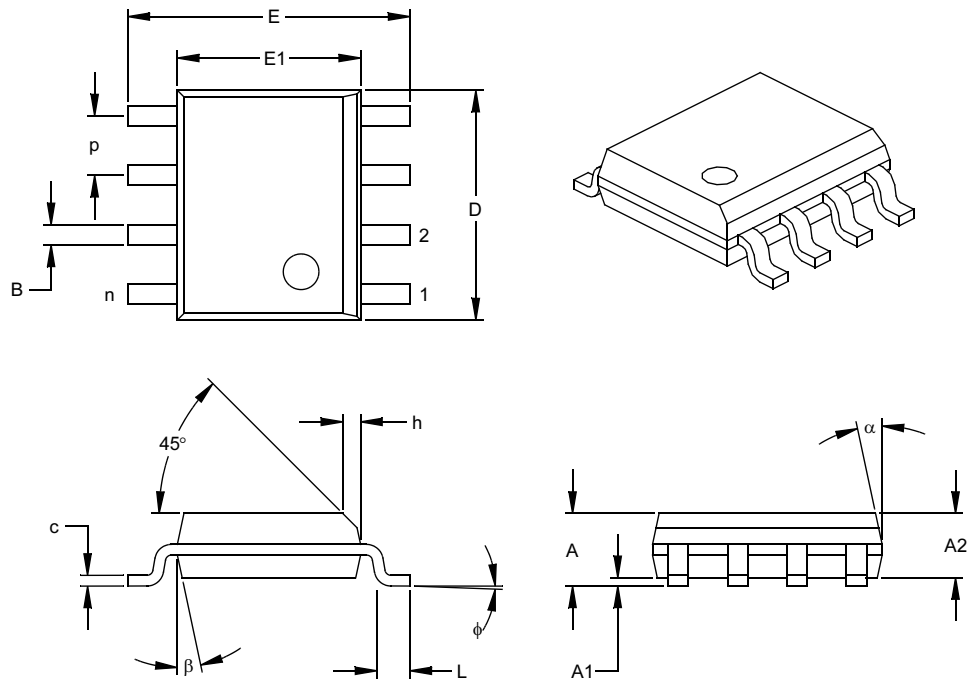
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

25XX080A/B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)
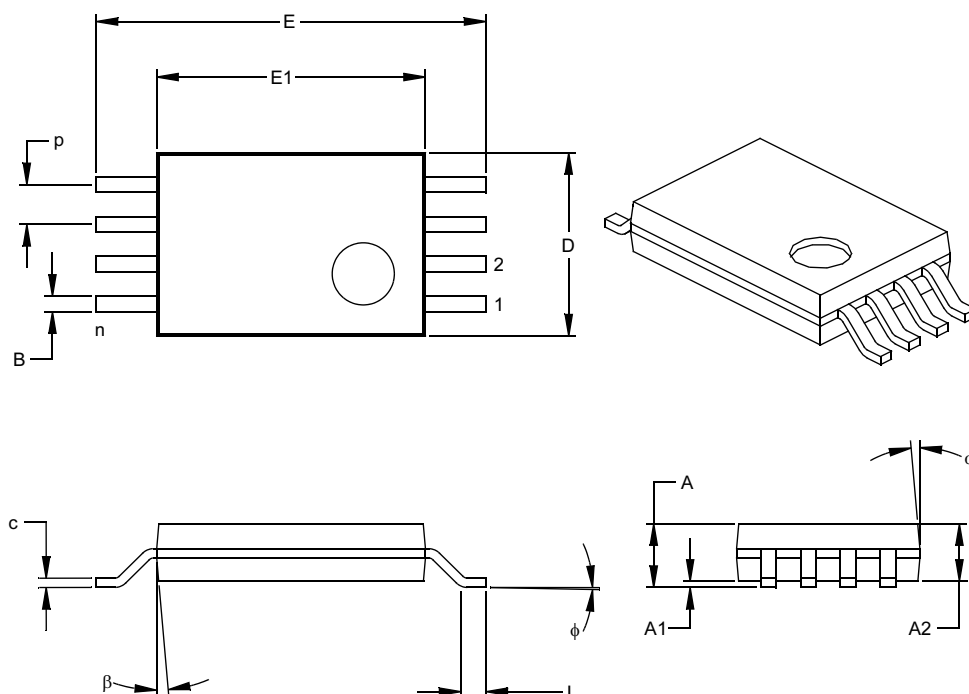
	Units		INCHES			MILLIMETERS*	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.005" (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

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042003

25AA080A/B, 25LC080A/B

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    _____
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    _____

7.   How would you improve this document?

    _____
    _____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	X	/XX	X
Device	Tape & Reel		Temp Range	Package	Lead Finish

Device	25AA080A		8 Kbit, 1.8V, 16 Byte Page SPI Serial EEPROM
	25AA080B		8 Kbit, 1.8V, 32 Byte Page SPI Serial EEPROM
	25LC080A		8 Kbit, 2.5V, 16 Byte Page SPI Serial EEPROM
	25LC080B		8 Kbit, 2.5V, 32 Byte Page SPI Serial EEPROM
Tape & Reel	Blank	=	Standard packaging
	T	=	Tape and Reel
Temperature Range	I	=	-40°C to+85°C
	E	=	-40°C to+125°C
Package	MS	=	Plastic MSOP (Micro Small Outline), 8-lead
	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil body), 8-lead
	ST	=	TSSOP, 8-lead
Lead Finish	Blank	=	Standard 63% / 37% Sn/Pb
	G	=	Matte Tin (Pure Sn)

Examples:

a) 25AA080A-I/MS = 8 Kbit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., MSOP package

b) 25AA080B-I/STG = 8 Kbit, 32-byte page, 1.8V Serial EEPROM, Industrial temp., TSSOP package, Pb-free

c) 25AA080AT-I/SN = 8 Kbit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

d) 25LC080A-I/MSG = 8 Kbit, 16-byte page, 2.5V Serial EEPROM, Industrial temp., MSOP package, Pb-free

e) 25LC080BT-I/SN = 8 Kbit, 32-byte page, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

f) 25LC080BT-I/ST = 8 Kbit, 32-byte page, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, TSSOP package

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