TOSHIBA

ATA/ATAPI, USB, I2C, SIO Controller

TOSHIBA GOKU-S

(TC86C001FG)

July 15, 2002

1. General Description

The GOKU-S, part number TC86C001FG, is a highly integrated, high-performance solution that integrates five popular and widely used interfaces: PCI Interface, ATA/ATAPI Host Controller, USB Host Controller, USB Device Controller, I2C Controller or Serial I/O Controller

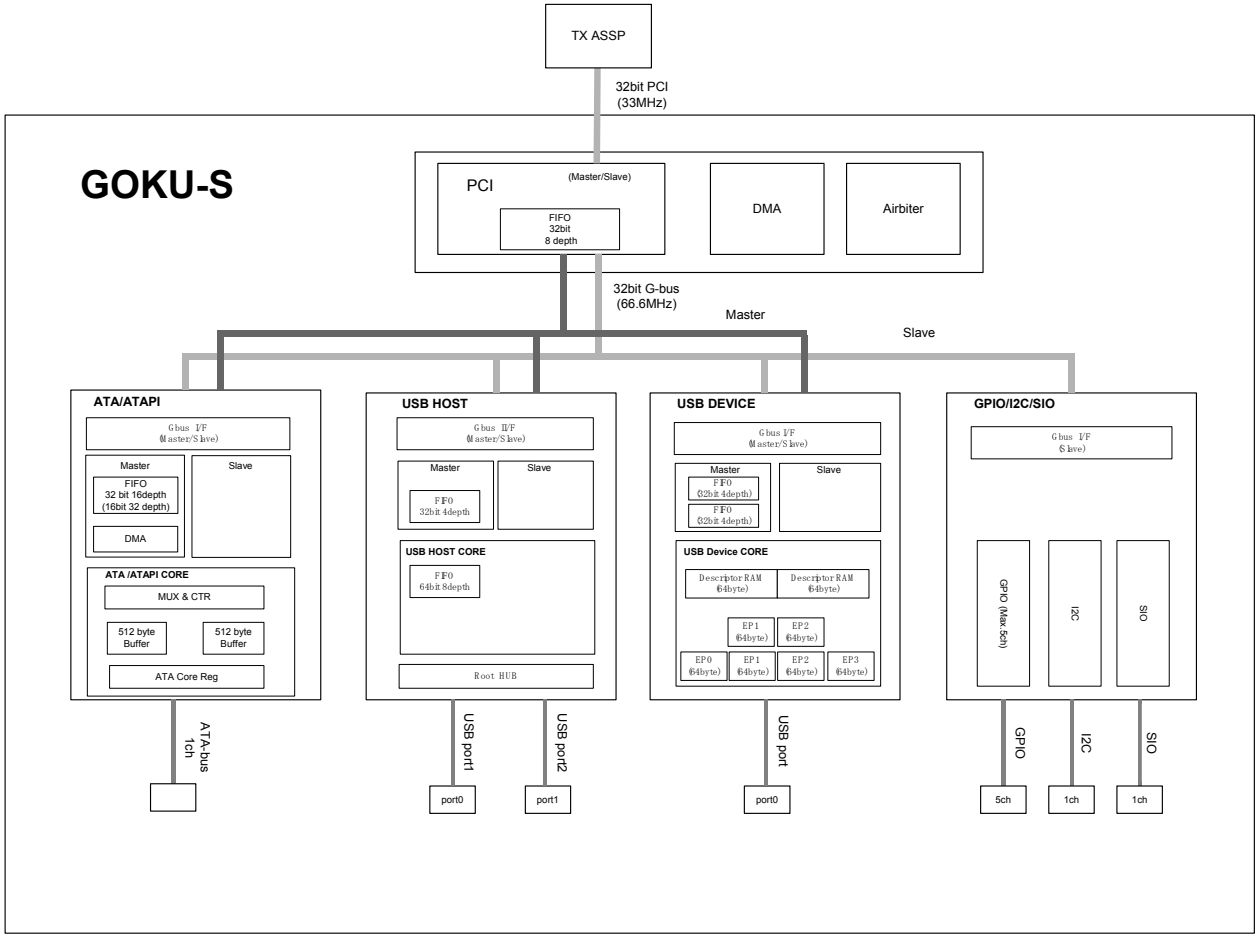
The GOKU-S provides the best solution for a wide range of digital products such as set-top boxes, personal video recorders, information appliances, multifunction printers and can be used as a companion chip to Toshiba's TX49 and TX39 System RISC family of processors.

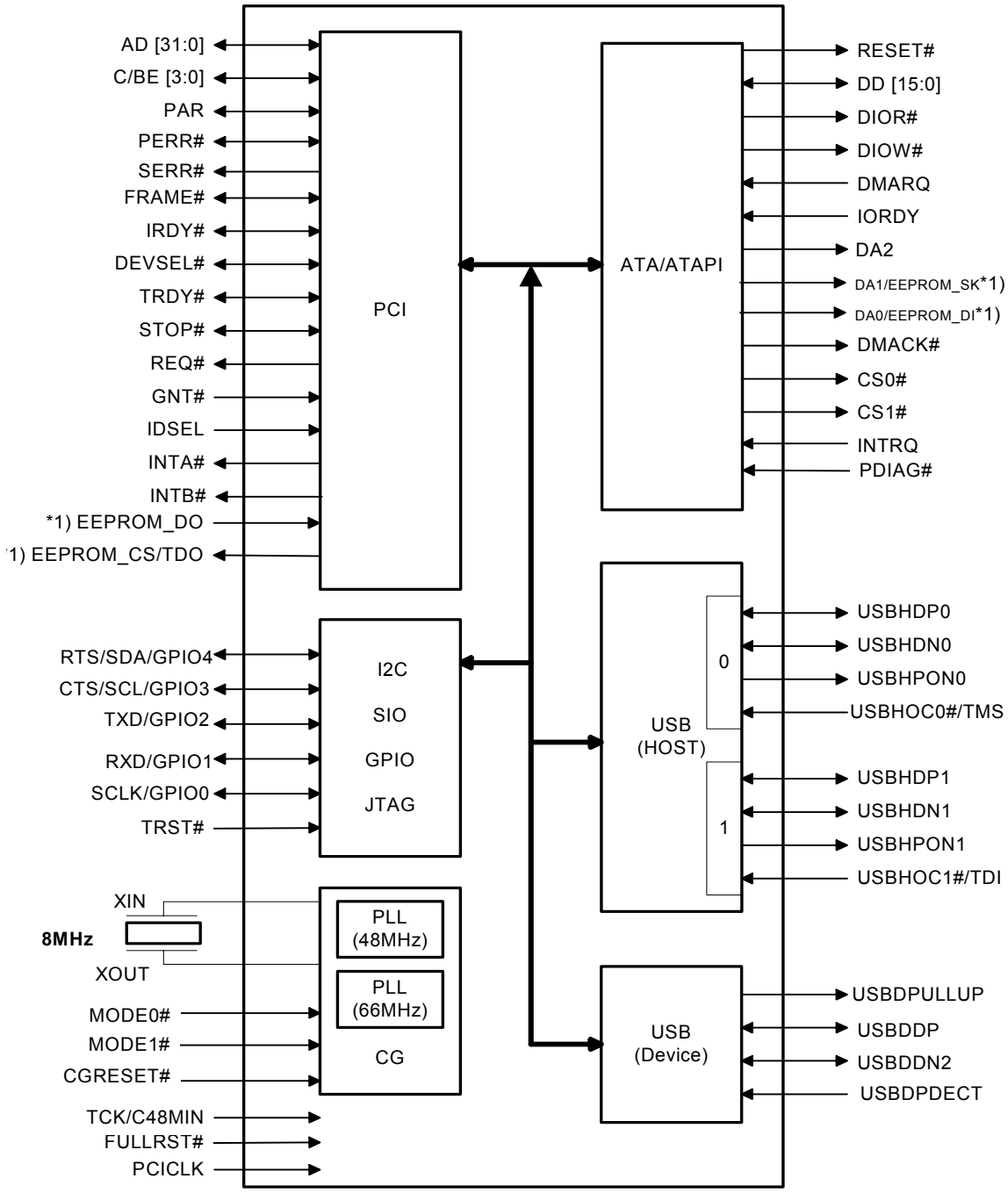
2. Outline and Features

GOKU-S is a multi-function PCI device that consists of ATA/ATAPI function, USB host function, USB device function, and I2C Bus / Serial I/O / general purpose I/O function.

- ATA/ATAPI Host Controller
  Single channel for up to two devices (Master/Slave)
  Ultra DMA mode4(ATA-5) (up to 66.67Mbyte/sec)
  Support Ultra DMA Mode 0,1,2,3,4
  PIO Mode 0 to 4, Multiword DMA Mode 0, 1 and 2
  Fully compliant with PCI IDE Controller Specification Rev1.0 (Native-PCI only)
  Fully compliant Programming Interface for Bus Master IDE Controller Rev1.0
  DMA controller with 512kbyte x 2 FIFOs
  ATAPI Overlap command not support
- USB Host Controller
  Fully compliant with Universal Serial Bus Specification Rev1.1
  Fully compliant with OpenHCI for USB Release 1.0a
  2 ports for serial transfers at 12 Mbit/Sec (Full Speed) or 1.5 Mbit/Sec (Low Speed)
  Over current protection and Power control for each port
- USB Device Controller
  Fully compliant with Universal Serial Bus Specification Rev1.1
  1 port for serial transfers at 12 Mbit/Sec (Full Speed) only.
  Supports three types of transfer, Control transfer, Bulk transfer, and Interrupt transfer
  Supports one control endpoint (EP0), three endpoint (EP1, EP2, EP3) for selectable Bulk/Interrupt transfer
  EP0 : Control transfer (64byte FIFO)
  EP1,2 : Bulk/Interrupt transfer(Receive/Transmit selectable,64byte+64byte FIFOs)
  EP3 : Bulk/Interrupt transfer (64byte FIFO)
  Isochroous transfers not support
- I2C, Serial I/O and GPIO Controller (Multiplexed I2C, Serial I/O, GPIO)
  I2C (Single Master / Slave) 1ch
  Serial I/O (Full duplex UART) 1ch
  GPIO 5pin(Max)
  Independent selection of direction of pins and output port type (totem-pole or open-drain output) on a per bit basis.
- PCI Interface
  32-bit PCI bus interface at 33MHz PCI operation., 3.3V Interface
  Fully compliant with PCI Local Bus Specification Rev. 2.2
  Fully compliant with PCI Bus Power Management interface Specification Rev. 1.1
  Loadable PCI Configuration Space with EEPROM Interface
  Supports 2 Interrupts function (INTA and INTB)
  PCI Arbiter with Round-robin priority arbitration for the internal PCI devices

3. Structure


TX ASSP
32bit PCI
(33MHz)
GOKU-S
PCI
(Master/Slave)
FIFO
32bit
8 depth
DMA
Airbiter
32bit G-bus
(66.6MHz)
Master
Slave
ATA/ATAPI
Gbus I/F
(Master/Slave)
Master
Slave
FIFO
32 bit 16depth
(16bit 32 depth)
DMA
ATA /ATAPI CORE
MUX & CTR
512 byte
Buffer
512 byte
Buffer
ATA Core Reg
ATA-bus
1ch
USB HOST
Gbus I/F
(Master/Slave)
Master
Slave
FIFO
32bit 4depth
USB HOST CORE
FIFO
64bit 8depth
Root HUB
USB port1
USB port2
port0
port1
USB DEVICE
Gbus I/F
(Master/Slave)
Master
Slave
FIFO
(32bit 4depth)
FIFO
(32bit 4depth)
USB Device CORE
Descriptor RAM
(64byte)
Descriptor RAM
(64byte)
EP1
(64byte)
EP2
(64byte)
EP0
(64byte)
EP1
(64byte)
EP2
(64byte)
EP3
(64byte)
USB port
port0
GPIO/I2C/SIO
Gbus I/F
Slave
GPIO (Max.5ch)
I2C
SIO
GPIO
I2C
SIO
5ch
1ch
1ch



*1) EEPROM interface Signals (PCI INTERFACE)

4. Pins

4.1 PCI INTERFACE

SIGNAL NAME	I/O	DESCRIPTION
PCICLK	I	PCI CLOCK (33 MHz) PCI bus clock signals.
AD [31:0]	IO	PCI ADDRESS/DATA Multiplexed address and data bus.
C/BE [3:0]	IO	BUS COMMAND AND BYTE ENABLES Command and byte enable signals.
PAR	IO	CALCULATED PARITY SIGNAL
PERR#	IO	PARITY ERROR
SERR#	O	SYSTEM ERROR
FRAME#	IO	CYCLE FRAME
IRDY#	IO	INITIATOR READY
DEVSEL#	IO	DEVICE SELECT
TRDY#	IO	TARGET READY
STOP#	IO	STOP
REQ#	O	BUS REQUEST
GNT#	I	BUS GRANT
IDSEL	I	INITIALIZATION DEVICE SELECT
INTA#	O	INTERRUPT A
INTB#	O	INTERRUPT B
EEPROM_DO	I	EEPROM Data from the EEPROM to the core
EEPROM_CS	O	EEPROM Chip Select

4.2 ATA/ATAPI INTERFACE (Multiplexed with Serial EEPROM INTERFACE)

SIGNAL NAME	I/O	DESCRIPTION
RESET#	O	RESET
DD [15:0]	IO	DATA
DIOR#	O	IO READ
DIOW#	O	IO WRITE
DMARQ	I	DMA REQUEST
IORDY	I	IO CHANNEL READY
DA2	O	ADDRESS2
DA1 / EEPROM_SK	O	ADDRESS1 / EEPROM_CLOCK
DA0 / EEPROM_DI	O	ADDRESS0 / EEPROM Data to the EEPROM from the core
DMACK#	O	DMA ACKNOWLEDGE
CS0#	O	CHIP SELECT
CS1#	O	CHIP SELECT
INTRQ	I	INTERRUPT REQUEST
PDIAG#	I	PASS DIAGNOSTIC

4.3 USB (Host) INTERFACE

SIGNAL NAME	I/O	DESCRIPTION
USBHDP0	IO	USB HOST PORT 0 DATA +
USBHDN0	IO	USB HOST PORT 0 DATA -
USBHPON0	O	POWER ON CONTROL (PORT 0)
USBHOC0#	I	OVER CURRENT DETECT (PORT 0)
USBHDP1	IO	USB HOST PORT 1 DATA +
USBHDN1	IO	USB HOST PORT 1 DATA -
USBHPON1	O	POWER ON CONTROL (PORT 1)
USBHOC1#	I	OVER CURRENT DETECT (PORT 1)

4.4 USB (Device) INTERFACE

SIGNAL NAME	I/O	DESCRIPTION
USBDDP	IO	USB DEVICE PORT DATA +
USBDDN	IO	USB DEVICE PORT DATA -
USBDPULLUP	O	USB DEVICE PULL UP
USBDPDECT	I	USB DEVICE POWER DETECT

4.5 I2C/SIO/GPIO INTERFACE

SIGNAL NAME	I/O	DESCRIPTION
GPIO4 (Mode0, 2) / SDA (Mode1, 3, 4) / RTS (Mode5, 6)	IO IO O	GENERAL PURPOSE INPUT/OUTPUT / SERIAL DATA LINE / SIO REQUEST TO SEND
GPIO3 (Mode0, 2) / SCL (Mode1, 3, 4) / CTS (Mode5, 6)	IO IO I	GENERAL PURPOSE INPUT/OUTPUT / SERIAL CLOCK LINE / SIO CLEAR TO SEND
GPIO2 (Mode0, 1) / TXD (Mode 2-6)	IO O	GENERAL PURPOSE INPUT/OUTPUT / SIO TRANSMIT DATA
GPIO1 (Mode0, 1) / RXD (Mode 2-6)	IO I	GENERAL PURPOSE INPUT/OUTPUT / SIO RECEIVE DATA
GPIO0 (Mode0-3,5) / SCLK (Mode 4,6)	IO I	GENERAL PURPOSE INPUT/OUTPUT / EXTERNAL SERIAL CLOCK

4.6 JTAG INTERFACE (Multiplexed with other signals)

SIGNAL NAME	I/O	DESCRIPTION
TRST#	I	TEST RESET INPUT
TDO	O	JTAG DATA OUTPUT
TDI	I	JTAG DATA INPUT
TMS	I	JTAG COMMAND
TCK / C48MIN (For test use)	I	JTAG CLOCK INPUT / USB internal CLK 48MHz (For test use)

4.7 CLOCK

SIGNAL NAME	I/O	DESCRIPTION
XIN	I	Crystal Input (8 MHz)
XOUT	O	Crystal Output (8 MHz)
CGRESET#	I	CG RESET

4.8 RESET

SIGNAL NAME	I/O	DESCRIPTION
FULLRST#	I	FULL RESET

4.9 TEST

SIGNAL NAME	I/O	DESCRIPTION
MODE0#	I	MODE SELECT Normal Mode :Set this pin to “High” JTAG Mode :Set this pin to “Low”
MODE1#	I	MODE SELECT Normal Mode :Set this pin to “High” JTAG Mode :Set this pin to “Low”

4.10 POWER/GROUND

SIGNAL NAME	I/O	DESCRIPTION
V_{CCINT}	I	VDD VOLTAGE PINS FOR INTERNAL CORE (1.5V)
V_{CCIO}	I	VDD VOLTAGE PINS FOR I/O SIGNALS (3.3V)
V_{SS}	I	GROUND PINS
PLL1VDD_A	I	VDD VOLTAGE PIN FOR PLL1
PLL1VSS_A	I	GROUND PIN FOR PLL1
PLL2VDD_A	I	VDD VOLTAGE Pin FOR PLL2
PLL2VSS_A	I	GROUND PIN FOR PLL2

5. Electrical Characteristics

5.1 ABSOLUTE MAXIMUM RATING (*1)

Table 5.1.1 Absolute Maxumum Rating

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage (for I/O)	$V_{CCIOMax}$	–0.3 to 3.9	V
Supply voltage (for internal)	$V_{CCINTMax}$	–0.3 to 3.0	V
Input voltage (*2)	V_{IN}	–0.3 to VccIO + 0.3V	V
Storage Temperature	T_{STG}	–40 to +125	°C
Power	P_D	T.B.D.	W

Note) (*1) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended condition. If these conditions are exceeded, reliability of LSI may be adversely affected.

(*2) The maximum rated $V_{ddIOMax}$ voltage must not be exceeded even at V_{ddIO} + 0.3 volts.

5.2 RECOMMENDED OPERATING CONDITIONS (*3)

Table 5.2.1 Recommemded Operating Conditions

PARAMETER		SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply Voltage	I/O	V_{CCIO}		3.1	3.5	V
	Internal	V_{CCINT}		1.4	1.6	V
Operating Temperature		Ta		0	85	°C

(*3) Functional operation should be restricted to the recommended operating conditions. Those are the limits under which proper device operation is guaranteed. Therefore, the end product must be designed within the recommended voltage and temperature ranges indicated.

6. Package and Pin Assignment

6.1 Pin Assignment

Figure 6.1.1 Pin Designations of GOKU-S(TC86C001FG)

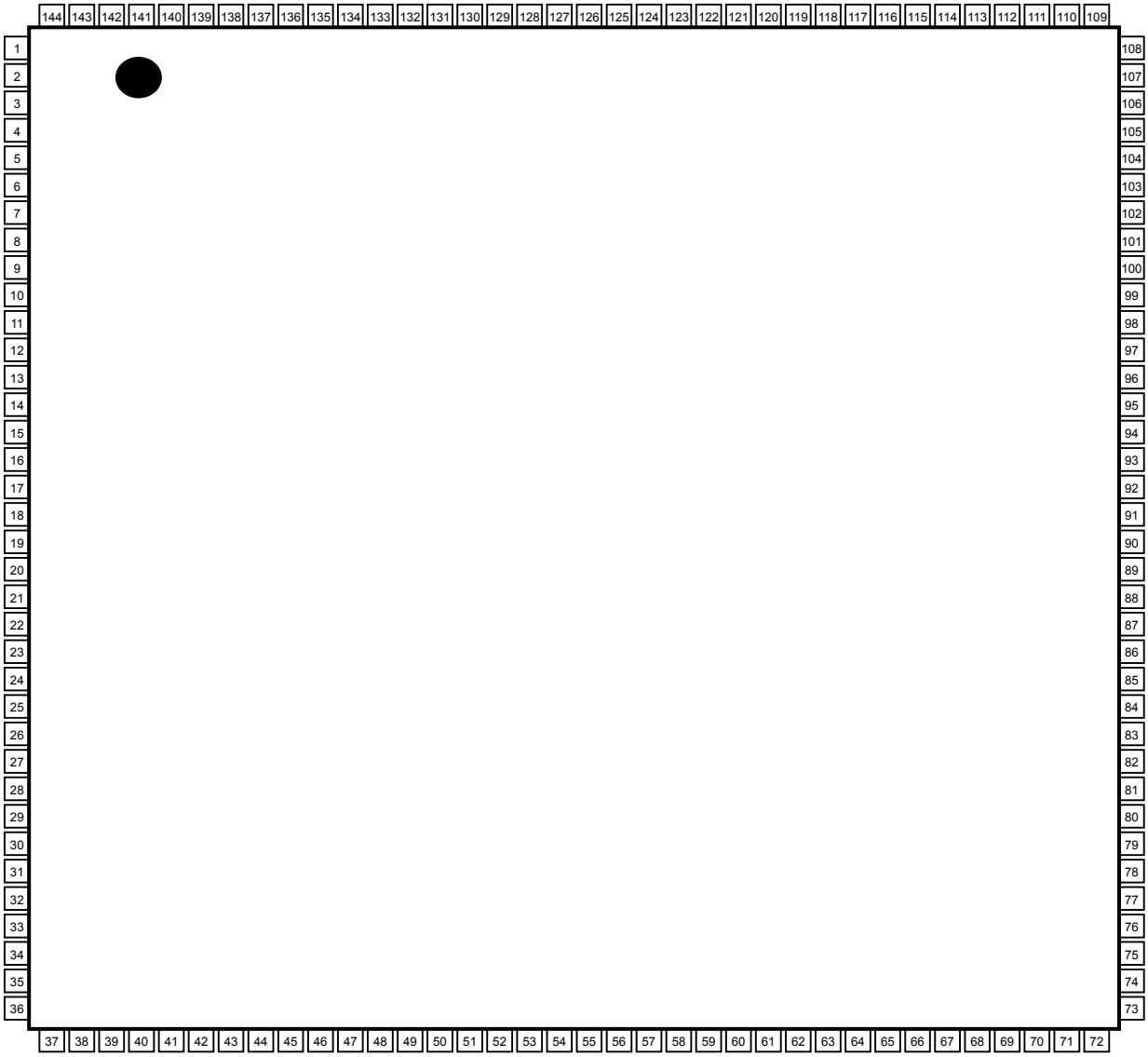
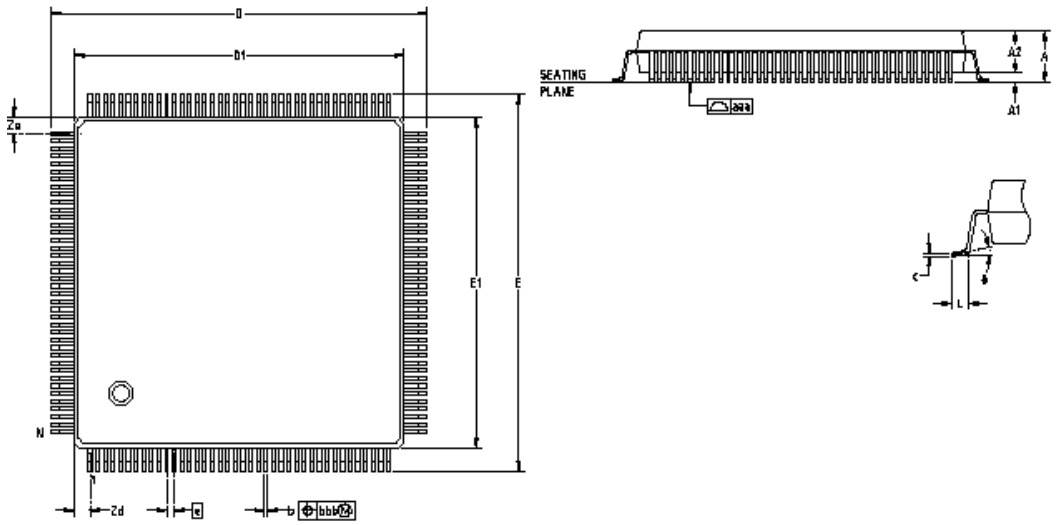


Table 6.1.1 Pin Designations (LQFP144)

PIN No.	PIN FUNCTION	PIN No.	PIN FUNCTION	PIN No.	PIN FUNCTION	PIN No.	PIN FUNCTION
1	V_{CCIO}	37	AD9	73	SCLK/GPIO0	109	DD02
2	AD24	38	AD8	74	V_{CCIO}	110	DD12
3	C/BE3	39	V_{CCIO}	75	TRST#	111	DD03
4	IDSEL	40	V_{SS}	76	MODE1#	112	V_{SS}
5	AD23	41	C/BE0	77	V_{SS}	113	DD11
6	AD22	42	AD7	78	FULLRST#	114	DD04
7	AD21	43	AD6	79	V_{CCINT}	115	DD10
8	V_{SS}	44	AD5	80	MODE0#	116	DD05
9	AD20	45	AD4	81	CGRESET#	117	DD09
10	AD19	46	AD3	82	V_{SS}	118	DD06
11	AD18	47	V_{SS}	83	USBHDP1	119	DD08
12	AD17	48	AD2	84	USBHDN1	120	DD07
13	AD16	49	AD1	85	V_{CCIO}	121	RESET#
14	C/BE2	50	AD0	86	EEPROM_CS/TDO	122	V_{CCIO}
15	V_{SS}	51	V_{CCIO}	87	EEPROM_DO	123	USBDDP
16	FRAME#	52	USBHDP0	88	CS1#	124	USBDDN
17	IRDY#	53	USBHDN0	89	CS0#	125	USBDPULLUP
18	V_{CCINT}	54	V_{SS}	90	V_{CCIO}	126	USBDPDECT
19	V_{CCIO}	55	USBHPON0	91	DA2	127	V_{SS}
20	TRDY#	56	USBHOC0#/TMS	92	DA0/EEPROM_DI	128	INTA#
21	DEVSEL#	57	USBHPON1	93	V_{SS}	129	INTB#
22	V_{SS}	58	USBHOC1#/TDI	94	PDIAG#	130	V_{CCINT}
23	STOP#	59	V_{CCIO}	95	DA1/EEPROM_SK	131	PCICLK
24	V_{SS}	60	TCK	96	INTRQ	132	V_{SS}
25	PERR#	61	V_{CCINT}	97	DMACK#	133	GNT#
26	SERR#	62	XIN	98	IORDY	134	REQ#
27	PAR	63	XOUT	99	DIOR#	135	AD31
28	C/BE1	64	V_{SS}	100	DIOW#	136	V_{SS}
29	V_{CCIO}	65	PLL1VSS_A	101	DMARQ	137	AD30
30	AD15	66	PLL1VDD_A	102	V_{SS}	138	AD29
31	AD14	67	PLL2VDD_A	103	DD15	139	AD28
32	V_{SS}	68	PLL2VSS_A	104	DD00	140	V_{CCIO}
33	AD13	69	RTS/SDA/GPIO4	105	DD14	141	AD27
34	AD12	70	CTS/SCL/GPIO3	106	DD01	142	AD26
35	AD11	71	TXD/GPIO2	107	DD13	143	AD25
36	AD10	72	RXD/GPIO1	108	V_{CCIO}	144	V_{SS}

6.2 Packege Dimensions

144 Lead LQFP (LQFP144-P-2020-0.50A)



Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	-	-	1.85	e	0.5 BSC		
A1	0.00	0.10	0.25	L	0.3	-	0.7
A2	1.2	1.4	1.6	Zd	1.25 TYP		
B	0.18	0.22	0.27	Ze	1.25 TYP		
C	0.100	0.145	0.200	Θ	0°	-	10°
D	21.8	22.0	22.2	aaa	0.10		
D1	19.8	20.0	20.2	bbb	0.10		
E	21.8	22.0	22.2	N	144		
E1	19.8	20.0	20.2				

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