

FDW2520C

Complementary PowerTrench® MOSFET

General Description

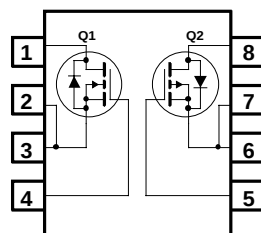
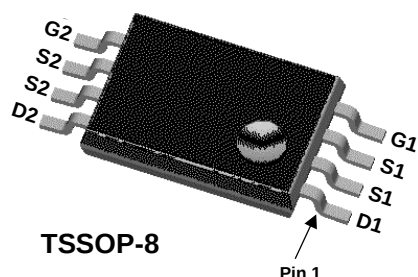
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC/DC conversion
- Power management
- Load switch

Features

- **Q1: N-Channel**
6 A, 20 V. $R_{DS(ON)} = 18\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 28\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- **Q2: P-Channel**
-4.4A, 20 V. $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 57\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DSS}	Drain-Source Voltage	20	−20	V
V _{GSS}	Gate-Source Voltage	±12	±12	V
I _D	Drain Current - Continuous (Note 1a)	6	−4.4	A
	- Pulsed	30	−30	
P _D	Power Dissipation (Note 1a)	1.0		W
	(Note 1b)	0.6		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	125	$^\circ\text{C/W}$
	(Note 1b)	208	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2520C	FDW2520C	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	Q1 Q2		14 -17		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	Q1 Q2	0.4 -0.4	1.0 -1.0	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	Q1 Q2		-3.3 3.1		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	Q1		14	18	$\text{m}\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 5\text{ A}$			19	28	
		$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}, T_J = 125^\circ\text{C}$			19	29	
		$V_{GS} = -4.5\text{ V}, I_D = -4.4\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -3.3\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -4.4\text{ A}, T_J = 125^\circ\text{C}$	Q2		28 43 39	35 57 56	$\text{m}\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	Q1 Q2	30 -30			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 6\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -4.4\text{ A}$	Q1 Q2		30 17		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ Q2:	Q1		1325		pF
			Q2		1330		pF
C_{oss}	Output Capacitance		Q1		358		pF
			Q2		552		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	Q1 Q2		168 153		pF
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$ Q2: $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1		6	20	ns
			Q2		12	25	
t_r	Turn-On Rise Time		Q1		11	40	ns
			Q2		19	40	
$t_{d(off)}$	Turn-Off Delay Time		Q1		32	60	ns
			Q2		60	100	
t_f	Turn-Off Fall Time		Q1 Q2		19 37	34 70	ns
Q_g	Total Gate Charge	Q1: $V_{DS} = 10\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 4.5\text{ V}$ Q2: $V_{DS} = -5\text{ V}, I_D = -4.4\text{ A},$ $V_{GS} = -4.5\text{ V}$	Q1		14	20	nC
			Q2		14	20	
Q_{gs}	Gate-Source Charge		Q1 Q2		2.6 3.0		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		3.7 3.9		nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1			0.83	A
			Q2			-0.83	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.83\text{ A}$ (Note 2)	Q1		0.5	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -0.83\text{ A}$ (Note 2)	Q2		-0.7	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
- b) $R_{\theta JA}$ is 208°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics: Q1

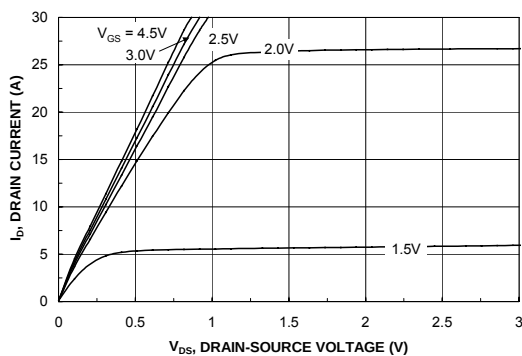


Figure 1. On-Region Characteristics.

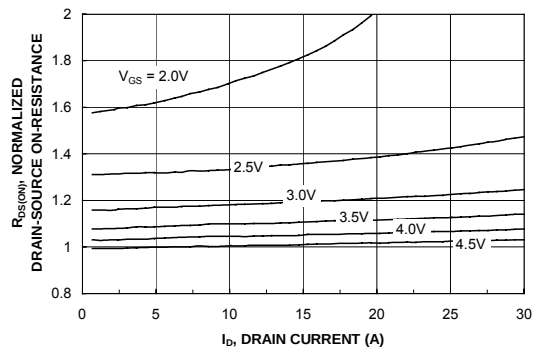


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

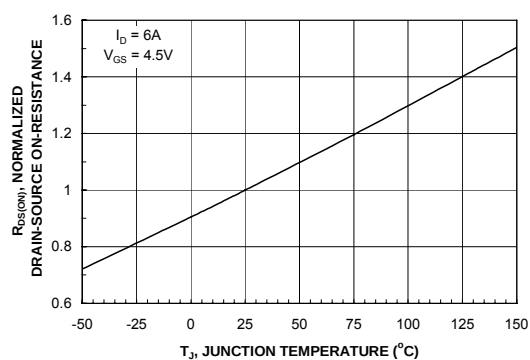


Figure 3. On-Resistance Variation with Temperature.

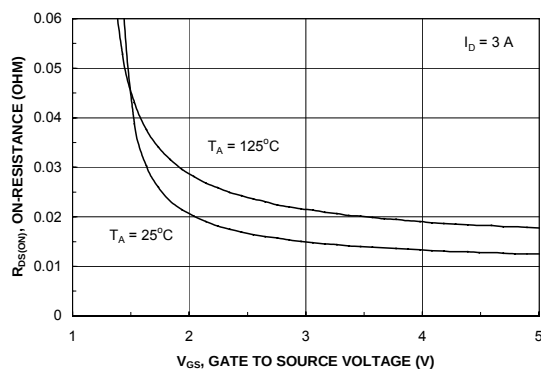


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

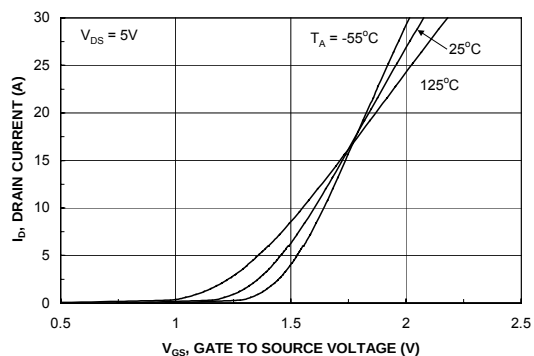


Figure 5. Transfer Characteristics.

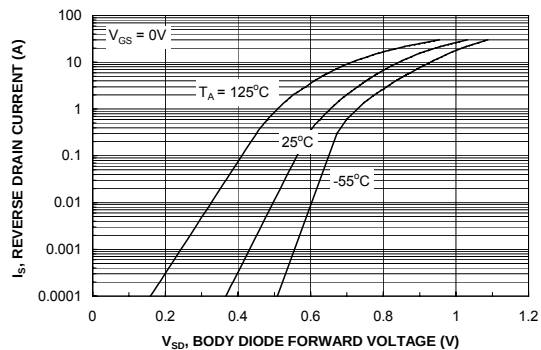


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

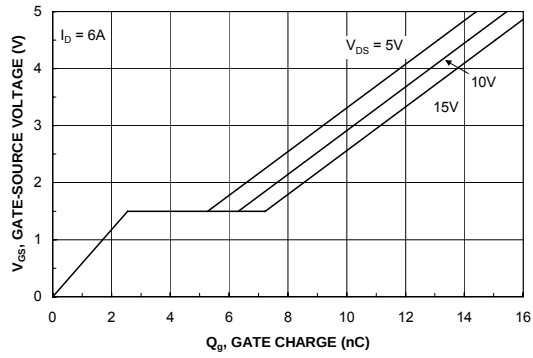


Figure 7. Gate Charge Characteristics.

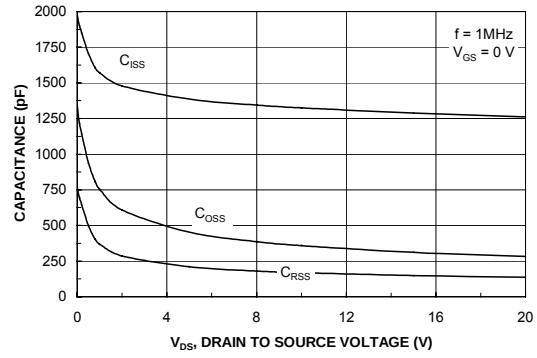


Figure 8. Capacitance Characteristics.

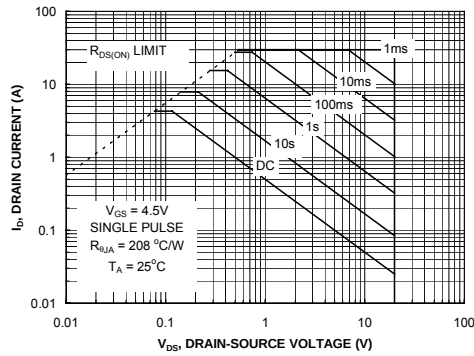


Figure 9. Maximum Safe Operating Area.

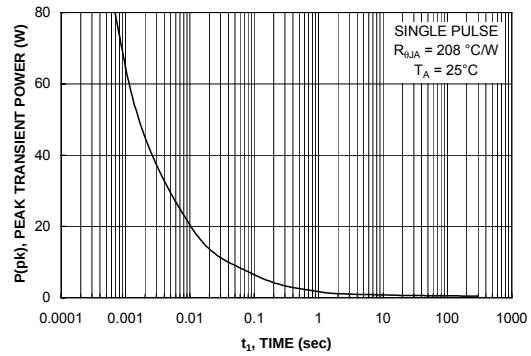


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q2

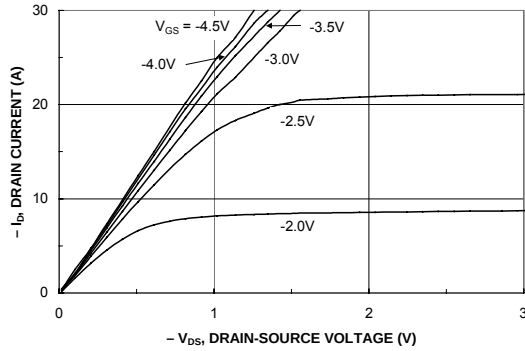


Figure 11. On-Region Characteristics.

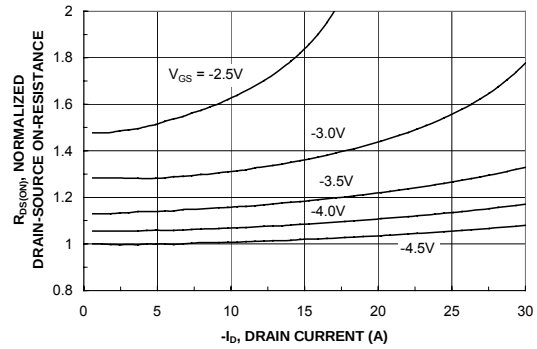


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

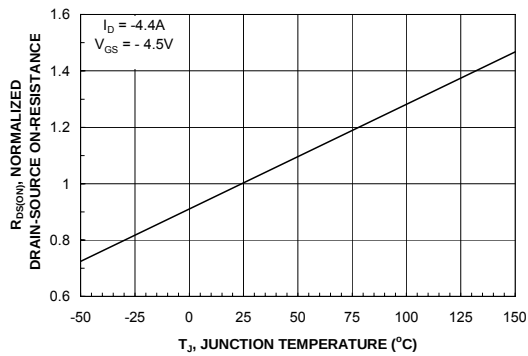


Figure 13. On-Resistance Variation with Temperature.

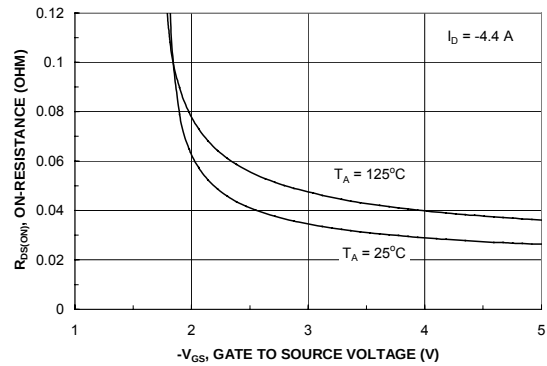


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

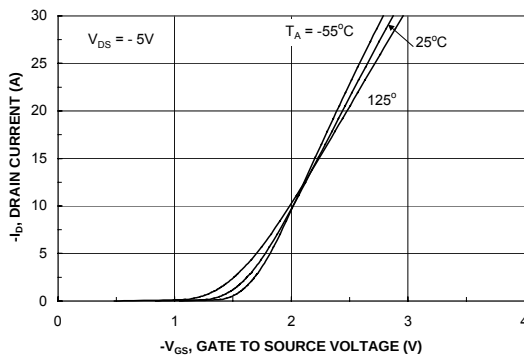


Figure 15. Transfer Characteristics.

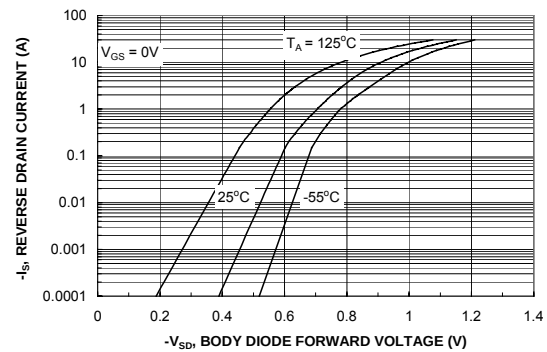


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

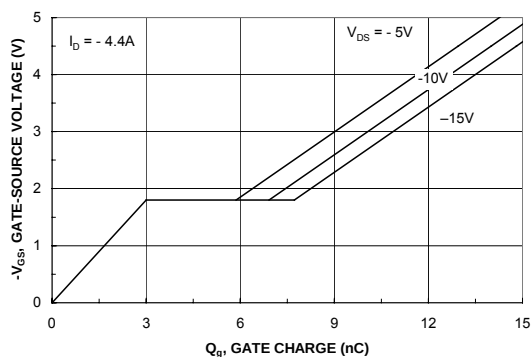


Figure 17. Gate Charge Characteristics.

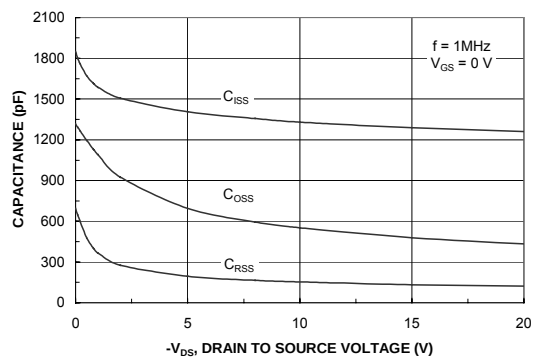


Figure 18. Capacitance Characteristics.

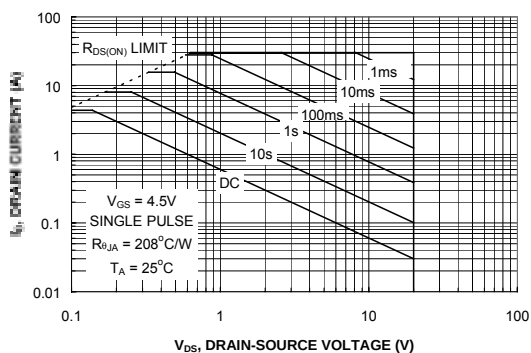


Figure 19. Maximum Safe Operating Area.

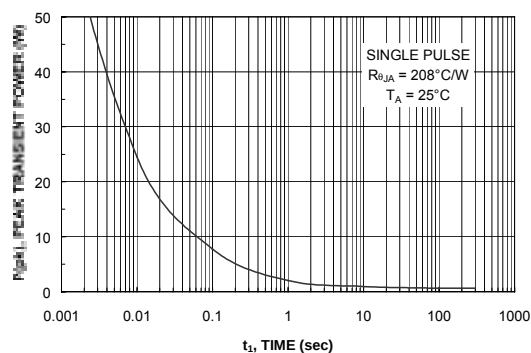


Figure 20. Single Pulse Maximum Power Dissipation.

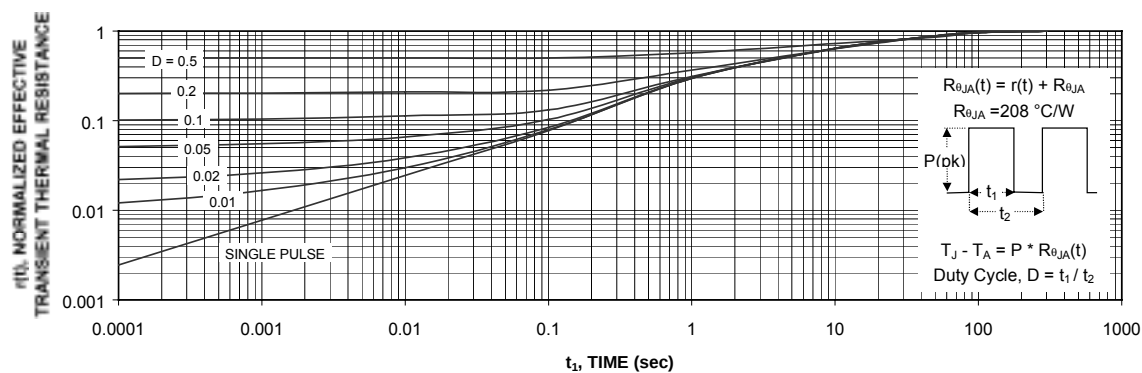


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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