ANALOG DEVICES

50–1000 MHz Quadrature Demodulator

Preliminary Technical Data AD8348

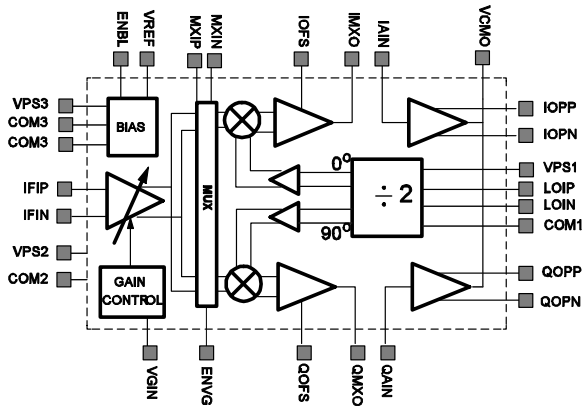
Features

Integrated I/Q demodulator with IF VGA Amplifier
Operating IF Frequency 50–1000 MHz
(3dB IF BW of 500MHz driven from Rs=200ohms)
Demodulation Bandwidth 60MHz
Linear-in-dB AGC Range 45dB
Third Order Intercept
IIP3 +26 dBm @ min gain (FIF=450MHz)
IIP3 -7 dBm @ max gain (FIF=450MHz)
Quadrature Demodulation Accuracy
Phase Accuracy 0.6° RMS
Amplitude Balance 0.3 dB
Noise Figure 12.5dB @ max gain (FIF=500MHz)
LO Input -10 dBm
Single Supply 2.7-5.5V
Power down mode
Compact 28-pin TSSOP package

Applications

QAM/QPSK Demodulator
W-CDMA/CDMA/GSM/NADC
Wireless Local Loop
LMDS/MMDS

Functional Block Diagram



General Description

The AD8348 is a broadband quadrature demodulator with an integrated intermediate frequency (IF) variable-gain amplifier (VGA) and integrated baseband amplifiers. It is suitable for use in communications receivers, performing quadrature demodulation from IF directly to baseband frequencies. The baseband amplifiers have been designed to directly interface with dual channel A-to-D converters such as the AD9201, AD9283, and AD9218 for digitizing and post-processing.

The IF input signal is fed into two Gilbert-cell mixers through an X-AMP VGA. The IF VGA provides 45dB of gain control. A precision gain-control circuit sets a linear-in-dB gain characteristic for the VGA and provides temperature compensation. The LO quadrature phase splitter employs a divide-by-two frequency divider to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range.

Optionally, the IF VGA can be disabled and bypassed. In this mode, the IF signal is applied directly to the quadrature mixer inputs via pins MXIP and MXIN.

Separate I & Q-channel baseband amplifiers follow the baseband outputs of the mixers. The DC common-mode voltage level at the baseband outputs is set by the voltage applied to the VCMO pin. Typically VCMO is connected to the internal VREF voltage but it can also be connected to an external voltage. This flexibility allows the user to maximize the input dynamic range to the A-to-D converter. Connecting a bypass capacitor at each offset compensation input (IOFS & QOFS) nulls DC offsets produced in the mixer. Offset compensation can be overridden by applying an external voltage at the offset compensation inputs.

The mixers' outputs are brought off-chip for optional filtering before final amplification. Inserting a channel selection filter before each baseband amplifier increases the baseband amplifiers' signal handling range by reducing the amplitude of high-level, out-of-channel interferers before the baseband signal is fed into the baseband amplifiers. The single-ended mixer output is amplified and converted to a differential signal for driving ADCs.

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AD8348-SPECIFICATIONS (V_S = 5V; T_A=25 °C; F_{LO}=500MHz; F_{IF}=501MHz; PIo=-10dBm, Rs(LO)= 50 Ω, Rs(IF)=200Ω, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
GENERAL					
LO Frequency Range	External input must be 2x LO frequency	100		2000	MHz
IF Frequency Range		50		1000	MHz
Baseband bandwidth			60		MHz
LO Input Level	50 Ω source, LOIP/LOIN terminated to 50 Ω	-10		0	dBm
LO Input Impedance	Measured differentially across LOIP/LOIN		320Ω||1pF		Ω||pF
VGIN Input Level		0.2		1.2	V
REFERENCE VOLTAGE V_{REF}			1		V
POWER SUPPLIES					
Voltage		2.7		5.5	V
Current Active	ENBL=5V		48		mA
Current Standby	ENBL=0		65		uA

Parameter	Condition	Min	Typ	Max	Units
IF FRONT-END WITH VGA	IFIP/IFIN to IMXO/VREF, QMXO/ VREF ENVG=5V				
Zin		150Ω||1pF	190Ω||1pF	230Ω||1pF	Ω||pF
Variable Gain Range			45		dB
Linear-in-dB error	VGIN=0.3 to 1.1V		+/-1		dB
Maximum Conversion Gain	VGIN=0.2V (max gain)		33		dB
Minimum Conversion Gain	VGIN=1.2V (min gain)		-14		dB
Conversion Gain 3 dB Bandwidth				500	MHz
IF Gain Flatness	FIF=50MHz-500MHz		3		dB p-p
2nd Order Input Intercept(IIP2)	IF1=455MHz, IF2=456MHz -10 dBm each tone from 200 Ω source VGIN=1.2V (min gain)		55		dBm
3rd Order Input Intercept(IIP3)	IF1=455MHz, IF2=456MHz -10 dBm each tone from 200 Ω source VGIN=1.2V (min gain)		26		dBm
2nd Order Input Intercept(IIP2)	IF1=455MHz, IF2=456MHz -42 dBm each tone from 200 Ω source VGIN=0.2V (max gain)		20		dBm
3rd Order Input Intercept(IIP3)	IF1=455MHz, IF2=456MHz -42 dBm each tone from 200 Ω source VGIN=0.2V (max gain)		-7		dBm
1dB Input compression point	VGIN=0.2V (max gain)		-23		dBm
Noise Figure	VGIN=0.2V (max gain) From 200 Ω source				
	Double sideband measurement		10		dB
	FIF=50MHz		12.5		
	FIF=500MHz				
Input LO Leakage	Measured at IFIP,IFIN		-125		dBm
Output LO Leakage	Measured at IMXO/QMXO (LO=50MHz)		10		mVp-p
Demodulation Bandwidth	Full-power bandwidth (IIP3 drops 3dB)		TBD		MHz
	Small-signal 3dB bandwidth		60		MHz
Quadrature Phase Error	LO=1GHz (LOIP/LOIN 2GHz, single-ended)		0.6		deg RMS
I/Q Amplitude Imbalance			0.3		dB
Mixer Output Impedance			40		Ω
Mixer Peak output current			2.5		mA

Parameter	Condition	Min	Typ	Max	Units
IF FRONT-END WITHOUT VGA	from MXIP,MXIN to IMXO/QMXO ENVG=0V				
Zin	Measured differentially across MXIP/ MXIN	150Ω||0.5pF	200Ω || 0.5pF	240Ω||0.5pF	Ω||Pf
Conversion Gain			12		dB
Conversion Gain 3 dB Bandwidth				TBD	MHz
IF Gain Flatness	FIF=50MHz-1GHz		TBD		dB p-p
2nd Order Input Intercept(IIP2)	IF1=455MHz, IF2=456MHz -32 dBm each tone from 200 Ω source		TBD		dBm
3rd Order Input Intercept(IIP3)	IF1=455MHz, IF2=456MHz -32 dBm each tone from 200 Ω source		TBD		dBm
1dB Input compression point	VGIN=0.2V (max gain)		-23		dBm
Noise Figure	VGIN=0.2V (max gain) From 200 Ω source Double sideband measurement		TBD		dB
Input LO Leakage	Measured at MXIP/MXIN		-120		dBm
Output LO Leakage	Measured at IMXO/QMXO		10		mVp-p
Demodulation Bandwidth	Full-power bandwidth (IIP3 drops 3dB)		TBD		MHz
	Small-signal 3dB bandwidth, 10pF load		60		MHz
Quadrature Phase Error	LO=1GHz (LOIP/LOIN 2GHz, single- ended input)		0.6		deg RMS
I/Q Amplitude Imbalance			0.3		dB
Capacitive load	shunt from IMXO,QMXO to VCMO	0		10	pF
Resistive load	shunt from IMXO,QMXO to VCMO		200		Ω
Peak output current			2.5		mA
BASEBAND AMPLIFIER	from IAIN to IOPP/IOPN & QAIN to QOPP/QOPN				
Gain			20		dB
Output Swing	differential		2		Vpp diff
Input referred Noise Voltage			8		nV/rtHz
Bandwidth	10pF differential load		60		MHz
Output DC differential offset	Corrected using 500pF capacitor on IOFS,QOFS		+/-30		mV
Output Common-mode offset			+/-15		mV
Group Delay Flatness	0.1-30MHz		0.3		ns pp
3rd Order Intermod. Distortion	Fin1=5MHz Fin2=6MHz Vin1=Vin2=50mVp-p		-71		dBc
Capacitive load drive capability	Differential across IOPP/IOPN, QOPP/QOPN		10		pF
Resistive load	Differential across IOPP/IOPN, QOPP/QOPN	2k			ohm
Peak output current			1		mA

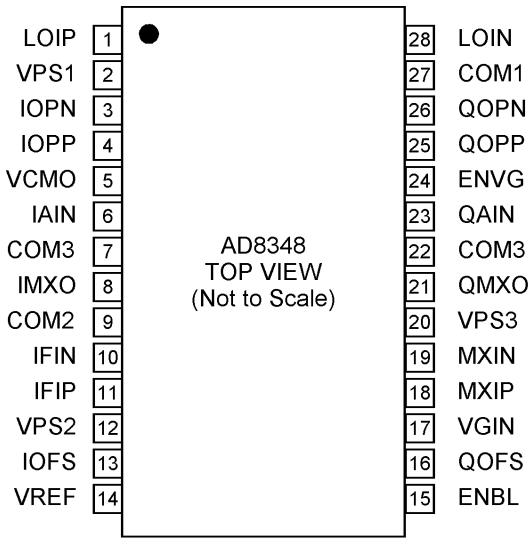
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPS1, VPS2, VPS3……..…….5.5V
LO & RF Input Power ……..……..…TBD dBm
Internal Power Dissipation ….……..……..……..TBD
θ_{JA} ……TBD C/W
Maximum Junction Temperature ……..…+TBD° C
Operating Temperature Range ….-40° C to +85° C
Storage Temperature Range …...-65° C to +150° C
Lead Temperature (Soldering 60 sec)..….+TBD° C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8348 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temp. Range	Package Description	Package Option
AD8348XXX	-34 °C to +85 °C	28-Lead TSSOP Thin Shrink Small Outline Package	RU-28
AD8348-EVAL		Evaluation Board	

PIN FUNCTION DESCRIPTIONS

Pin	Name	Description	Equiv. Cir.
1,28	LOIP,LOIN	LO Input. For optimum performance, these inputs should be driven differentially. Typical input drive level is equal to –10 dBm. To obtain a broadband 50 Ω input impedance, connect a 60.4 Ω shunt resistor between LOIP and LOIN.	
2, 12, 20	VPS1, VPS2, VPS3	Positive Supply for LO, IF, and Biasing & Baseband sections respectively. Each of these pins should be decoupled with 0.1 uF and 100 pF capacitors.	
3,4, 25, 26	IOPN,IOPP, QOPP, QOPN	I- and Q-channel differential baseband outputs. Typical output swing is equal to 2Vpp differential. The DC common-mode voltage level on these pins is set by the voltage on VCMO.	
5	VCMO	Baseband DC common-mode voltage. The voltage applied to this pin sets the DC common-mode levels for all the baseband outputs and inputs (IMXO, QMXO, IOPP, IOPN, QOPP, QOPN, IAIN and QAIN). This pin can either be connected to VREF or to a reference voltage from another device, such as an ADC).	
6	IAIN	I-channel baseband amplifier input. The single-ended signal on this pin is referenced to VCMO and should have a DC bias equal to the DC voltage on the VCMO pin. If IAIN is DC-coupled to IMXO, biasing will be provided by IMXO. If an AC-coupled filter is placed between IMXO and IAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from IAIN to the differential outputs IOPN/IOPP is 20 dB.	
7,22	COM3	Ground for Biasing and Baseband sections.	
8,21	IMXO, QMXO	I- and Q-channel mixer baseband outputs. These are low impedance (40 Ohms) outputs whose bias level is set by the voltage on the VCMO pin. These pins are typically connected to IAIN and QAIN respectively, either directly or through a filter. These outputs can drive a maximum current of 2.5 mA	
9	COM2	IF Section Ground	
10, 11	IFIN,IFIP	IF Input. IFIN should be AC-coupled to ground. The single-ended IF input signal should be AC-coupled into IFIP. The nominal differential impedance of these pins is 200 Ohms. For a broadband 50 Ω input impedance, a minimum loss L-pad should be used. R_{series}=174 Ohms, R_{shunt}=57.6 Ohms.	
13, 16	IOFS, QOFS	I- and Q-channel offset nulling inputs. DC offsets on the I-channel mixer output (IMXO) can be nulled by connecting a 0.1 uF capacitor from IOFS to ground. Driving IOFS with a fixed voltage (typically from a DAC) can extended the operating frequency range to include DC by nulling out the offset at the baseband outputs.	
14	VREF	Reference Voltage Output. This output voltage (1V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers.	
15	ENBL	Chip Enable Input. Active high. Threshold is equal to +Vs/2.	
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the RF VGA. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a conversion gain range from +25 dB to –18 dB. This is the gain to the output of the mixers (i.e. QMXO and IMXO). There is an additional 20 dB of gain in the final baseband amplifiers (IAIN to IOPP/IOPN and QAIN to QOPP/QOPN). Note that the gain control function has a negative sense (i.e. increasing voltage decreases gain).	
18, 19	MXIP, MXIN	Auxiliary mixer inputs. If ENVG is low then the IFIP, IFIN inputs are disabled and MXIP, MXIN are enabled, allowing the VGA to be bypassed. This is a fully differential input which should be AC coupled to the signal source.	
23	QAIN	Q-channel baseband amplifier input. The single-ended signal on this pin is referenced to VCMO and should have a DC bias equal to the DC voltage on the VCMO pin. If QAIN is DC-coupled to QMXO, biasing will be provided by QMXO. If an AC-coupled filter is placed between QMXO and QAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from QAIN to the differential outputs QOPN/QOPP is 20 dB.	
24	ENVG	Active high VGA enable. When ENVG is high, IFIP, IFIN inputs are enabled and MXIP, MXIN inputs are disabled. When ENVG is low, MXIP, MXIN inputs are enabled and IFIP, IFIN inputs are disabled.	
27	COM1	LO Section Ground	

Theory of operation

VGA
The VGA is implemented using the patented X-AMP architecture. The single-ended IF signal is attenuated in eight discrete 6-dB steps by a passive R-2R ladder. Each discrete attenuated version of the IF signal is applied to the input of a transconductance stage. The current outputs of all transconductance stages are summed together and drive a resistive load at the output of the VGA. Gain control is achieved by smoothly turning on and off the relevant transconductance stages with a temperature-compenstated interpolation circuit. This scheme allows the gain to continuously varied over a 48dB range with linear-in-dB gain control. This configuration also keeps the relative dynamic range constant (e.g. IIP3-NF in dB) over gain setting. The absolute intermodulation intercepts and noise figure, however, vary directly with gain. The analog voltage VGIN sets the gain. VGIN=0V is the maximum gain setting, and VGIN=1.2V is the minimum voltage gain setting.

Downconversion mixers
The output of the VGA drives two (I & Q) double-balanced Gilbert-cell down-conversion mixers. Alternatively, the VGA can be disabled by driving the ENVG pin low and the mixers can be driven directly externally via the MXIP, MXIN port. At the input of the mixer, a degenerated differential pair performs linear voltage-to-current conversion. The differential output current feeds into the mixer core where it is downconverter by the mixing action of the Gilbert cell. The phase splitter provides quadrature LO signals which drive the LO ports of the in- phase and quadrature mixers.

Buffers at the output of each mixer drive pins IMXO and QMXO respectively. These linear, low-output impedance buffers drive 40ohm temperature-stable, passive resistors in series with each of the output pins (IMXO, QMXO). This 40ohms should be considered when calculating the reverse termination if an external filter is inserted between IMXO(QMXO) and IAIN(QAIN). The DC output level of the buffer is set by the VCMO pin. This can be set externally or connected to the on-chip 1.0V reference VREF.

Phase splitter
Quadrature generation is achieved using a divide-by-two frequency divider. Unlike a poly-phase filter which achieves quadrature over a limited frequency range, the divide-by-two approach maintains quadrature over a broad frequency range and does not attenuate the LO. The user, however, must provide an external reference XLO which is twice the frequency of the desired LO frequency. XLO drives the clock inputs of two flip-flops which divide down the frequency by a factor of two. The outputs of the two flip-flops are one half-period of XLO out of phase. Equivalently, the outputs are one quarter-period (90 degrees) of the desired LO frequency out of phase. Because the transitions on XLO define the phase difference at the outputs, deviation from 50% duty cycle translates directly to quadrature phase errors.

Baseband amplifiers
Two (I &Q) fixed-gain (20dB), single-ended to differential amplifers are provided to amplify the demodulated signal after off-chip filtering. The amplifiers use voltage feedback to linearize the gain over the demolation bandwidth. These amplifiers can be used to maximize the dynamic range at the input of an ADC following the AD8348.

The input to the baseband amplifiers IAIN (QAIN) feeds into the base of a bipolar transistor with an input impedance of roughly 100kohm. The baseband amplifiers sense the single-ended difference between IAIN (QAIN) and VCMO. IAIN can be DC biased by terminating with a shunt resistor to VCMO, such as when an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). Alternatively, any DC connection to IMXO (QXMO) can provide appropriate bias via the offset-nulling loop.

Bias
The global bias for the chip is controlled by a master biasing cell that can be disabled using the ENBL pin. If the ENBL is held low, the entire chip will power down to a low-power sleep mode typically consuming 60uA at 5V.

Baseband offset cancellation
A low output current integrator senses the output voltage offset at IOPP,IOPN (QOPP,QOPN) and injects a nulling current into the signal path. The integration time constant of the offset nulling loop is set by capacitor COFS from IOFS (QOFS) to VCMO. This forms a high-pass response for the baseband signal path with a lower 3dB frequency of

$$f_{pass} = \frac{1}{2\pi \cdot 200\Omega \cdot C_{OFS}}$$

Alternatively, the user can externally adjust the DC offset by driving IOFS (QOFS) with a digital-to-analog converter or other voltage source. In this case, the baseband circuit will operate all the way down to DC (fpass=0Hz). The integrator output current is only 50uA and can be easily overridden with an external voltage source. The IOFS (QOFS) pin must be either connected to a bypass capacitor (>0.1uF) or an external voltage source to prevent the feedback loop from oscillating.

Applications

Basic Connections
The basic connections described here refer to the AD8348 evaluation board. The schematic for the evaluation board is shown in Figure 1.

Power Supply
The voltage supply for the AD8348, between 2.7V and 5V, should be connected to the +Vs test point and ground should be connected to one of the GND test points.

Device Enable
To enable the device, the pin ENBL should be driven to +Vs. Grounding the same pin will disable the device. On the evaluation board this can be achieved by moving SW11 to the ENBL and DENBL positions respectively.

VGA Enable
The VGA can be enabled by driving the voltage on the pin ENVG to +Vs. In this mode, the MX inputs are disabled and the IF inputs should be utilized. Grounding the pin will disable the VGA and the IF inputs. When the VGA is disabled the MX inputs should be used. On the evaluation board, SW12 should be positioned in either the IF or MX positions.

Gain Control
When the VGA is enabled, the gain can be controlled by the voltage on pin VGIN. The gain control voltage range is between 0.2 V and 1.2 V. This corresponds to a gain range between 25.6 dB and –18.3 dB. For convenience, a potentiometer R15 is provided to allow for changes in gain without the need for an additional DC voltage source. To use the potentiometer, the switch SW13 must be set to the POT position. Alternatively, an external voltage applied to either the testpoint or SMA connector labeled VGIN can set the gain. SW13 must be set to the EXT position when an external gain control voltage is used.

LO Input
The local oscillator signal should be fed to the SMA connector J21. This port is terminated in 50 Ohms. The recommended LO drive level is between –10 and 0 dBm. The LO frequency at the input to the device should be twice that of the desired LO frequency at the mixer core. The applied LO frequency range is between 100 MHz and 2 GHz.

IF Input
The IF input should be fed into the SMA connector IFIP. The VGA must be enabled when this port is used (SW12 in the IF position).

MX Input
The input to the mixer input can be either single-ended or differential. The evaluation board is, by default, set for single-ended MX drive. To change to a differential drive, T41 should be removed along with resistor R42. DC blocking capacitors (C42, C43) should be installed in place of T41. This will present a nominal differential impedance of 200 Ohms (100 Ohms each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.

Baseband Outputs
The baseband outputs are at the IOPP, IOPN, QOPP and QOPN testpoints and SMA connectors. These outputs are not designed to drive 50 Ohm loads directly and should be presented with loads of at least 2k Ohms.

Output DC Bias Level
The DC bias level of the baseband amplifier outputs are by default tied to Vref through LK11. If desired, the DC bias level can be changed by removing LK11 and driving a DC voltage onto either the VCMO testpoint.

Evaluation Board

Figure 1 shows the schematic for the AD8348 evaluation board. Note that uninstalled components are indicated with the "OPEN" designation. The board is powered by a single supply in the range of 2.7 to 5.5 V. Table I details the various configuration options of the evaluation board.

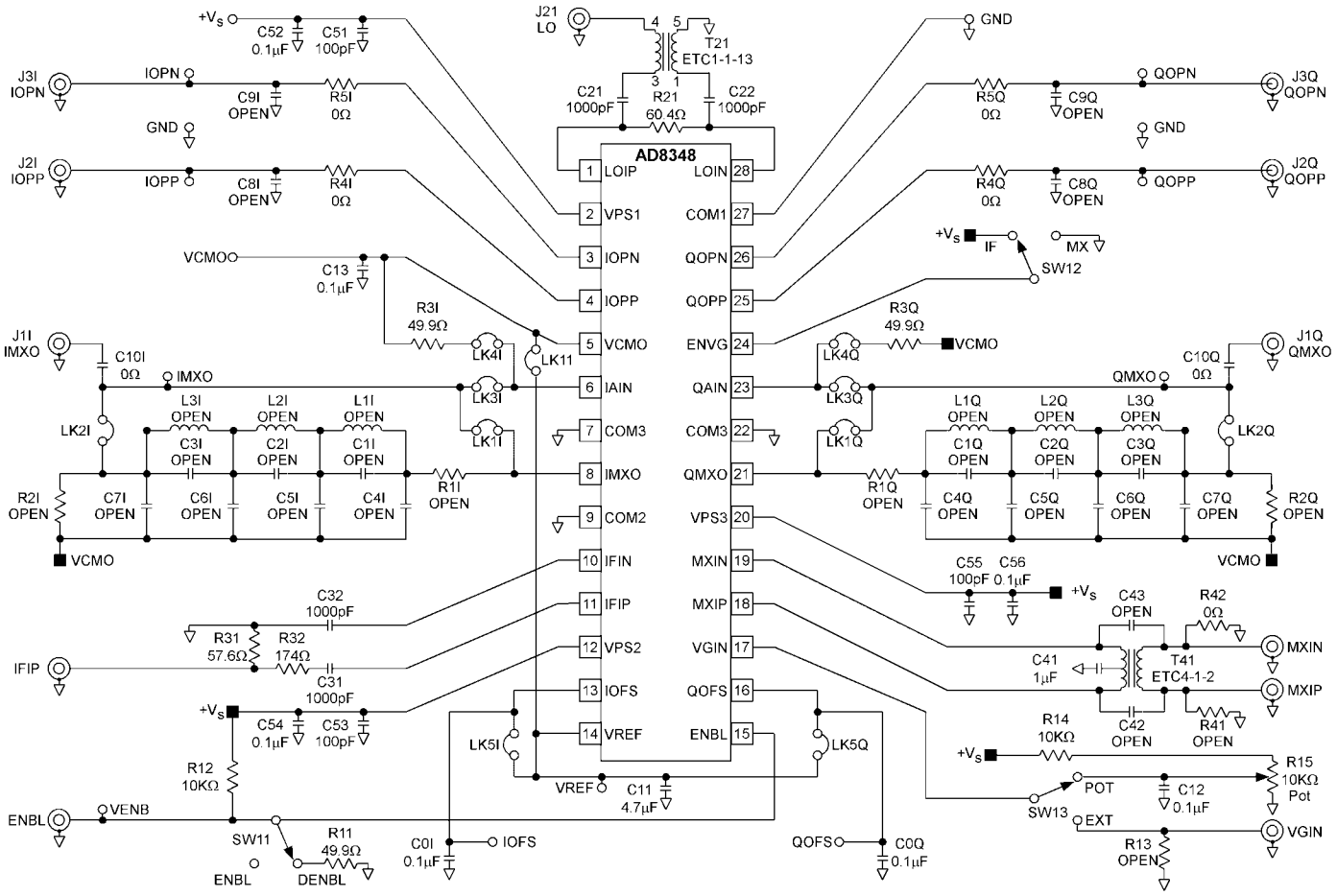


Figure 1. Evaluation board schematic.

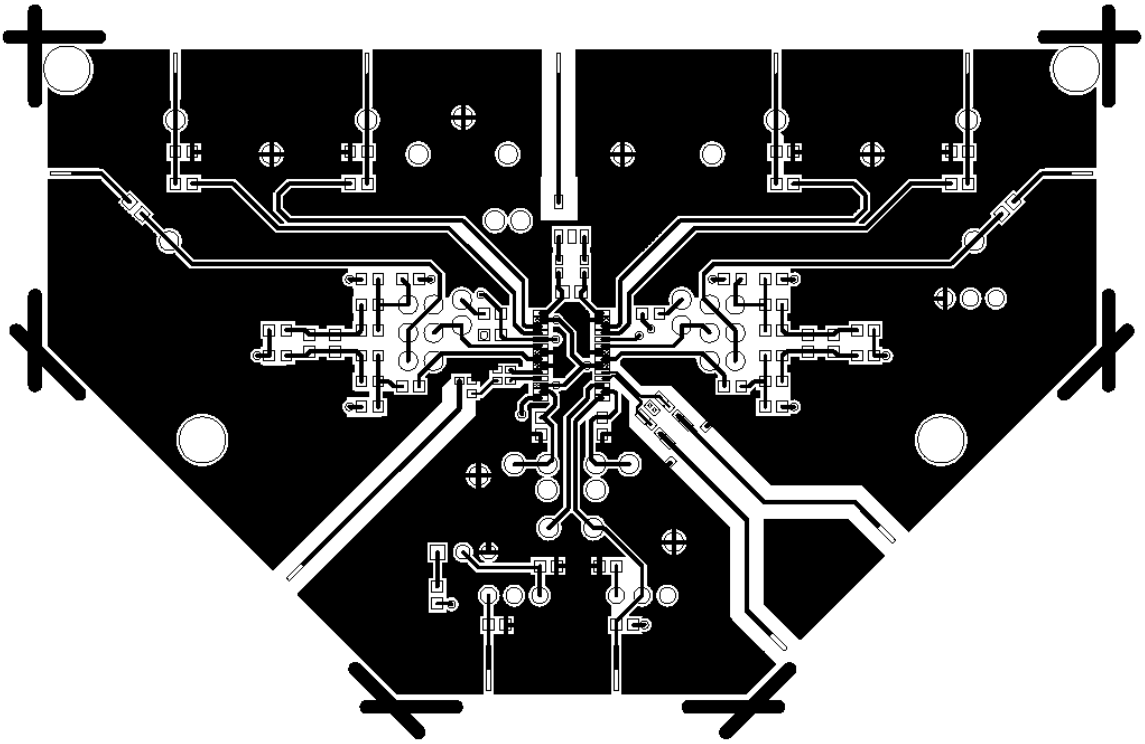


Figure 2. Evaluation Board Top Layer.

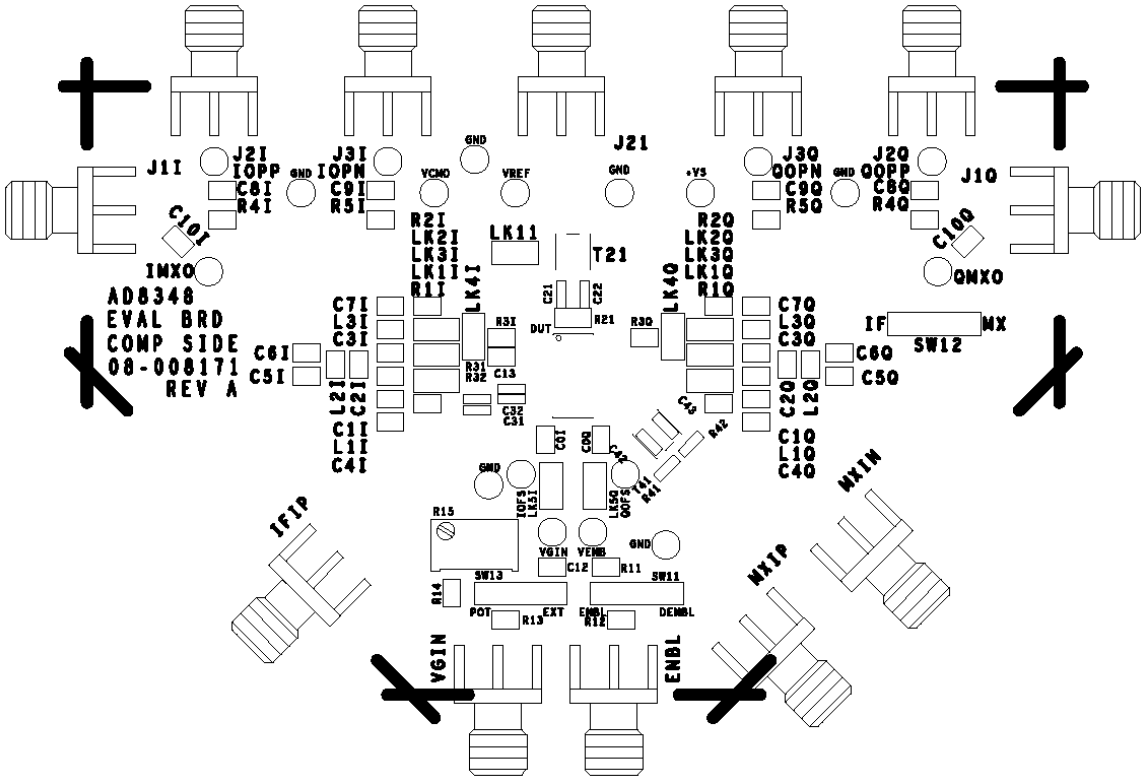


Figure 3. Evaluation Board Top Silkscreen.

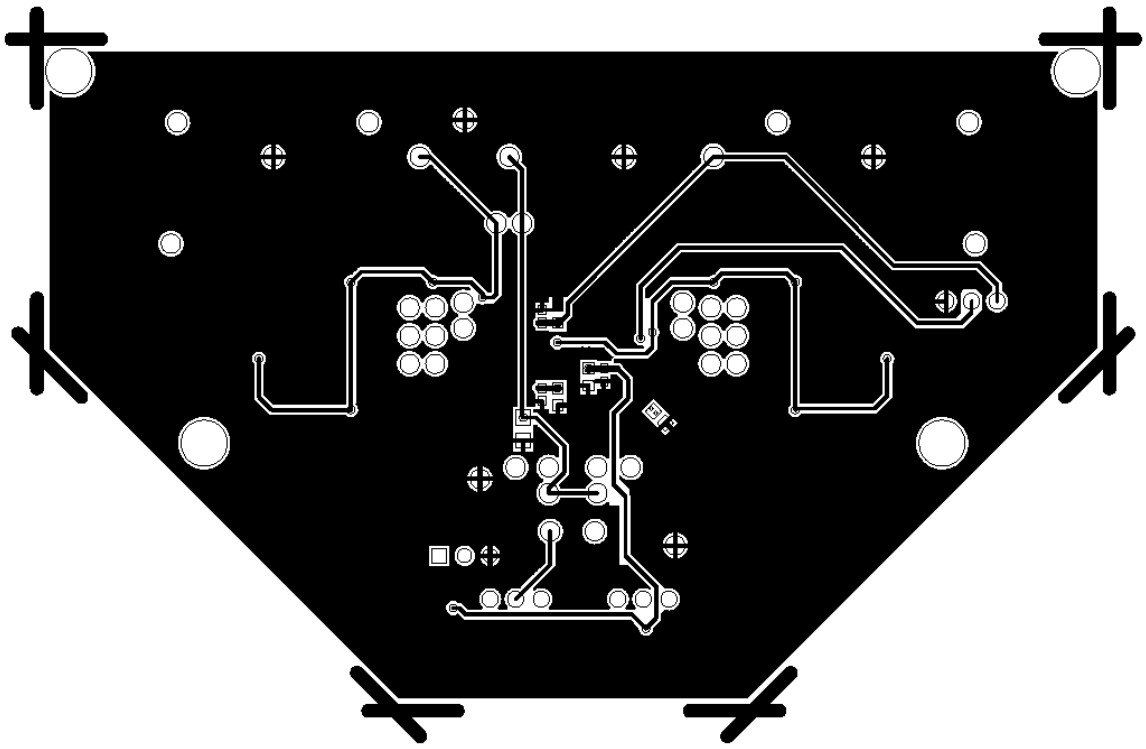


Figure 4. Evaluation Board Bottom Layer.

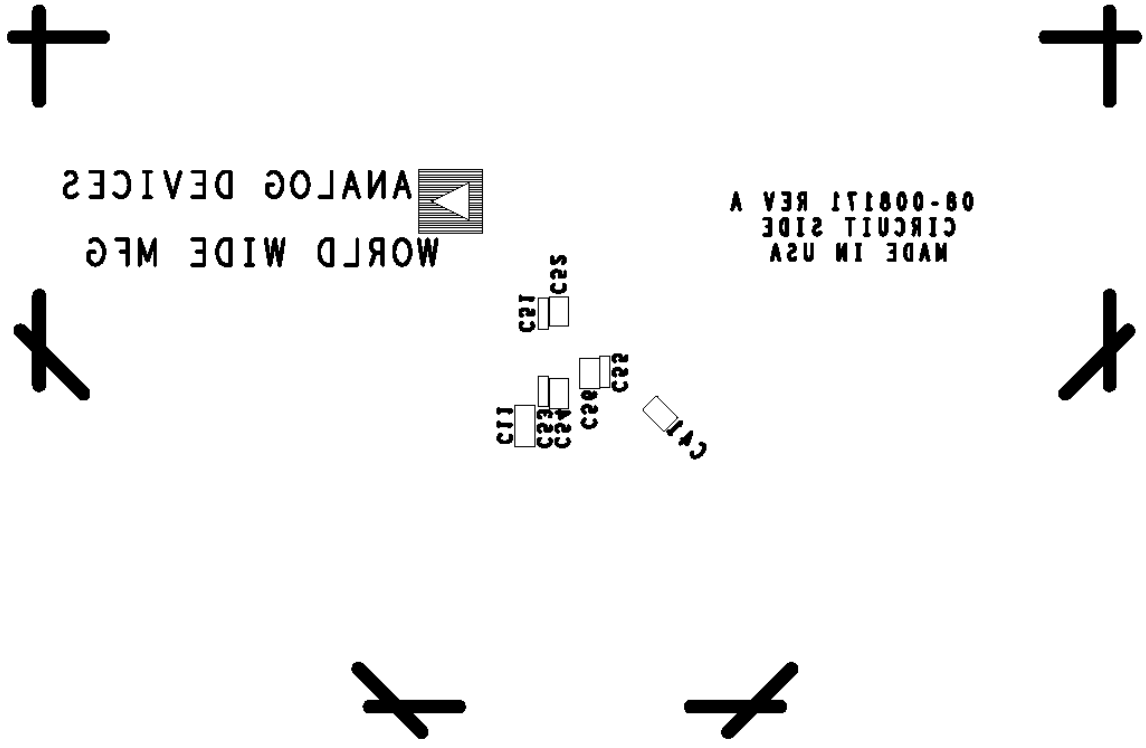


Figure 5. Evaluation Board Bottom Silkscreen.

Table I Evaluation Board Configuration Options

Component	Function	Default Condition
+Vs, GND	**Power Supply and Ground Vector Pins**	Not Applicable
SW11, ENBL	**Device Enable:** Place SW11 in the ENBL position to connect the ENBL pin to +Vs. Place in the DENBL position to disable the device by grounding the pin ENBL through a 50 Ohm pull down resistor. The device may also be enabled via an external voltage applied to ENBL or VENB.	SW11 = ENBL
SW13, R15, VGIN	**Gain Control Selection:** With SW13 in the POT position the gain of the VGA can be set using the potentiometer R15. With SW13 in the EXT position the VGA gain can be set by an external voltage to SMA connector VGIN. For VGA operation the VGA must first be enabled by setting SW12 to the IF position.	SW2 = POT
SW12	**VGA Enable Selection:** With SW12 in the IF position, the ENVG pin is connected to +Vs and the VGA is enabled. The IF input should be used when SW12 is in the IF position. With SW12 in the MX position the ENVG pin is grounded and the VGA is disabled. The MX inputs should be used when SW12 is in the MX position.	SW12 = IF
IFIP, R31, R32	**IF Input:** The single-ended IF signal should be connected to this SMA connector. R31 and R32 form a L-pad that presents a 50 Ohm termination to the input.	R31 = 57.6 Ohms R32 = 174 Ohms
MXIP, MXIN T41, R42	**Mixer Inputs:** These inputs can be configured for either differential or single-ended operation. The default is single-ended operation with T41 and R42 installed. In single-ended mode the input is applied to the 50 Ohm SMA connector MXIP. For differential drive, T41 should be	T41 = ETC4-1-2 R42 = 0 Ohms
C42, C43	removed along with resistor R42. DC blocking capacitors (C42, C43) should be installed in place of T41. This will present a nominal differential impedance of 200 Ohms (100 Ohms each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.	
LK11, VCMO	**Baseband Amplifier Output Bias**: Installing LK11 connects VREF to VCMO. This sets the bias level on the baseband amplifiers to V_{REF} which is equal to approximately 1V. Alternatively, with LK11 removed, the bias level of the baseband amplifiers can be set by applying an external voltage to the VCMO testpoint.	LK11 Installed
C8, C9, R4, R5 (I and Q)	**Baseband Amplifier Outputs and Output Filter:** Additional low-pass filtering can be provided at the baseband output with these filters.	R4, R5 = 0 Ohms
C10 (I and Q)	**Mixer Output DC Blocking Capacitors:** The mixer outputs are biased to VCMO. To prevent damage to test equipment that cannot tolerate DC biases, C10 is provided to block the DC component, thus protecting the test equipment.	C10 = 0 Ohms
C1 – C7 R1, R2 L1 – L3 (I and Q)	**Baseband Filter:** These components are provided for baseband filtering between the mixer outputs and the baseband amplifier inputs. The baseband amplifier input impedance is high and the filter termination impedance is set by R2. See Table II below for jumper settings.	All = OPEN
LK5 (I and Q)	**Offset Compensation Loop Disable:** Installing these jumpers will disable the offset compensation loop for the corresponding channel.	LK5x = OPEN

Table II Filter Jumper Configuration Options

Condition	LK1 x	LK2 x	LK3 x	LK4 x
xMXO to xAIN direct	●		●	
xMXO to xAIN via filter		●	●	
xMXO to J1x direct, xAIN unused	●			●
xMXO to J1x via filter, xAIN unused		●		●
Drive xAIN from J1x (x = I and Q)				●

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)