To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M61506FP

Peak hold IC for 5 band spectrum analyzer displays

DESCRIPTION

The M61506FP is a 5 band peak hold ICs that use microprocessor time division to produce serial output for spectrum analyzer displays.

FEATURES

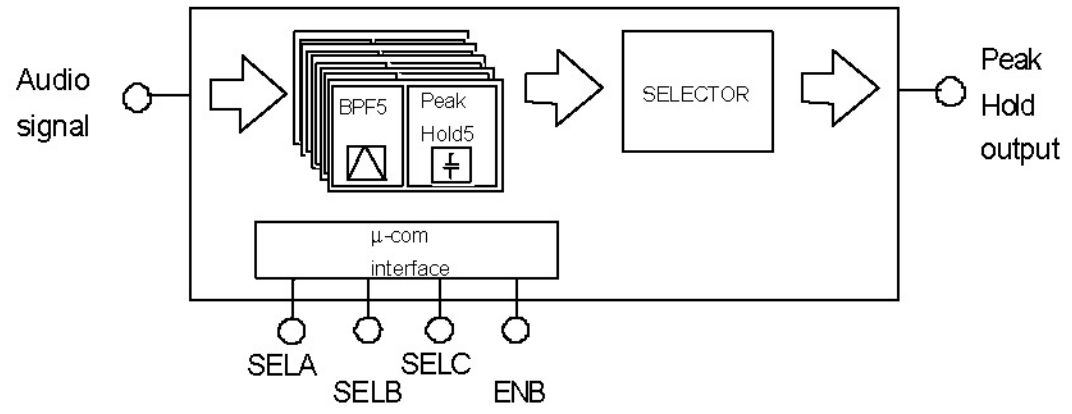
- 5 band peak hold elements for spectrum analyzer displays.
- Discharge time constant circuit for each band is on the chip.
- Single 5V power supply.

RECOMMENDED OPERATING CONDITIONS

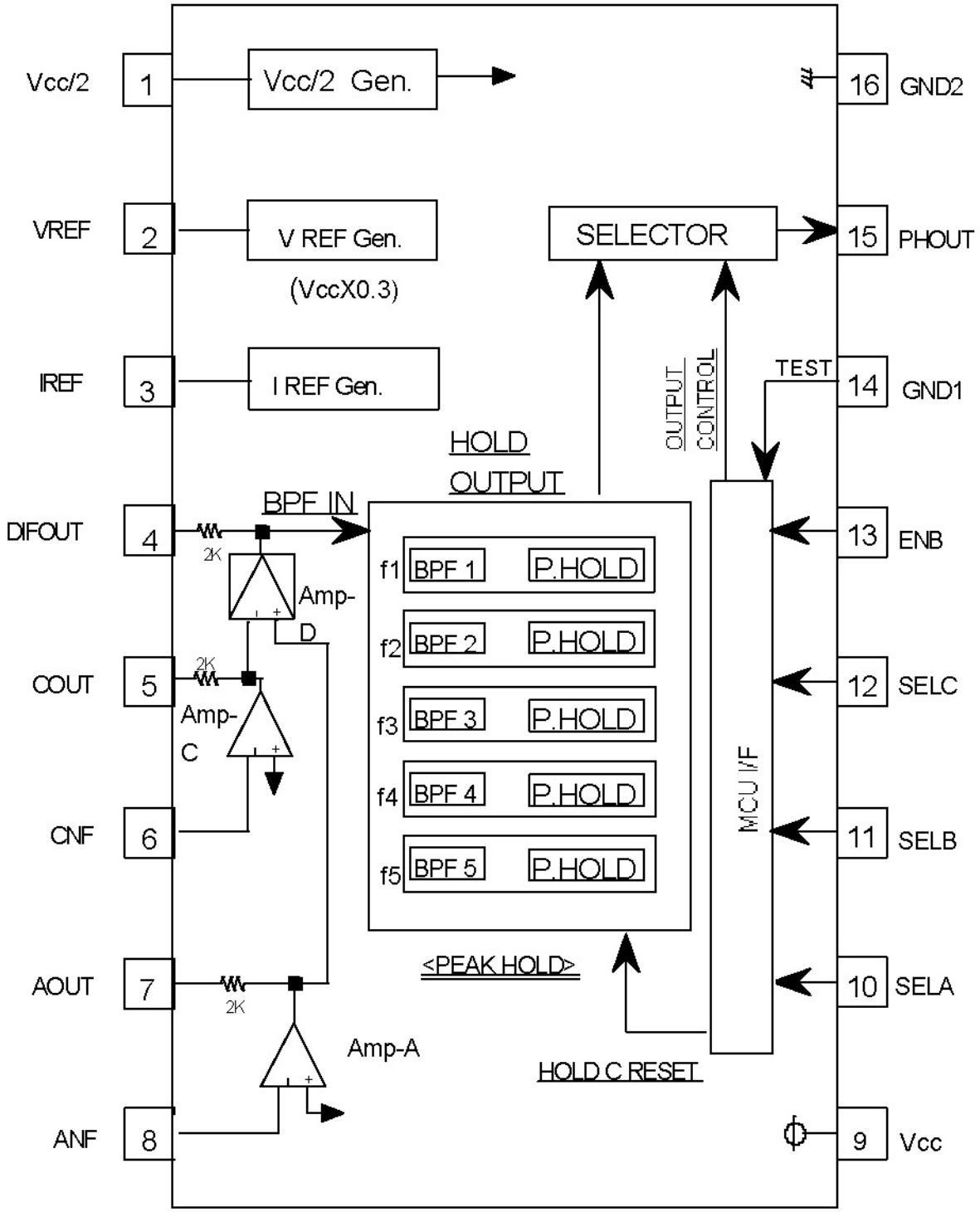
Supply voltage range ——— 4.5 to 6.5V

Rated supply voltage ——— 5.0V

SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



(Notes)f1=105Hz,f2=340Hz,f3=1KHz,f4=3.4KHz,f5=10.5KHz

(The value is the design value)

Units Resistance :Ω
Capacitance: F

FUNCTIONAL DESCRIPTION

(1)The audio signal amplified by Amp-A and Amp-D into BPF/peak hold circuit for spectrum analyzer display.
Because the last output signal inputs into A/D of microprocessor.
The Vcc,GND had better be common with Vcc,GND of A/D of maicroprocessor.
It untilizes effect of common-mode rejection of Amp-D.Amp-C is the input amplifier to reject common-mode signal(noise).To get to good ground isolation.

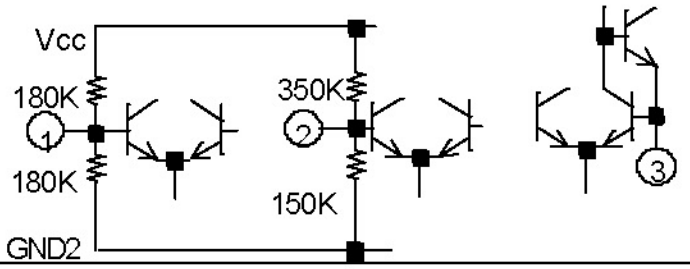
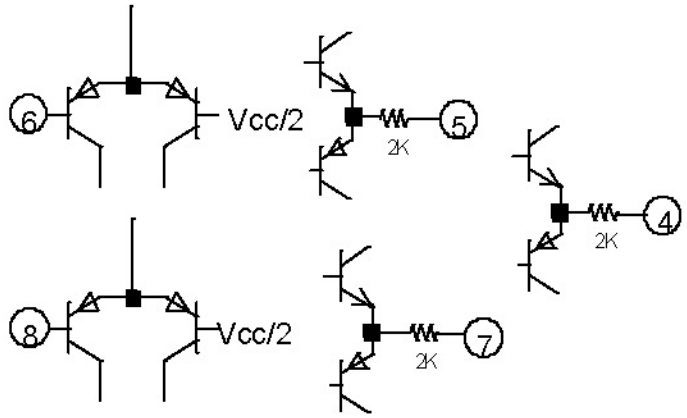
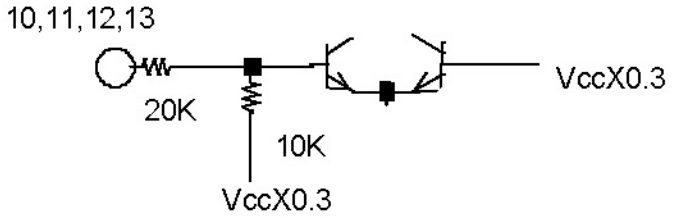
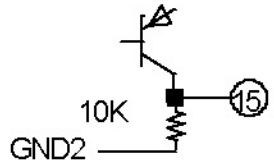
(2)BPF/peak hold circuit is fit for 5 band spectrum analyzer display.
<center frequency>
f1=105Hz
f2=340Hz
f3=1KHz
f4=3.4KHz
f5=10.5KHz
(The value is the design value)
Center frequency and Q of BPF is
$\omega 0=gm/C$
gm:matual condactance of inside amplifier circuit
(It depends on outside resistor value of Pin.No.3)
C:inside capacitor
Q=(R1+R2)/R1:it is fixed by inside resistor ratio.
(The design value of Q is 3.5)

(3)The hold capacitor of peak hold circuit is included.
The reset(discharge) signal is made automatically after ending the output of hold value(Discharge pulse effect:-3dB(typ).fall refer to output value)

(4)The internal output voltage of peak hold circuit is refered to Vcc/2. (Pin.No.1)
When it is selected by the output select circuit,it appear at PHout (Pin.No.15) refered to GND.

PIN DESCRIPTION

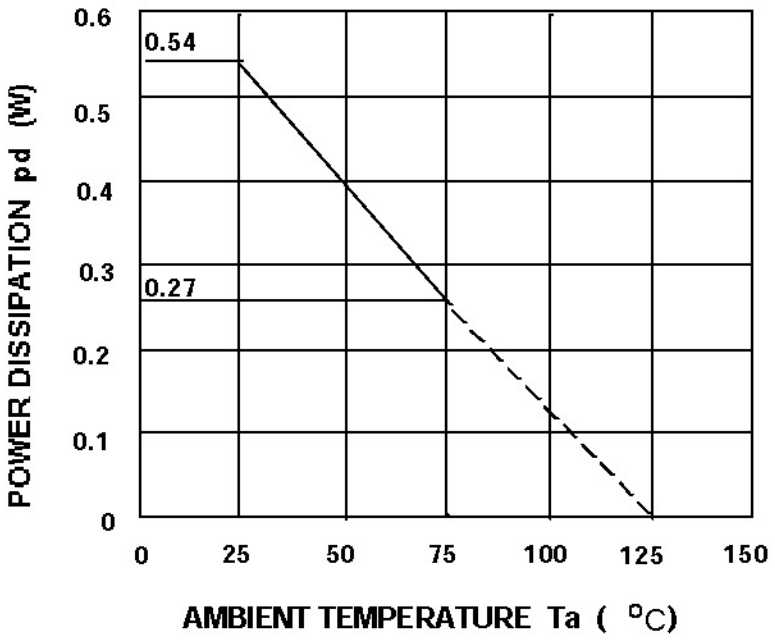
PIN No.	Name	I/O	Function
1	Vcc/2	I	1/2Vcc bias
2	VREF	I	0.3Vcc bias
3	IREF	I	BPF center frequency setting current terminal
4	DIFOUT	O	Output of amplifier-D(BPF input signal)
5	COUT	O	Output of amplifier-C
6	CNF	I	Inverted input of amplifier-C
7	AOUT	O	Output of amplifier-A
8	ANF	I	Inverted input of amplifier-A
9	Vcc	I	System supply
10	SELA	I	Output setting control terminal A(logic input)
11	SELB	I	Output setting control terminal B(logic input)
12	SELC	I	Output setting control terminal C(logic input)
13	ENB	I	Output setting control enable terminal(logic input)
14	GND1	I	Ground 1
15	PHOUT	O	Peak hold output terminal
16	GND2	I	Ground 2

PIN No.	Name	I/O	Peripheral circuit of pins
1	Vcc/2	I	
2	VREF	I	
3	IREF	I	
4	DIFOUT	O	
5	COUT	O	
6	CNF	I	
7	AOUT	O	
8	ANF	I	
9	Vcc	I	Supply
10	SELA	I	
11	SELB	I	
12	SELC	I	
13	ENB	I	
14	GND1	I	Ground1
15	PHOUT	O	
16	GND2	I	Ground2

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc(max)	Supply Voltage		7	V
Pd	Power dissipation	Ta≤25 °C	540	mW
Kθ	Thermal derating	Ta>25 °C	5.4	mW/ °C
Topr	Operating temperature		-20 to +75	°C
Tstg	Storage temperature		-40 to +125	°C
Vi(max)	Input voltage range		GND-0.3 to Vcc+0.3	V
Vo(max)	Output voltage range		GND to Vcc	V

Thermal derating(maximum rating)



Recommended operating conditions

(Ta=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	Vcc		4.5	5.0	6.5	V
Logic input H level voltage	VIH	Vcc=5V	2.5	——	VCC	V
Logic input L level voltage	VIL	Vcc=5V	GND	——	0.5	V

(Note 1)

The center frequency characteristics of BPF are determined by the resistor connected between 3pin terminal and GND.If it is necessary,adjust the resistor value(note:all bands will be shifted together).

The Q of BPF is fixed in 3.5 by inside circuit.

(Note 2)

The internal output resistor of peak hold output(PIN 15)is 10k typ.

The input resistance of the microprocessor must be much larger than 10k .

(Note 3)

The control voltage from the microprocessor must be from GND -0.3V to Vcc+0.3V.

If the control voltage is out of the above range.

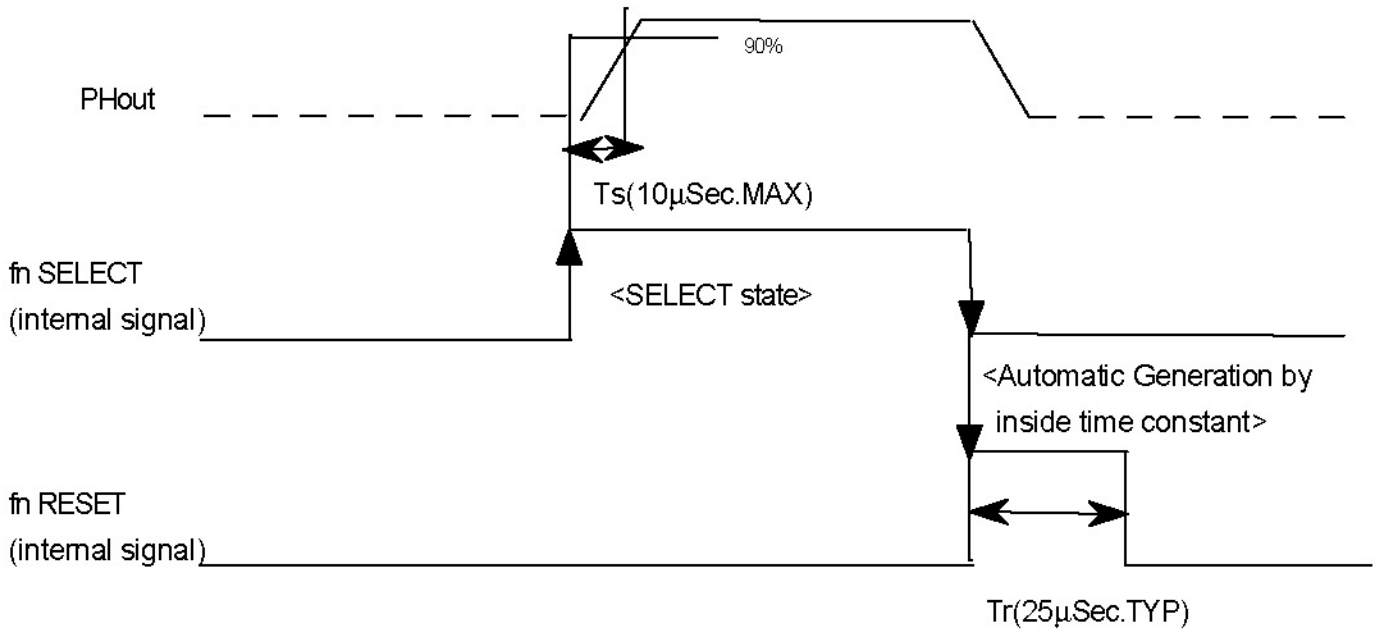
It`s necessary to modify the control voltage in the above range by using resistors or diodes.

OUTPUT CONTROL SPECIFICATION

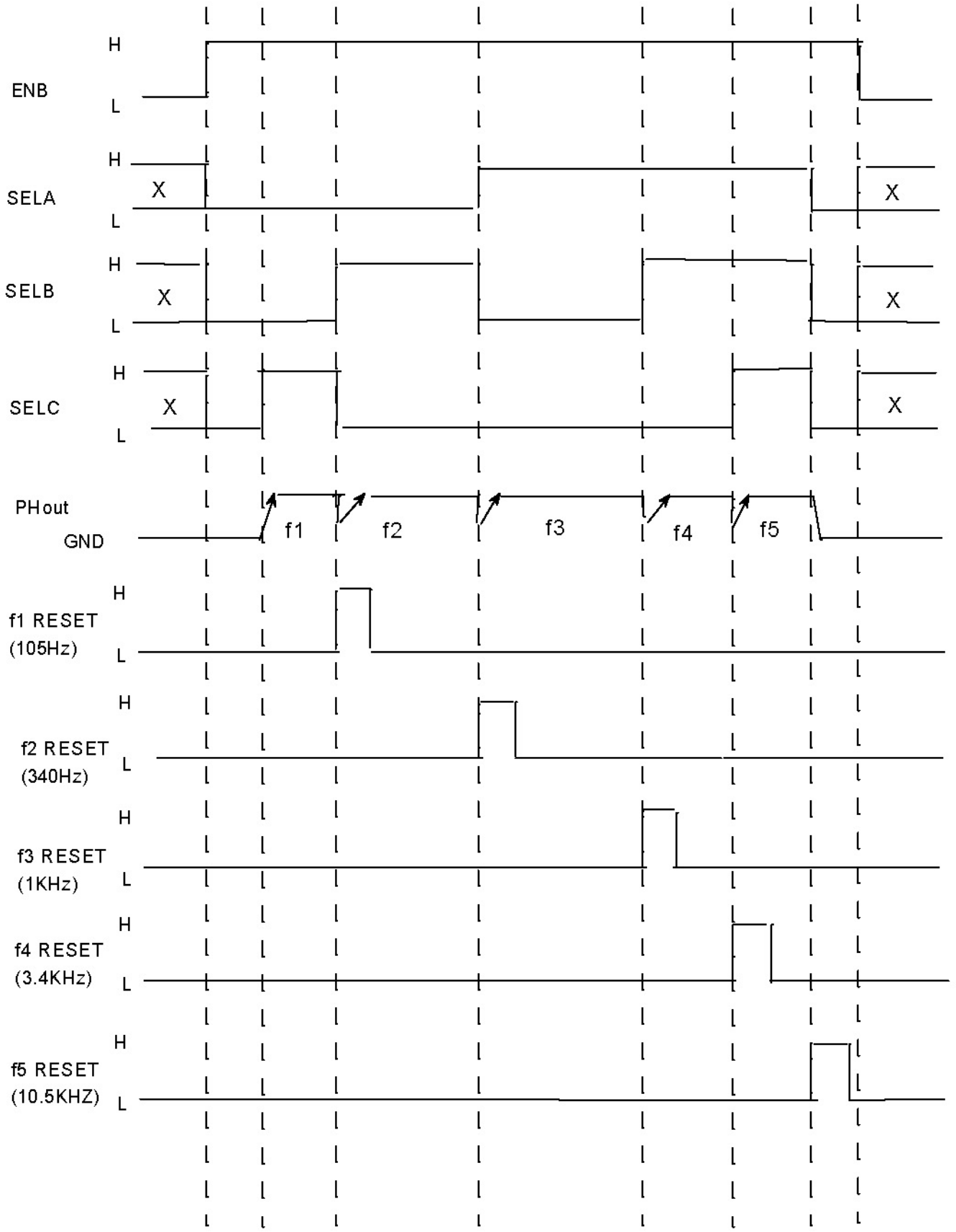
<Output select logic table>

PHout (PinNo.15)	ENB	SELA	SELB	SELC	Note
GND(output stop)	0	X	X	X	X:Don`t Care
GND	1	0	0	0	
f1:105Hz	1	0	0	1	
f2:340Hz	1	0	1	0	
GND	1	0	1	1	
f3:1kHz	1	1	0	0	
GND	1	1	0	1	
f4:3.4kHz	1	1	1	0	
f5:10.5kHz	1	1	1	1	

<Note 1>
'H'=low level,'1'=high level,'X'='0'or'1'
<Note 2>
The output setting time is more than 10µsec.
(When the output setting time is short,the output value and reset signal become unstable)



TIMING CHART

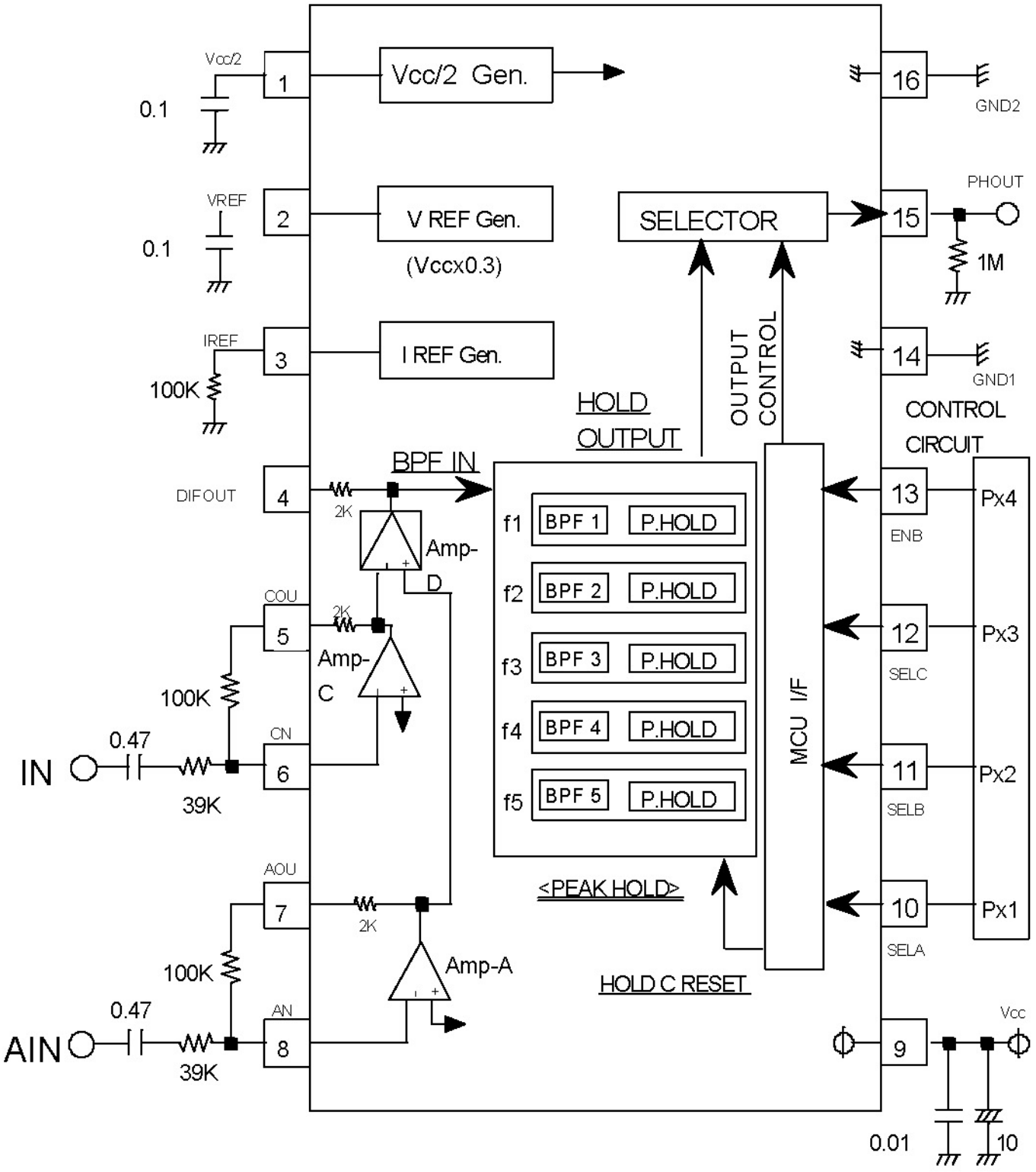


ELECTRICAL CHARACTERISTICS

(Ta=25 °C ,Vcc=5.0V,PHout(Pin.No.15)RL=1MΩ unless otherwise noted.VAIN=-30dBV, f=1KHz,ENB(Pin.No.13)=1)

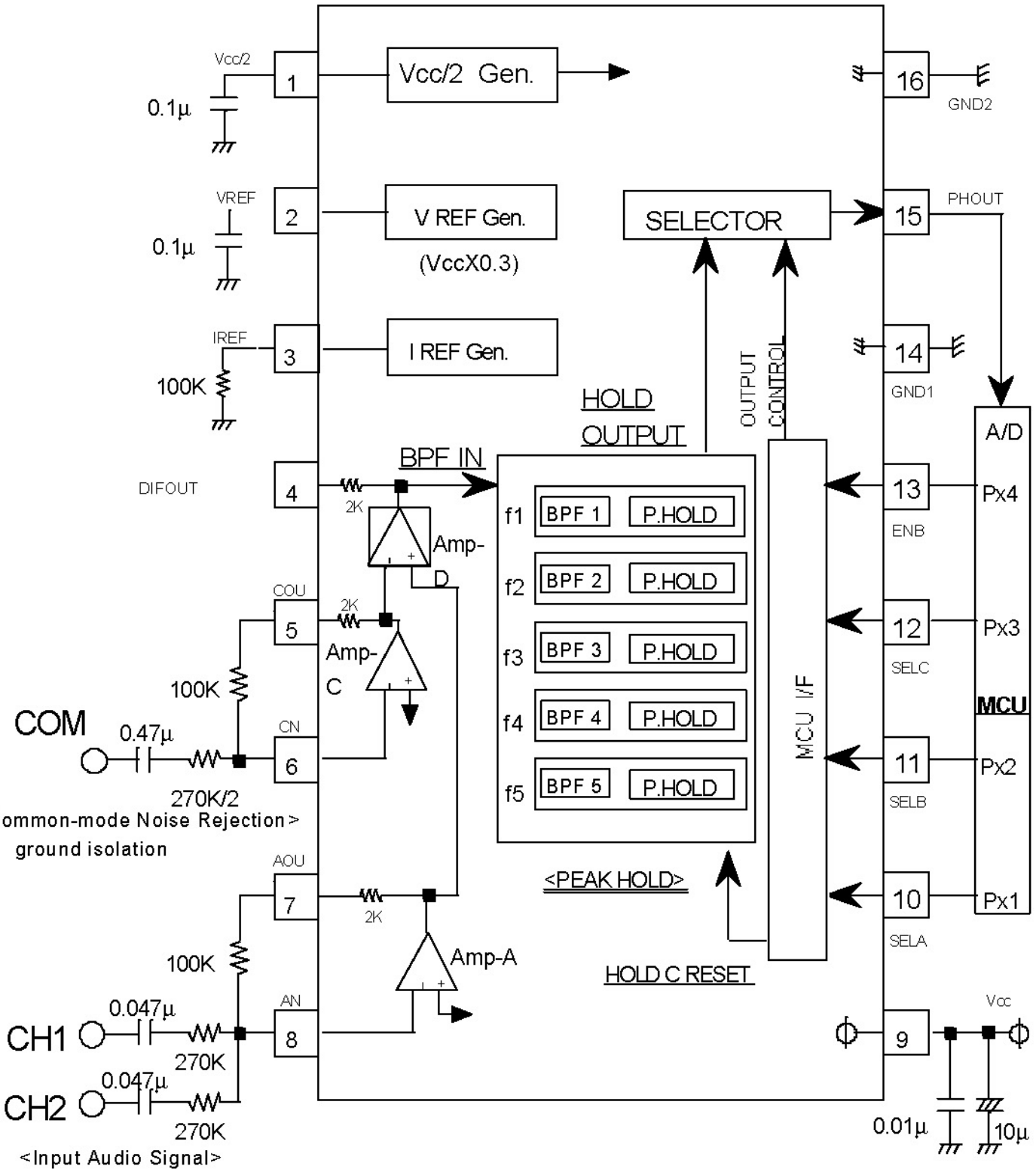
Parameter	Symbol	Condition	Limits			Unit
			Min	typ	Max	
Circuit current	Icc	No signal,No select (ENB,SELA,SELB,SELC=0)	—	8	13	mA
Maximum output level	Vo	f1 to f5 Measured at each output (VAIN=-14dBV)	4.0	4.7	—	V
Output offset voltage	Vos	f1 to f5 Measured at each output (No signal,ENB=0/1)	—	30	60	mV
Logic input H level	VIH		2.5	5.0	Vcc +0.3	V
Logic input L level	VIL		GND -0.3	0	0.5	V
Common-mode rejection ratio	CMRR		25	50	—	dB
f1 output level	Vo1	f1(fin=80 to 130Hz)	0.5	1.0	1.70	V
f2 output level	Vo2	f2(fin=270 to 410Hz)	0.5	1.0	1.70	V
f3 output level	Vo3	f3(fin=0.8 to 1.2KHz)	0.5	1.0	1.70	V
f4 output level	Vo4	f4(fin=2.7 to 4.1KHz)	0.5	1.0	1.70	V
f5 output level	Vo5	f5(fin=8.0 to 13.0KHz)	0.5	1.0	1.70	V
Output response time	Ts	The time from the rise of output selection until the rise of PHout (90% of peak)	—	5	10	µsec
Discharge level	DS	<Reference> Inside reset signal Tr=25µsecTYP.	—	-3	—	dB

TEST CIRCUIT



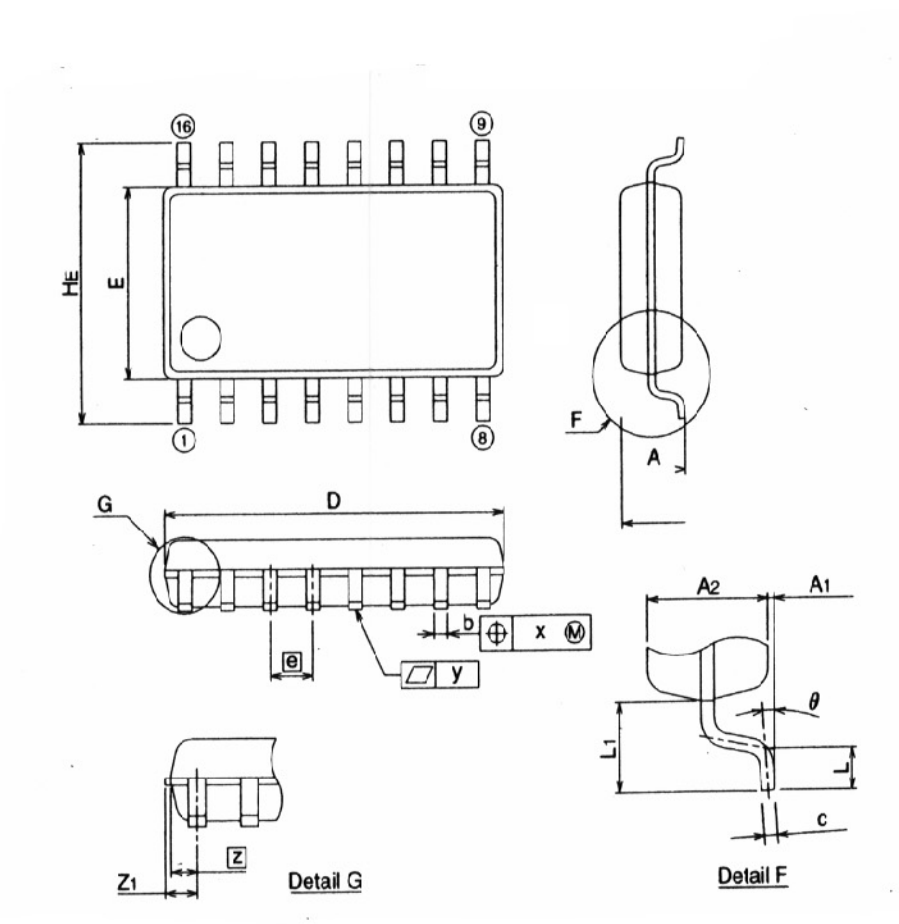
Units resistance:
capacitance:F

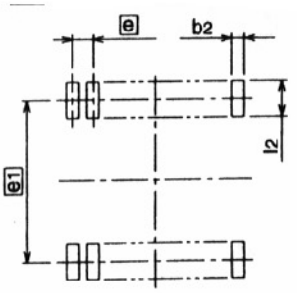
APPLICATION EXAMPLE



Units resistance: Ω
capacitance: F

OUTLINE





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A			2.1
A1	0	0.1	0.2
A2	–	1.8	–
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	1.27	–
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	–	1.25	–
z	–	0.605	–
Z1	–	–	0.755
x	–	–	0.25
y	–	–	0.1
θ	0°	–	8°
b2	–	0.76	–
e1	–	7.62	–
l2	1.27	–	–