

# MPC8541E PowerQUICC™ III Integrated Communications Processor Hardware Specifications

The MPC8541E integrates a PowerPC™ processor core built on Power Architecture™ technology with system logic required for networking, telecommunications, and wireless infrastructure applications. The MPC8541E is a member of the PowerQUICC™ III family of devices that combine system-level support for industry-standard interfaces with processors that implement the embedded category of the Power Architecture technology. For functional characteristics of the processor, refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual*.

To locate any published errata or updates for this document refer to <http://www.freescale.com> or contact your Freescale sales office.

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# 1 Overview

The following section provides a high-level overview of the MPC8541E features. Figure 1 shows the major functional units within the MPC8541E.

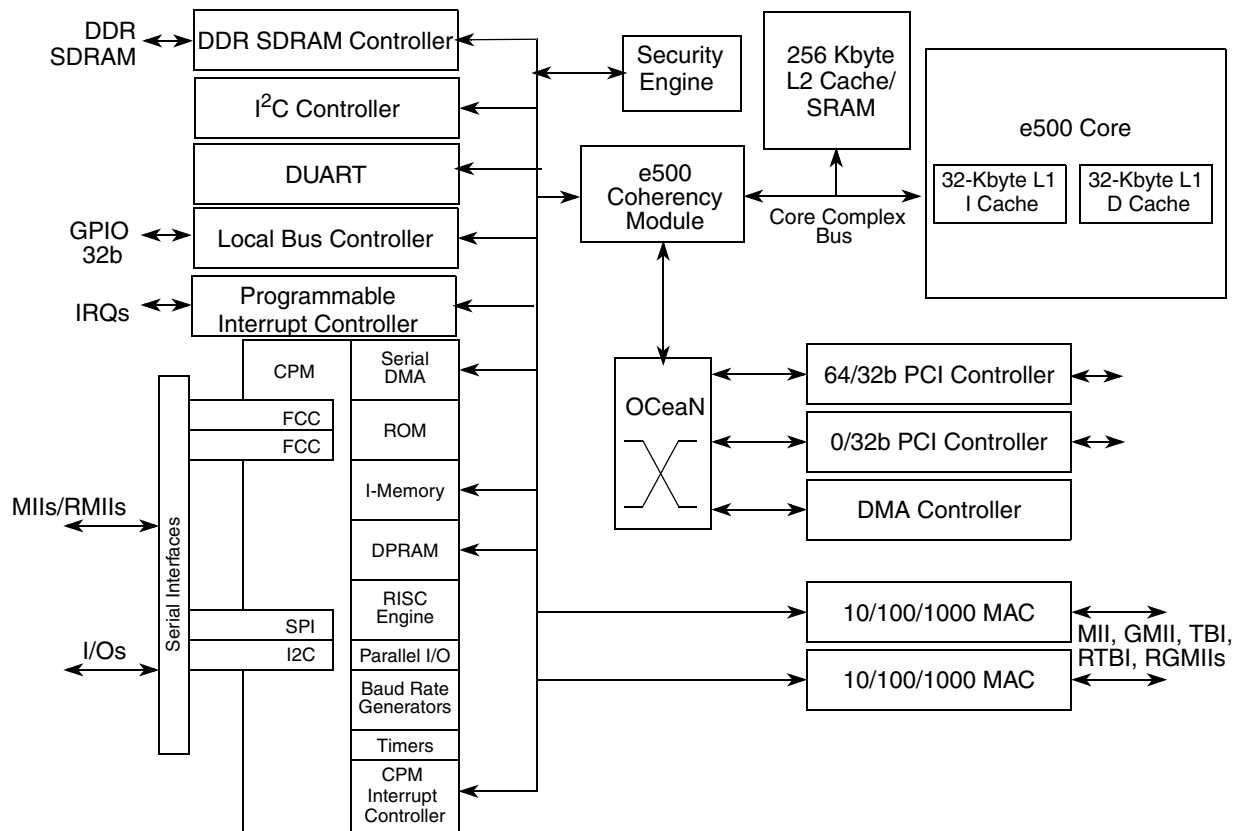


Figure 1. MPC8541E Block Diagram

## 1.1 Key Features

The following lists an overview of the MPC8541E feature set.

- Embedded e500 Book E-compatible core
  - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
  - Dual-issue superscalar, 7-stage pipeline design
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
  - Lockable L1 caches—entire cache or on a per-line basis
  - Separate locking for instructions and data
  - Single-precision floating-point operations
  - Memory management unit especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Dynamic power management
  - Performance monitor facility

- Security Engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i, iSCSI, and IKE processing. The Security Engine contains 4 Crypto-channels, a Controller, and a set of crypto Execution Units (EUs). The Execution Units are:
  - Public Key Execution Unit (PKEU) supporting the following:
    - RSA and Diffie-Hellman
    - Programmable field size up to 2048-bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511-bits
  - Data Encryption Standard Execution Unit (DEU)
    - DES, 3DES
    - Two key (K1, K2) or Three Key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced Encryption Standard Unit (AESU)
    - Implements the Rijndael symmetric key cipher
    - Key lengths of 128, 192, and 256 bits. Two key
    - ECB, CBC, CCM, and Counter modes
  - ARC Four execution unit (AFEU)
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message Digest Execution Unit (MDEU)
    - SHA with 160-bit or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random Number Generator (RNG)
  - 4 Crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 Bytes for each execution unit, with flow control for large data sizes
- High-performance RISC CPM
  - Two full-duplex fast communications controllers (FCCs) that support the following protocol:
    - IEEE802.3/Fast Ethernet (10/100)
  - Serial peripheral interface (SPI) support for master or slave
  - I<sup>2</sup>C bus controller
  - General-purpose parallel ports—16 parallel I/O lines with interrupt capability
- 256 Kbytes of on-chip memory
  - Can act as a 256-Kbyte level-2 cache
  - Can act as a 256-Kbyte or two 128-Kbyte memory-mapped SRAM arrays
  - Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
  - Full ECC support on 64-bit boundary in both cache and SRAM modes

- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
  - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI
    - Four inbound windows
    - Four outbound windows plus default translation for PCI
- DDR memory controller
  - Programmable timing supporting first generation DDR SDRAM
  - 64-bit data interface, up to MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self refresh DDR SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller

- Four global high resolution timers/counters that can generate interrupts
- Supports additional internal interrupt sources
- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- Two I<sup>2</sup>C controllers (one is contained within the CPM, the other is a stand-alone controller which is not part of the CPM)
  - Two-wire interface
  - Multiple master support
  - Master or slave I<sup>2</sup>C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the stand-alone I<sup>2</sup>C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I<sup>2</sup>C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (RXD, TXD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Two Three-speed (10/100/1000)Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z AC compliant controllers
  - Support for Ethernet physical interfaces:
    - 10/100/1000 Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII

- 1000 Mbps IEEE 802.3z TBI
  - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
  - Three-port crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no-snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI Controllers
  - PCI 2.2 compatible
  - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
  - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible

- Selectable hardware-enforced coherency
- Selectable clock source (SYSCLK or independent PCI\_CLK)
- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power save modes: doze, nap, and sleep
  - Employs dynamic power management
  - Selectable clock source (sysclk or independent PCI\_CLK)
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 FC-PBGA package

## 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8541E. The MPC8541E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings** <sup>1</sup>

| Characteristic  |  | Symbol     | Max Value                                    | Unit | Notes |
|---|--|------------|--|------|-------|
| Core supply voltage   |  | $V_{DD}$   | –0.3 to 1.32<br>0.3 to 1.43 (for 1 GHz only) | V    |       |
| PLL supply voltage  |  | $AV_{DD}$  | –0.3 to 1.32<br>0.3 to 1.43 (for 1 GHz only) | V    |       |
| DDR DRAM I/O voltage  |  | $GV_{DD}$  | –0.3 to 3.63                                 | V    |       |
| Three-speed Ethernet I/O, MII management voltage  |  | $LV_{DD}$  | –0.3 to 3.63<br>–0.3 to 2.75                 | V    |       |
| CPM, PCI, local bus, DUART, system control and power management, I <sup>2</sup> C, and JTAG I/O voltage |  | $OV_{DD}$  | –0.3 to 3.63                                 | V    | 3     |
| Input voltage   | DDR DRAM signals   | $MV_{IN}$  | –0.3 to ( $GV_{DD} + 0.3$ )                  | V    | 2, 5  |
|   | DDR DRAM reference   | $MV_{REF}$ | –0.3 to ( $GV_{DD} + 0.3$ )                  | V    | 2, 5  |
|   | Three-speed Ethernet signals   | $LV_{IN}$  | –0.3 to ( $LV_{DD} + 0.3$ )                  | V    | 4, 5  |
|   | CPM, Local bus, DUART, SYSCLK, system control and power management, I <sup>2</sup> C, and JTAG signals | $OV_{IN}$  | –0.3 to ( $OV_{DD} + 0.3$ ) <sup>1</sup>     | V    | 5     |
|   | PCI  | $OV_{IN}$  | –0.3 to ( $OV_{DD} + 0.3$ )                  | V    | 6     |
| Storage temperature range   |  | $T_{STG}$  | –55 to 150                                   | °C   |       |

**Notes:**

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:**  $MV_{IN}$  must not exceed  $GV_{DD}$  by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:**  $OV_{IN}$  must not exceed  $OV_{DD}$  by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:**  $LV_{IN}$  must not exceed  $LV_{DD}$  by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (M,L,O) $V_{IN}$  and  $MV_{REF}$  may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- $OV_{IN}$  on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.



## 2.1.2 Power Sequencing

The MPC8541E requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1.  $V_{DD}$ ,  $AV_{DDn}$
2.  $GV_{DD}$ ,  $LV_{DD}$ ,  $OV_{DD}$  (I/O supplies)

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

### NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay will not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

### NOTE

From a system standpoint, if the I/O power supplies ramp prior to the VDD core supply, the I/Os on the MPC8541E may drive a logic one or zero during power-up.

## 2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8541E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

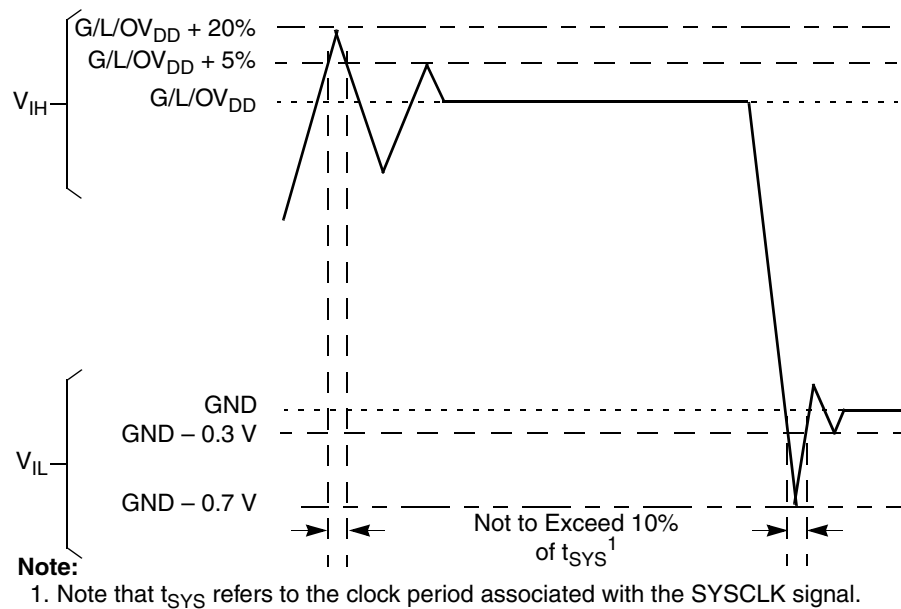
**Table 2. Recommended Operating Conditions**

| Characteristic   | Symbol    | Recommended Value                                       | Unit |
|--|-----------|---|------|
| Core supply voltage  | $V_{DD}$  | 1.2 V $\pm$ 60 mV<br>1.3 V $\pm$ 50 mV (for 1 GHz only) | V    |
| PLL supply voltage   | $AV_{DD}$ | 1.2 V $\pm$ 60 mV<br>1.3 V $\pm$ 50 mV (for 1 GHz only) | V    |
| DDR DRAM I/O voltage   | $GV_{DD}$ | 2.5 V $\pm$ 125 mV                                      | V    |
| Three-speed Ethernet I/O voltage   | $LV_{DD}$ | 3.3 V $\pm$ 165 mV<br>2.5 V $\pm$ 125 mV                | V    |
| PCI, local bus, DUART, system control and power management, I <sup>2</sup> C, and JTAG I/O voltage | $OV_{DD}$ | 3.3 V $\pm$ 165 mV                                      | V    |

Table 2. Recommended Operating Conditions (continued)

| Characteristic           |  | Symbol     | Recommended Value | Unit |
|--------------------------|--|------------|-------------------|------|
| Input voltage            | DDR DRAM signals   | $MV_{IN}$  | GND to $GV_{DD}$  | V    |
|                          | DDR DRAM reference   | $MV_{REF}$ | GND to $GV_{DD}$  | V    |
|                          | Three-speed Ethernet signals   | $LV_{IN}$  | GND to $LV_{DD}$  | V    |
|                          | PCI, local bus, DUART, SYSCLK, system control and power management, I <sup>2</sup> C, and JTAG signals | $OV_{IN}$  | GND to $OV_{DD}$  | V    |
| Die-junction Temperature |  | $T_j$      | 0 to 105          | °C   |

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8541E.

Figure 2. Overshoot/Undershoot Voltage for  $GV_{DD}/OV_{DD}/LV_{DD}$ 

The MPC8541E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage.  $OV_{DD}$  and  $LV_{DD}$  based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied  $MV_{REF}$  signal (nominally set to  $GV_{DD}/2$ ) as is appropriate for the SSTL2 electrical signaling standard.

## 2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type                           | Programmable Output Impedance ( $\Omega$ ) | Supply Voltage               | Notes |
|---------------------------------------|--|------------------------------|-------|
| Local bus interface utilities signals | 25   | $OV_{DD} = 3.3\text{ V}$     | 1     |
|                                       | 42 (default)                               |                              |       |
| PCI signals                           | 25   |                              | 2     |
|                                       | 42 (default)                               |                              |       |
| DDR signal                            | 20   | $GV_{DD} = 2.5\text{ V}$     |       |
| TSEC/10/100 signals                   | 42   | $LV_{DD} = 2.5/3.3\text{ V}$ |       |
| DUART, system control, I2C, JTAG      | 42   | $OV_{DD} = 3.3\text{ V}$     |       |

**Notes:**

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the PCI interface is determined by the setting of the PCI\_GNT1 signal at reset.

## 3 Power Characteristics

The estimated typical power dissipation for this family of PowerQUICC III devices is shown in Table 4.

**Table 4. Power Dissipation<sup>(1) (2)</sup>**

| CCB Frequency (MHz) | Core Frequency (MHz) | $V_{DD}$ | Typical Power <sup>(3)(4)</sup> (W) | Maximum Power <sup>(5)</sup> (W) |
|---------------------|----------------------|----------|-------------------------------------|----------------------------------|
| 200                 | 400                  | 1.2      | 4.4                                 | 6.1                              |
|                     | 500                  | 1.2      | 4.7                                 | 6.5                              |
|                     | 600                  | 1.2      | 5.0                                 | 6.8                              |
| 267                 | 533                  | 1.2      | 4.9                                 | 6.7                              |
|                     | 667                  | 1.2      | 5.4                                 | 7.2                              |
|                     | 800                  | 1.2      | 5.8                                 | 8.6                              |
| 333                 | 667                  | 1.2      | 5.5                                 | 7.4                              |
|                     | 833                  | 1.2      | 6.0                                 | 8.8                              |
|                     | 1000 <sup>(6)</sup>  | 1.3      | 9.0                                 | 12.2                             |

**Notes:**

1. The values do not include I/O supply power ( $OV_{DD}$ ,  $LV_{DD}$ ,  $GV_{DD}$ ) or  $AV_{DD}$ .
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 degrees junction temperature is not exceeded on this device.

## Power Characteristics

3. Typical power is based on a nominal voltage of  $V_{DD} = 1.2V$ , a nominal process, a junction temperature of  $T_j = 105^\circ C$ , and a Dhrystone 2.1 benchmark application.
4. Thermal solutions will likely need to design to a value higher than Typical Power based on the end application,  $T_A$  target, and I/O power.
5. Maximum power is based on a nominal voltage of  $V_{DD} = 1.2V$ , worst case process, a junction temperature of  $T_j = 105^\circ C$ , and an artificial smoke test.
6. The nominal recommended  $V_{DD} = 1.3V$  for this speed grade.

**Table 5. Typical I/O Power Dissipation**

| Interface     | Parameters    | GVDD<br>(2.5V) | OVDD<br>(3.3V) | LVDD<br>(3.3V) | LVDD<br>(2.5V) | Unit | Comments                               |
|---------------|---------------|----------------|----------------|----------------|----------------|------|--|
| DDR I/O       | CCB = 200 MHz | 0.46           |                |                |                | W    | —                                      |
|               | CCB = 266 Mhz | 0.59           |                |                |                | W    | —                                      |
|               | CCB = 300 Mhz | 0.66           |                |                |                | W    | —                                      |
|               | CCB = 333 Mhz | 0.73           |                |                |                | W    | —                                      |
| PCI I/O       | 64b, 66Mhz    |                | 0.14           |                |                | W    | —                                      |
|               | 64b, 33Mhz    |                | 0.08           |                |                | W    | —                                      |
|               | 32b, 66Mhz    |                | 0.07           |                |                | W    | Multiply by 2 if using two 32b ports   |
|               | 32b, 33Mhz    |                | 0.04           |                |                | W    |  |
| Local Bus I/O | 32b, 167Mhz   |                | 0.30           |                |                | W    | —                                      |
|               | 32b, 133Mhz   |                | 0.24           |                |                | W    | —                                      |
|               | 32b, 83Mhz    |                | 0.16           |                |                | W    |  |
|               | 32b, 66Mhz    |                | 0.13           |                |                | W    | —                                      |
|               | 32b, 33Mhz    |                | 0.07           |                |                | W    | —                                      |
| TSEC I/O      | MII           |                |                | 0.01           |                | W    | Multiply by number of interfaces used. |
|               | GMII or TBI   |                |                | 0.07           |                | W    |  |
|               | RGMII or RTBI |                |                |                | 0.04           | W    |  |
| CPM - FCC     | MII           |                | 0.015          |                |                | W    | —                                      |
|               | RMII          |                | 0.013          |                |                | W    | —                                      |
|               | HDLC 16 Mbps  |                | 0.009          |                |                | W    | —                                      |

## 4 Clock Timing

### 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8541E.

**Table 6. SYSCLK AC Timing Specifications**

| Parameter/Condition       | Symbol                             | Min | Typical | Max     | Unit | Notes |
|---------------------------|------------------------------------|-----|---------|---------|------|-------|
| SYSCLK frequency          | $f_{\text{SYSCLK}}$                | —   | —       | 166     | MHz  | 1     |
| SYSCLK cycle time         | $t_{\text{SYSCLK}}$                | 6.0 | —       | —       | ns   | —     |
| SYSCLK rise and fall time | $t_{\text{KH}}, t_{\text{KL}}$     | 0.6 | 1.0     | 1.2     | ns   | 2     |
| SYSCLK duty cycle         | $t_{\text{KHK}}/t_{\text{SYSCLK}}$ | 40  | —       | 60      | %    | 3     |
| SYSCLK jitter             | —                                  | —   | —       | +/- 150 | ps   | 4, 5  |

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- For spread spectrum clocking, guidelines are +/-1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

### 4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC\_GTX\_CLK125) AC timing specifications for the MPC8541E.

**Table 7. EC\_GTX\_CLK125 AC Timing Specifications**

| Parameter/Condition                                  | Symbol                             | Min      | Typical | Max      | Unit | Notes |
|--|------------------------------------|----------|---------|----------|------|-------|
| EC_GTX_CLK125 frequency                              | $f_{\text{G125}}$                  | —        | 125     | —        | MHz  |       |
| EC_GTX_CLK125 cycle time                             | $t_{\text{G125}}$                  | —        | 8       | —        | ns   |       |
| EC_GTX_CLK125 rise time                              | $t_{\text{G125R}}$                 | —        | —       | 1.0      | ns   | 1     |
| EC_GTX_CLK125 fall time                              | $t_{\text{G125F}}$                 | —        | —       | 1.0      | ns   | 1     |
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>RGMII, RTBI | $t_{\text{G125H}}/t_{\text{G125}}$ | 45<br>47 | —       | 55<br>53 | %    | 1, 2  |

**Notes:**

- Timing is guaranteed by design and characterization.
- EC\_GTX\_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC\_GTX\_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX\_CLK of TSEC.

## 4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

**Table 8. RTC AC Timing Specifications**

| Parameter/Condition | Symbol     | Min                | Typical | Max | Unit | Notes |
|---------------------|------------|--------------------|---------|-----|------|-------|
| RTC clock high time | $t_{RTCH}$ | 2 x $t_{CCB\_CLK}$ | —       | —   | ns   |       |
| RTC clock low time  | $t_{RTCL}$ | 2 x $t_{CCB\_CLK}$ | —       | —   | ns   |       |

## 5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8541E. Table 9 provides the RESET initialization AC timing specifications.

**Table 9. RESET Initialization Timing Specifications**

| Parameter/Condition  | Min | Max | Unit    | Notes |
|--|-----|-----|---------|-------|
| Required assertion time of $\overline{HRESET}$   | 100 | —   | $\mu s$ |       |
| Minimum assertion time for $\overline{SRESET}$   | 512 | —   | SYSCLKs | 1     |
| PLL input setup time with stable SYSCLK before $\overline{HRESET}$ negation  | 100 | —   | $\mu s$ |       |
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{HRESET}$             | 4   | —   | SYSCLKs | 1     |
| Input hold time for POR configs (including PLL config) with respect to negation of $\overline{HRESET}$               | 2   | —   | SYSCLKs | 1     |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{HRESET}$ | —   | 5   | SYSCLKs | 1     |

**Notes:**

1. SYSCLK is identical to the PCI\_CLK signal and is the primary clock input for the MPC8541E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

**Table 10. PLL and DLL Lock Times**

| Parameter/Condition | Min  | Max     | Unit       | Notes |
|---------------------|------|---------|------------|-------|
| PLL lock times      | —    | 100     | $\mu s$    |       |
| DLL lock times      | 7680 | 122,880 | CCB Clocks | 1, 2  |

**Notes:**

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the  $SYSCLK \times \text{platform PLL ratio}$ .

## 6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8541E.

### 6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8541E.

**Table 11. DDR SDRAM DC Electrical Characteristics**

| Parameter/Condition                       | Symbol     | Min                   | Max                   | Unit    | Notes |
|---|------------|-----------------------|-----------------------|---------|-------|
| I/O supply voltage                        | $GV_{DD}$  | 2.375                 | 2.625                 | V       | 1     |
| I/O reference voltage                     | $MV_{REF}$ | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V       | 2     |
| I/O termination voltage                   | $V_{TT}$   | $MV_{REF} - 0.04$     | $MV_{REF} + 0.04$     | V       | 3     |
| Input high voltage                        | $V_{IH}$   | $MV_{REF} + 0.18$     | $GV_{DD} + 0.3$       | V       |       |
| Input low voltage                         | $V_{IL}$   | -0.3                  | $MV_{REF} - 0.18$     | V       |       |
| Output leakage current                    | $I_{OZ}$   | -10                   | 10                    | $\mu A$ | 4     |
| Output high current ( $V_{OUT} = 1.95$ V) | $I_{OH}$   | -15.2                 | —                     | mA      |       |
| Output low current ( $V_{OUT} = 0.35$ V)  | $I_{OL}$   | 15.2                  | —                     | mA      |       |
| $MV_{REF}$ input leakage current          | $I_{VREF}$ | —                     | 5                     | $\mu A$ |       |

**Notes:**

- $GV_{DD}$  is expected to be within 50 mV of the DRAM  $GV_{DD}$  at all times.
- $MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed  $\pm 2\%$  of the DC value.
- $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to  $MV_{REF}$ . This rail should track variations in the DC level of  $MV_{REF}$ .
- Output leakage is measured with all outputs disabled,  $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$ .

Table 12 provides the DDR capacitance.

**Table 12. DDR SDRAM Capacitance**

| Parameter/Condition                         | Symbol    | Min | Max | Unit | Notes |
|---|-----------|-----|-----|------|-------|
| Input/output capacitance: DQ, DQS, MSYNC_IN | $C_{IO}$  | 6   | 8   | pF   | 1     |
| Delta input/output capacitance: DQ, DQS     | $C_{DIO}$ | —   | 0.5 | pF   | 1     |

**Note:**

- This parameter is sampled.  $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$ ,  $f = 1 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak to peak) = 0.2 V.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 13. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions with  $GV_{DD}$  of  $2.5\text{ V} \pm 5\%$ .

| Parameter  | Symbol       | Min               | Max               | Unit | Notes |
|--|--------------|-------------------|-------------------|------|-------|
| AC input low voltage   | $V_{IL}$     | —                 | $MV_{REF} - 0.31$ | V    |       |
| AC input high voltage  | $V_{IH}$     | $MV_{REF} + 0.31$ | $GV_{DD} + 0.3$   | V    |       |
| MDQS—MDQ/MECC input skew per byte<br>For DDR = 333 MHz<br>For DDR $\leq$ 266 MHz | $t_{DISKEW}$ | —                 | 750<br>1125       | ps   | 1     |

**Note:**

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if  $0 \leq n \leq 7$ ) or ECC (MECC[{0...7}] if  $n = 8$ ).

### 6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

**Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode**

At recommended operating conditions with  $GV_{DD}$  of  $2.5\text{ V} \pm 5\%$ .

| Parameter  | Symbol <sup>1</sup> | Min                     | Max               | Unit | Notes |
|--|---------------------|-------------------------|-------------------|------|-------|
| MCK[n] cycle time, (MCK[n]/ $\overline{\text{MCK}}[n]$ crossing)           | $t_{MCK}$           | 6                       | 10                | ns   | 2     |
| Skew between any MCK to ADDR/CMD<br>333 MHz<br>266 MHz<br>200 MHz          | $t_{AOSKEW}$        | -1000<br>-1100<br>-1200 | 200<br>300<br>400 | ps   | 3     |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHAS}$        | 2.8<br>3.45<br>4.6      | —                 | ns   | 4     |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz  | $t_{DDKHAX}$        | 2.0<br>2.65<br>3.8      | —                 | ns   | 4     |
| MCS(n) output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz   | $t_{DDKHCS}$        | 2.8<br>3.45<br>4.6      | —                 | ns   | 4     |



**Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)**At recommended operating conditions with  $GV_{DD}$  of 2.5 V  $\pm$  5%.

| Parameter  | Symbol <sup>1</sup>            | Min                         | Max                         | Unit | Notes |
|--|--------------------------------|-----------------------------|-----------------------------|------|-------|
| $\overline{MCS}(n)$ output hold with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCX}$                   | 2.0<br>2.65<br>3.8          | —                           | ns   | 4     |
| MCK to MDQS<br>333 MHz<br>266 MHz<br>200 MHz   | $t_{DDKMHM}$                   | -0.9<br>-1.1<br>-1.2        | 0.3<br>0.5<br>0.6           | ns   | 5     |
| MDQ/MECC/MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz      | $t_{DDKHDS}$ ,<br>$t_{DDKLDS}$ | 900<br>900<br>1200          | —                           | ps   | 6     |
| MDQ/MECC/MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz       | $t_{DDKHDX}$ ,<br>$t_{DDKLDX}$ | 900<br>900<br>1200          | —                           | ps   | 6     |
| MDQS preamble start  | $t_{DDKHMP}$                   | $-0.5 \times t_{MCK} - 0.9$ | $-0.5 \times t_{MCK} + 0.3$ | ns   | 7     |
| MDQS epilogue end  | $t_{DDKLME}$                   | -0.9                        | 0.3                         | ns   | 7     |

**Notes:**

- The symbols used for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example,  $t_{DDKHAS}$  symbolizes DDR timing (DD) for the time  $t_{MCK}$  memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also,  $t_{DDKLDS}$  symbolizes DDR timing (DD) for the time  $t_{MCK}$  memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{MCK}$  referenced measurements are made from the crossing of the two signals  $\pm 0.1$  V.
- In the source synchronous mode, MCK/ $\overline{MCK}$  can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for  $t_{AOSKEW}$  it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$ ,  $\overline{MCS}$ , and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
- Note that  $t_{DDKMHM}$  follows the symbol conventions described in note 1. For example,  $t_{DDKMHM}$  describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns.  $t_{DDKMHM}$  can be modified through control of the DQSS override bits in the TIMING\_CFG\_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK\_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8541E.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8541E. Note that  $t_{DDKHMP}$  follows the symbol conventions described in note 1.

Figure 3 shows the DDR SDRAM output timing for address skew with respect to any MCK.

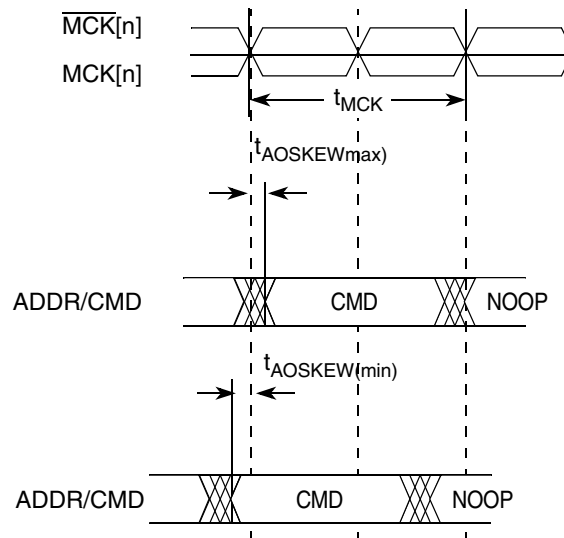


Figure 3. Timing Diagram for  $t_{AOSKEW}$  Measurement

Figure 4 shows the DDR SDRAM output timing diagram for the source synchronous mode.

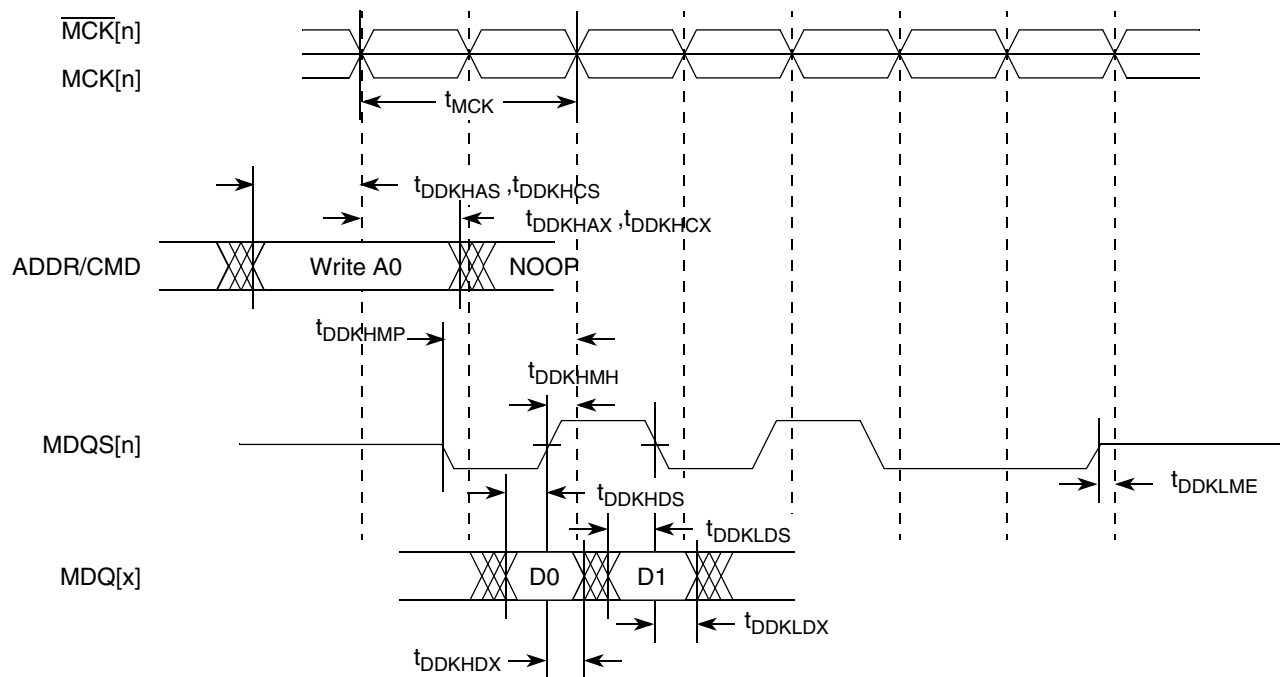


Figure 4. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

Figure 5 provides the AC test load for the DDR bus.

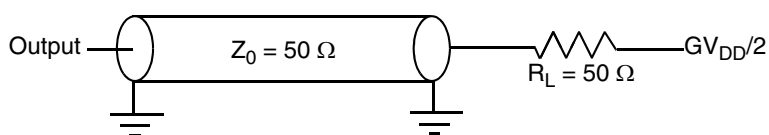


Figure 5. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

| Symbol    | DDR                           | Unit | Notes |
|-----------|-------------------------------|------|-------|
| $V_{TH}$  | $MV_{REF} \pm 0.31 \text{ V}$ | V    | 1     |
| $V_{OUT}$ | $0.5 \times GV_{DD}$          | V    | 2     |

**Notes:**

1. Data input threshold measurement point.
2. Data output measurement point.

## 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8541E.

### 7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8541E.

Table 16. DUART DC Electrical Characteristics

| Parameter                 | Symbol   | Test Condition  | Min             | Max             | Unit          |
|---------------------------|----------|---|-----------------|-----------------|---------------|
| High-level input voltage  | $V_{IH}$ | $V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$ | 2               | $OV_{DD} + 0.3$ | V             |
| Low-level input voltage   | $V_{IL}$ |   | -0.3            | 0.8             | V             |
| Input current             | $I_{IN}$ | $V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$                              | —               | $\pm 5$         | $\mu\text{A}$ |
| High-level output voltage | $V_{OH}$ | $OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$                        | $OV_{DD} - 0.2$ | —               | V             |
| Low-level output voltage  | $V_{OL}$ | $OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$                         | —               | 0.2             | V             |

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8541E.

**Table 17. DUART AC Timing Specifications**

| Parameter         | Value                    | Unit | Notes |
|-------------------|--------------------------|------|-------|
| Minimum baud rate | $f_{CCB\_CLK} / 1048576$ | baud | 3     |
| Maximum baud rate | $f_{CCB\_CLK} / 16$      | baud | 1, 3  |
| Oversample rate   | 16                       | —    | 2, 3  |

**Notes:**

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8<sup>th</sup> sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.
3. Guaranteed by design.

## 8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

### 8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3](#), “Ethernet Management Interface Electrical Characteristics.”

#### 8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 18](#) and [Table 19](#). The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (i.e., a GMII driver powered from a 3.6-V supply driving  $V_{OH}$  into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 18. GMII, MII, and TBI DC Electrical Characteristics

| Parameter            | Symbol    | Conditions                 |                        | Min  | Max             | Unit          |
|----------------------|-----------|----------------------------|------------------------|------|-----------------|---------------|
| Supply voltage 3.3 V | $LV_{DD}$ | —                          |                        | 3.13 | 3.47            | V             |
| Output high voltage  | $V_{OH}$  | $I_{OH} = -4.0 \text{ mA}$ | $LV_{DD} = \text{Min}$ | 2.40 | $LV_{DD} + 0.3$ | V             |
| Output low voltage   | $V_{OL}$  | $I_{OL} = 4.0 \text{ mA}$  | $LV_{DD} = \text{Min}$ | GND  | 0.50            | V             |
| Input high voltage   | $V_{IH}$  | —                          | —                      | 1.70 | $LV_{DD} + 0.3$ | V             |
| Input low voltage    | $V_{IL}$  | —                          | —                      | -0.3 | 0.90            | V             |
| Input high current   | $I_{IH}$  | $V_{IN}^1 = LV_{DD}$       |                        | —    | 40              | $\mu\text{A}$ |
| Input low current    | $I_{IL}$  | $V_{IN}^1 = \text{GND}$    |                        | -600 | —               | $\mu\text{A}$ |

**Note:**

1. The symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

Table 19. GMII, MII, RGMII RTBI, and TBI DC Electrical Characteristics

| Parameters   | Symbol    | Min                | Max             | Unit          |
|--|-----------|--------------------|-----------------|---------------|
| Supply voltage 2.5 V   | $LV_{DD}$ | 2.37               | 2.63            | V             |
| Output high voltage<br>( $LV_{DD} = \text{Min}$ , $I_{OH} = -1.0 \text{ mA}$ ) | $V_{OH}$  | 2.00               | $LV_{DD} + 0.3$ | V             |
| Output low voltage<br>( $LV_{DD} = \text{Min}$ , $I_{OL} = 1.0 \text{ mA}$ )   | $V_{OL}$  | $\text{GND} - 0.3$ | 0.40            | V             |
| Input high voltage<br>( $LV_{DD} = \text{Min}$ )                               | $V_{IH}$  | 1.70               | $LV_{DD} + 0.3$ | V             |
| Input low voltage<br>( $LV_{DD} = \text{Min}$ )                                | $V_{IL}$  | -0.3               | 0.70            | V             |
| Input high current<br>( $V_{IN}^1 = LV_{DD}$ )                                 | $I_{IH}$  | —                  | 10              | $\mu\text{A}$ |
| Input low current<br>( $V_{IN}^1 = \text{GND}$ )                               | $I_{IL}$  | -15                | —               | $\mu\text{A}$ |

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

## 8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

**Table 20. GMII Transmit AC Timing Specifications**

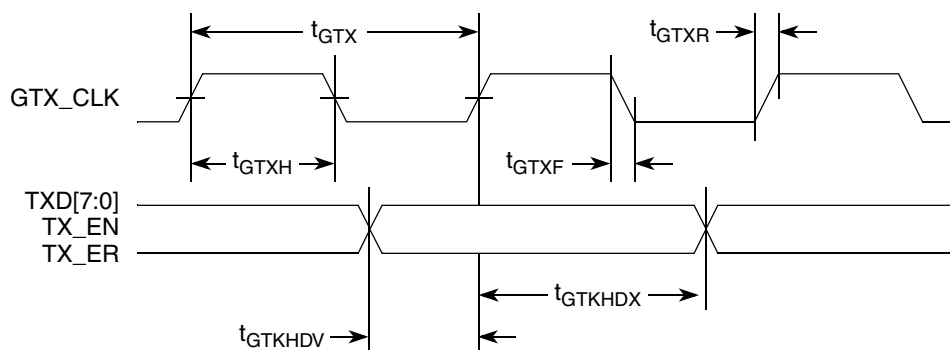
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

| Parameter/Condition                               | Symbol <sup>1</sup>          | Min | Typ | Max | Unit |
|---|------------------------------|-----|-----|-----|------|
| GTX_CLK clock period                              | $t_{GTX}$                    | —   | 8.0 | —   | ns   |
| GTX_CLK duty cycle                                | $t_{GTXH}/t_{GTX}$           | 40  | —   | 60  | %    |
| GMII data TXD[7:0], TX_ER, TX_EN setup time       | $t_{GTKHDV}$                 | 2.5 | —   | —   | ns   |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$                 | 0.5 | —   | 5.0 | ns   |
| GTX_CLK data clock rise and fall times            | $t_{GTXR}^3, t_{GTXF}^{2,4}$ | —   | —   | 1.0 | ns   |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GTKHDV}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also,  $t_{GTKHDX}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GTX}$  represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 6 shows the GMII transmit AC timing diagram.



**Figure 6. GMII Transmit AC Timing Diagram**

### 8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

**Table 21. GMII Receive AC Timing Specifications**

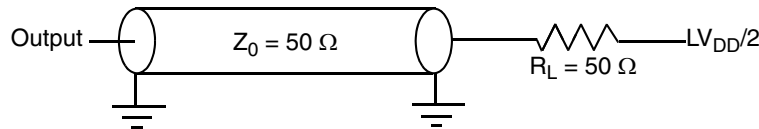
At recommended operating conditions with  $LV_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

| Parameter/Condition                         | Symbol <sup>1</sup>                    | Min | Typ | Max | Unit |
|---|--|-----|-----|-----|------|
| RX_CLK clock period                         | $t_{GRX}$                              | —   | 8.0 | —   | ns   |
| RX_CLK duty cycle                           | $t_{GRXH}/t_{GRX}$                     | 40  | —   | 60  | %    |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$                           | 2.0 | —   | —   | ns   |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK  | $t_{GRDXKH}$                           | 0.5 | —   | —   | ns   |
| RX_CLK clock rise and fall time             | $t_{GRXR}$ , $t_{GRXF}$ <sup>2,3</sup> | —   | —   | 1.0 | ns   |

**Note:**

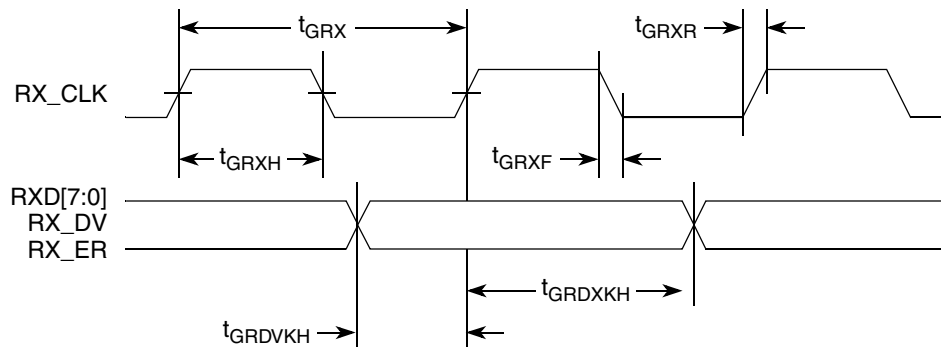
- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GRDVKH}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{RX}$  clock reference (K) going to the high state (H) or setup time. Also,  $t_{GRDXKL}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{GRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GRX}$  represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 7 provides the AC test load for TSEC.



**Figure 7. TSEC AC Test Load**

Figure 8 shows the GMII receive AC timing diagram.



**Figure 8. GMII Receive AC Timing Diagram**

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

**Table 22. MII Transmit AC Timing Specifications**

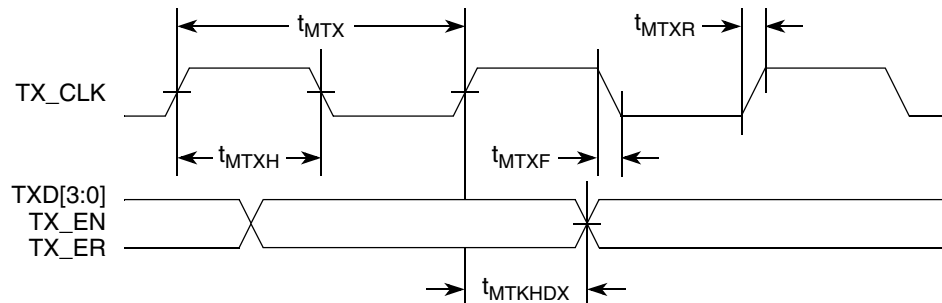
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

| Parameter/Condition                             | Symbol <sup>1</sup>           | Min | Typ | Max | Unit |
|---|-------------------------------|-----|-----|-----|------|
| TX_CLK clock period 10 Mbps                     | $t_{MTX}^2$                   | —   | 400 | —   | ns   |
| TX_CLK clock period 100 Mbps                    | $t_{MTX}$                     | —   | 40  | —   | ns   |
| TX_CLK duty cycle                               | $t_{MTXH}/t_{MTX}$            | 35  | —   | 65  | %    |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$                  | 1   | 5   | 15  | ns   |
| TX_CLK data clock rise and fall time            | $t_{MTXR}$ , $t_{MTXF}^{2,3}$ | 1.0 | —   | 4.0 | ns   |

**Notes:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MTKHDX}$  symbolizes MII transmit timing (MT) for the time  $t_{MTX}$  clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of  $t_{MTX}$  represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 9 shows the MII transmit AC timing diagram.



**Figure 9. MII Transmit AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

Table 23 provides the MII receive AC timing specifications.



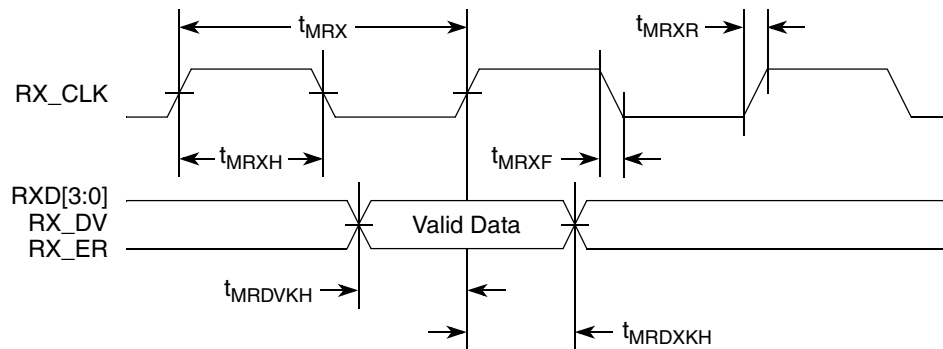
**Table 23. MII Receive AC Timing Specifications**At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

| Parameter/Condition                         | Symbol <sup>1</sup>        | Min  | Typ | Max | Unit |
|---|----------------------------|------|-----|-----|------|
| RX_CLK clock period 10 Mbps                 | $t_{MRX}^2$                | —    | 400 | —   | ns   |
| RX_CLK clock period 100 Mbps                | $t_{MRX}$                  | —    | 40  | —   | ns   |
| RX_CLK duty cycle                           | $t_{MRXH}/t_{MRX}$         | 35   | —   | 65  | %    |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$               | 10.0 | —   | —   | ns   |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK  | $t_{MRDXKH}$               | 10.0 | —   | —   | ns   |
| RX_CLK clock rise and fall time             | $t_{MRXR}, t_{MRXF}^{2,3}$ | 1.0  | —   | 4.0 | ns   |

**Notes:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MRDVKH}$  symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MRX}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{MRDXKL}$  symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{MRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{MRX}$  represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 10 shows the MII receive AC timing diagram.

**Figure 10. MII Receive AC Timing Diagram**

## 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

**Table 24. TBI Transmit AC Timing Specifications**

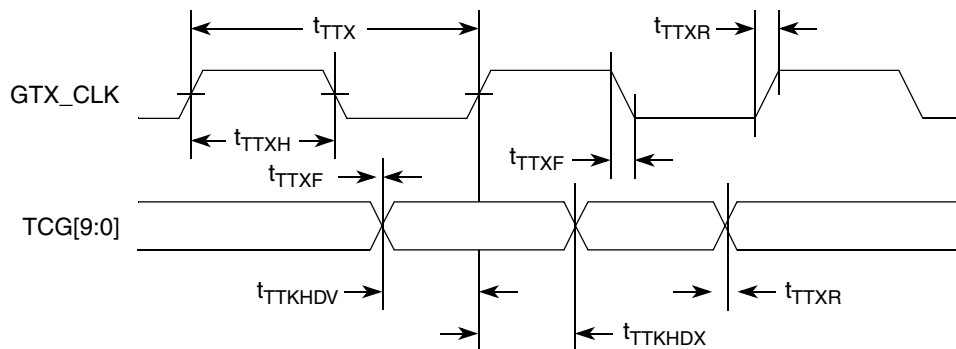
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

| Parameter/Condition   | Symbol <sup>1</sup>           | Min | Typ | Max | Unit |
|---|-------------------------------|-----|-----|-----|------|
| GTX_CLK clock period  | $t_{TTX}$                     | —   | 8.0 | —   | ns   |
| GTX_CLK duty cycle  | $t_{TTXH}/t_{TTX}$            | 40  | —   | 60  | %    |
| GMII data TCG[9:0], TX_ER, TX_EN setup time<br>GTX_CLK going high     | $t_{TTKHDTV}$                 | 2.0 | —   | —   | ns   |
| GMII data TCG[9:0], TX_ER, TX_EN hold time from<br>GTX_CLK going high | $t_{TTKHDX}$                  | 1.0 | —   | —   | ns   |
| GTX_CLK clock rise and fall time                                      | $t_{TTXR}$ , $t_{TTXF}^{2,3}$ | —   | —   | 1.0 | ns   |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{TTKHDTV}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also,  $t_{TTKHDX}$  symbolizes the TBI transmit timing (TT) with respect to the time from  $t_{TTX}$  (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{TTX}$  represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 11 shows the TBI transmit AC timing diagram.



**Figure 11. TBI Transmit AC Timing Diagram**

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 25 provides the TBI receive AC timing specifications.

**Table 25. TBI Receive AC Timing Specifications**

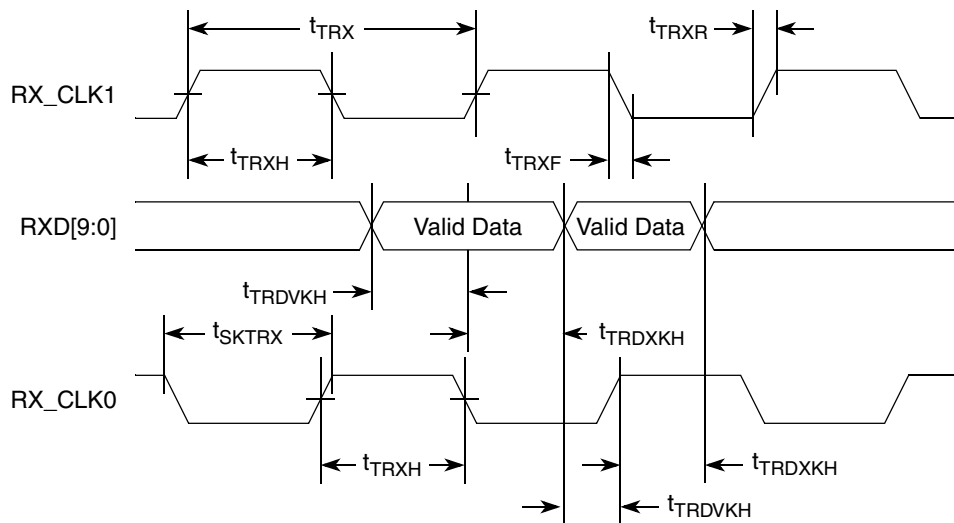
At recommended operating conditions with  $V_{DD}$  of 3.3 V  $\pm$  5%.

| Parameter/Condition                  | Symbol <sup>1</sup>                    | Min | Typ  | Max | Unit |
|--------------------------------------|--|-----|------|-----|------|
| RX_CLK clock period                  | $t_{TRX}$                              |     | 16.0 |     | ns   |
| RX_CLK skew                          | $t_{SKTRX}$                            | 7.5 | —    | 8.5 | ns   |
| RX_CLK duty cycle                    | $t_{TRXH}/t_{TRX}$                     | 40  | —    | 60  | %    |
| RCG[9:0] setup time to rising RX_CLK | $t_{TRDVKH}$                           | 2.5 | —    | —   | ns   |
| RCG[9:0] hold time to rising RX_CLK  | $t_{TRDXKH}$                           | 1.5 | —    | —   | ns   |
| RX_CLK clock rise time and fall time | $t_{TRXR}$ , $t_{TRXF}$ <sup>2,3</sup> | 0.7 | —    | 2.4 | ns   |

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{TRDVKH}$  symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{TRX}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{TRDXKH}$  symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{TRX}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{TRX}$  represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

Figure 12 shows the TBI receive AC timing diagram.



**Figure 12. TBI Receive AC Timing Diagram**

## 8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

**Table 26. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with  $LV_{DD}$  of 2.5 V  $\pm$  5%.

| Parameter/Condition                                 | Symbol <sup>1</sup>              | Min  | Typ | Max  | Unit |
|---|----------------------------------|------|-----|------|------|
| Data to clock output skew (at transmitter)          | $t_{SKRGT}^{5}$                  | –500 | 0   | 500  | ps   |
| Data to clock input skew (at receiver) <sup>2</sup> | $t_{SKRGT}$                      | 1.0  | —   | 2.8  | ns   |
| Clock cycle duration <sup>3</sup>                   | $t_{RGT}^{6}$                    | 7.2  | 8.0 | 8.8  | ns   |
| Duty cycle for 1000Base-T <sup>4</sup>              | $t_{RGTH}/t_{RGT}^{6}$           | 45   | 50  | 55   | %    |
| Duty cycle for 10BASE-T and 100BASE-TX <sup>3</sup> | $t_{RGTH}/t_{RGT}^{6}$           | 40   | 50  | 60   | %    |
| Rise and fall times                                 | $t_{RGTR}^{6,7}, t_{RGTF}^{6,7}$ | —    | —   | 0.75 | ns   |

**Notes:**

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of  $t_{RGT}$  represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX\_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
- For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns  $\pm$  40 ns and 40 ns  $\pm$  4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{RGT}$  of the lowest speed transitioned between.
- Guaranteed by characterization.
- Guaranteed by design.
- Signal timings are measured at 0.5 V and 2.0 V voltage levels.

Figure 13 shows the RBMII and RTBI AC timing and multiplexing diagrams.

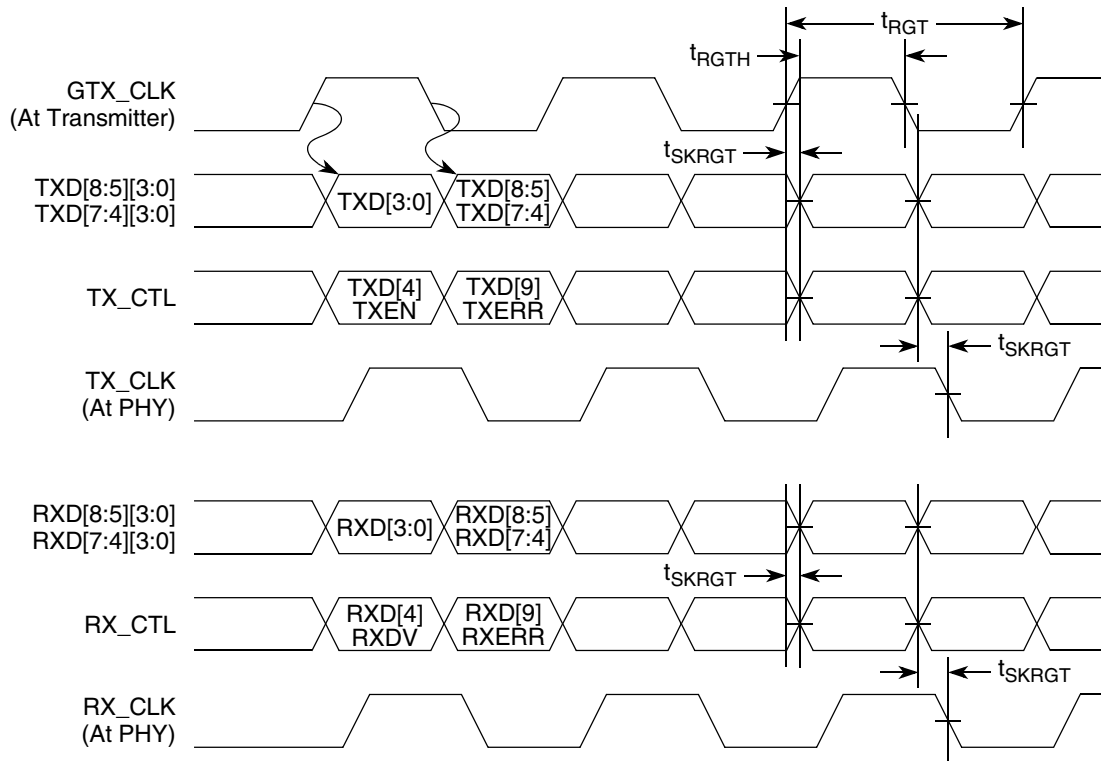


Figure 13. RGMII and RTBI AC Timing and Multiplexing Diagrams

## 8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 8.1, “Three-Speed Ethernet Controller \(TSEC\) \(10/100/1000 Mbps\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

### 8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics

| Parameter              | Symbol    | Conditions                 |                        | Min  | Max             | Unit |
|------------------------|-----------|----------------------------|------------------------|------|-----------------|------|
| Supply voltage (3.3 V) | $OV_{DD}$ | —                          |                        | 3.13 | 3.47            | V    |
| Output high voltage    | $V_{OH}$  | $I_{OH} = -1.0 \text{ mA}$ | $LV_{DD} = \text{Min}$ | 2.10 | $LV_{DD} + 0.3$ | V    |
| Output low voltage     | $V_{OL}$  | $I_{OL} = 1.0 \text{ mA}$  | $LV_{DD} = \text{Min}$ | GND  | 0.50            | V    |
| Input high voltage     | $V_{IH}$  | —                          |                        | 1.70 | —               | V    |
| Input low voltage      | $V_{IL}$  | —                          |                        | —    | 0.90            | V    |

Table 27. MII Management DC Electrical Characteristics (continued)

| Parameter          | Symbol   | Conditions             |                            | Min  | Max | Unit          |
|--------------------|----------|------------------------|----------------------------|------|-----|---------------|
| Input high current | $I_{IH}$ | $LV_{DD} = \text{Max}$ | $V_{IN}^1 = 2.1 \text{ V}$ | —    | 40  | $\mu\text{A}$ |
| Input low current  | $I_{IL}$ | $LV_{DD} = \text{Max}$ | $V_{IN} = 0.5 \text{ V}$   | −600 | —   | $\mu\text{A}$ |

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in [Table 1](#) and [Table 2](#).

## 8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with  $LV_{DD}$  is  $3.3 \text{ V} \pm 5\%$ .

| Parameter/Condition        | Symbol <sup>1</sup> | Min   | Typ | Max                        | Unit | Notes |
|----------------------------|---------------------|-------|-----|----------------------------|------|-------|
| MDC frequency              | $f_{MDC}$           | 0.893 | —   | 10.4                       | MHz  | 2     |
| MDC period                 | $t_{MDC}$           | 96    | —   | 1120                       | ns   |       |
| MDC clock pulse width high | $t_{MDCH}$          | 32    | —   | —                          | ns   |       |
| MDC to MDIO valid          | $t_{MDKHDV}$        |       |     | $2 * [1/(f_{ccb\_clk}/8)]$ | ns   | 3     |
| MDC to MDIO delay          | $t_{MDKHDX}$        | 10    | —   | $2 * [1/(f_{ccb\_clk}/8)]$ | ns   | 3     |
| MDIO to MDC setup time     | $t_{MDDVKH}$        | 5     | —   | —                          | ns   |       |
| MDIO to MDC hold time      | $t_{MDDXKH}$        | 0     | —   | —                          | ns   |       |
| MDC rise time              | $t_{MDCR}$          | —     | —   | 10                         | ns   |       |
| MDC fall time              | $t_{MDHF}$          | —     | —   | 10                         | ns   |       |

**Notes:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{MDKHDX}$  symbolizes management data timing (MD) for the time  $t_{MDC}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{MDDVKH}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MDC}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

Figure 14 shows the MII management AC timing diagram.

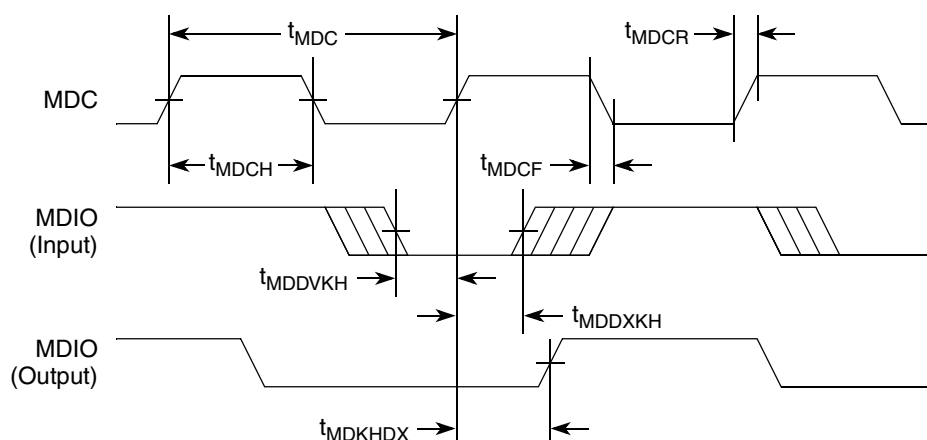


Figure 14. MII Management Interface Timing Diagram

## 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8541E.

### 9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

| Parameter                 | Symbol   | Test Condition  | Min             | Max             | Unit          |
|---------------------------|----------|---|-----------------|-----------------|---------------|
| High-level input voltage  | $V_{IH}$ | $V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$ | 2               | $OV_{DD} + 0.3$ | V             |
| Low-level input voltage   | $V_{IL}$ |   | -0.3            | 0.8             | V             |
| Input current             | $I_{IN}$ | $V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$                              | —               | $\pm 5$         | $\mu\text{A}$ |
| High-level output voltage | $V_{OH}$ | $OV_{DD} = \text{min, } I_{OH} = -2\text{mA}$                             | $OV_{DD} - 0.2$ | —               | V             |
| Low-level output voltage  | $V_{OL}$ | $OV_{DD} = \text{min, } I_{OL} = 2\text{mA}$                              | —               | 0.2             | V             |

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

## 9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL enabled.

**Table 30. Local Bus General Timing Parameters - DLL Enabled**

| Parameter   | Configuration <sup>7</sup>           | Symbol <sup>1</sup> | Min | Max | Unit | Notes   |
|---|--------------------------------------|---------------------|-----|-----|------|---------|
| Local bus cycle time  |                                      | $t_{LBK}$           | 6.0 | —   | ns   | 2       |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT                                  |                                      | $t_{LBKSKEW}$       | —   | 150 | ps   | 7, 9    |
| Input setup to local bus clock (except LUPWAIT)                       |                                      | $t_{LBIVKH1}$       | 1.8 | —   | ns   | 3, 4, 8 |
| LUPWAIT input setup to local bus clock                                |                                      | $t_{LBIVKH2}$       | 1.7 | —   | ns   | 3, 4    |
| Input hold from local bus clock (except LUPWAIT)                      |                                      | $t_{LBIXKH1}$       | 0.5 | —   | ns   | 3, 4, 8 |
| LUPWAIT input hold from local bus clock                               |                                      | $t_{LBIXKH2}$       | 1.0 | —   | ns   | 3, 4    |
| LALE output transition to LAD/LDP output transition (LATCH hold time) |                                      | $t_{LBOTOT}$        | 1.5 | —   | ns   | 6       |
| Local bus clock to output valid (except LAD/LDP and LALE)             | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOV1}$       | —   | 2.3 | ns   | 3, 8    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     |     | 3.8 |      |         |
| Local bus clock to data valid for LAD/LDP                             | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOV2}$       | —   | 2.5 | ns   | 3, 8    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     |     | 4.0 |      |         |
| Local bus clock to address valid for LAD                              | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOV3}$       | —   | 2.6 | ns   | 3, 8    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     |     | 4.1 |      |         |
| Output hold from local bus clock (except LAD/LDP and LALE)            | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOX1}$       | 0.7 | —   | ns   | 3, 8    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     | 1.6 |     |      |         |
| Output hold from local bus clock for LAD/LDP                          | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOX2}$       | 0.7 | —   | ns   | 3, 8    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     | 1.6 |     |      |         |
| Local bus clock to output high Impedance (except LAD/LDP and LALE)    | $\overline{LWE}[0:1] = 00$           | $t_{LBKHOZ1}$       | —   | 2.8 | ns   | 5, 9    |
|   | $\overline{LWE}[0:1] = 11$ (default) |                     |     | 4.2 |      |         |



**Table 30. Local Bus General Timing Parameters - DLL Enabled (continued)**

| Parameter  | Configuration <sup>7</sup>                  | Symbol <sup>1</sup>  | Min | Max | Unit | Notes |
|--|---|----------------------|-----|-----|------|-------|
| Local bus clock to output high impedance for LAD/LDP | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKHOZ2}}$ | —   | 2.8 | ns   | 5, 9  |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |     | 4.2 |      |       |

Notes:

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})}$  (reference)(state) for inputs and  $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{\text{LBIXKH1}}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{\text{LBK}}$  clock reference (K) goes high (H), in this case for clock one(1). Also,  $t_{\text{LBKHOX}}$  symbolizes local bus timing (LB) for the  $t_{\text{LBK}}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC\_IN for DLL enabled mode.
- All signals are measured from  $\text{OV}_{\text{DD}}/2$  of the rising edge of LSYNC\_IN for DLL enabled to  $0.4 \times \text{OV}_{\text{DD}}$  of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- The value of  $t_{\text{LBOTOT}}$  is defined as the sum of 1/2 or 1 ccb\_clk cycle as programmed by  $\text{LBCR}[\text{AHD}]$ , and the number of local bus buffer delays used as programmed at power-on reset with configuration pins  $\overline{\text{LWE}}[0:1]$ .
- Maximum possible clock skew between a clock  $\text{LCLK}[m]$  and a relative clock  $\text{LCLK}[n]$ . Skew measured between complementary signals at  $\text{OV}_{\text{DD}}/2$ .
- Guaranteed by characterization.
- Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8541E with the DLL bypassed.

**Table 31. Local Bus General Timing Parameters - DLL Bypassed**

| Parameter  | Configuration <sup>7</sup>                  | Symbol <sup>1</sup>  | Min  | Max | Unit | Notes |
|--|---|----------------------|------|-----|------|-------|
| Local bus cycle time   |   | $t_{\text{LBK}}$     | 6.0  | —   | ns   | 2     |
| Internal launch/capture clock to LCLK delay                          |   | $t_{\text{LBKHK1}}$  | 1.8  | 3.4 | ns   | 8     |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT                                 |   | $t_{\text{LBKSKEW}}$ | —    | 150 | ps   | 7, 9  |
| Input setup to local bus clock (except LUPWAIT)                      |   | $t_{\text{LBIVKH1}}$ | 5.2  | —   | ns   | 3, 4  |
| LUPWAIT input setup to local bus clock                               |   | $t_{\text{LBIVKH2}}$ | 5.1  | —   | ns   | 3, 4  |
| Input hold from local bus clock (except LUPWAIT)                     |   | $t_{\text{LBIXKH1}}$ | -1.3 | —   | ns   | 3, 4  |
| LUPWAIT input hold from local bus clock                              |   | $t_{\text{LBIXKH2}}$ | -0.8 | —   | ns   | 3, 4  |
| LAL output transition to LAD/LDP output transition (LATCH hold time) |   | $t_{\text{LBOTOT}}$  | 1.5  | —   | ns   | 6     |
| Local bus clock to output valid (except LAD/LDP and LAL)             | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOV1}}$ | —    | 0.5 | ns   | 3     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |      | 2.0 |      |       |
| Local bus clock to data valid for LAD/LDP                            | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOV2}}$ | —    | 0.7 | ns   | 3     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |      | 2.2 |      |       |

**Table 31. Local Bus General Timing Parameters - DLL Bypassed (continued)**

| Parameter  | Configuration <sup>7</sup>                  | Symbol <sup>1</sup>  | Min  | Max | Unit | Notes |
|--|---|----------------------|------|-----|------|-------|
| Local bus clock to address valid for LAD                           | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOV3}}$ | —    | 0.8 | ns   | 3     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |      | 2.3 |      |       |
| Output hold from local bus clock (except LAD/LDP and LALE)         | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOX1}}$ | -2.7 | —   | ns   | 3     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      | -1.8 |     |      |       |
| Output hold from local bus clock for LAD/LDP                       | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOX2}}$ | -2.7 | —   | ns   | 3     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      | -1.8 |     |      |       |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOZ1}}$ | —    | 1.0 | ns   | 5     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |      | 2.4 |      |       |
| Local bus clock to output high impedance for LAD/LDP               | $\overline{\text{LWE}}[0:1] = 00$           | $t_{\text{LBKLOZ2}}$ | —    | 1.0 | ns   | 5     |
|  | $\overline{\text{LWE}}[0:1] = 11$ (default) |                      |      | 2.4 |      |       |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of  $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$  for inputs and  $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$  for outputs. For example,  $t_{\text{LBIXKH1}}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{\text{LBK}}$  clock reference (K) goes high (H), in this case for clock one(1). Also,  $t_{\text{LBKHOX}}$  symbolizes local bus timing (LB) for the  $t_{\text{LBK}}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC\_IN for DLL enabled mode.
3. All signals are measured from  $\text{OV}_{\text{DD}}/2$  of the rising edge of local bus clock for DLL bypass mode to  $0.4 \times \text{OV}_{\text{DD}}$  of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of  $t_{\text{LBOTOT}}$  is defined as the sum of 1/2 or 1 ccb\_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins  $\overline{\text{LWE}}[0:1]$ .
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at  $\text{OV}_{\text{DD}}/2$ .
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 15 provides the AC test load for the local bus.

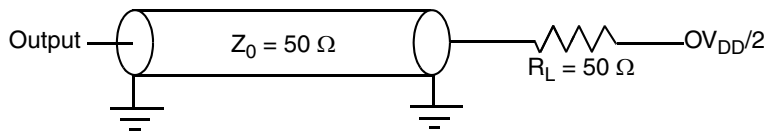
**Figure 15. Local Bus C Test Load**

Figure 16 to Figure 21 show the local bus signals.

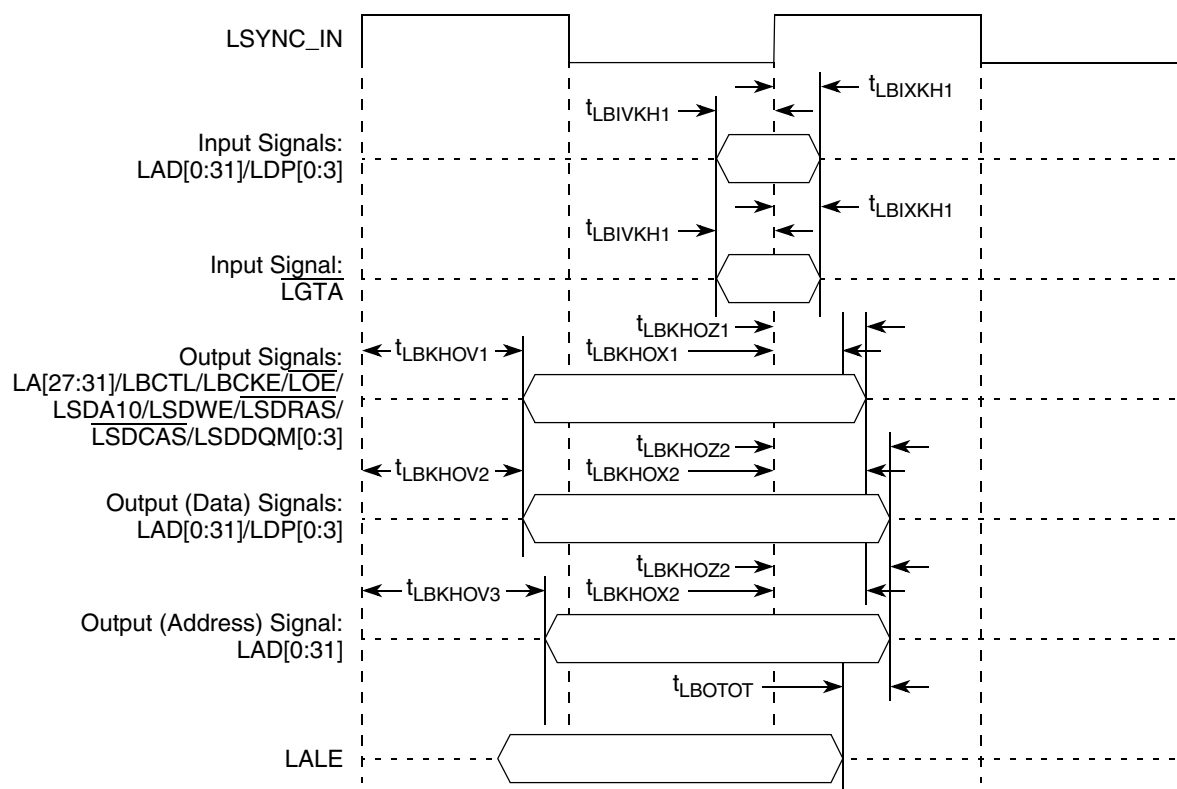


Figure 16. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

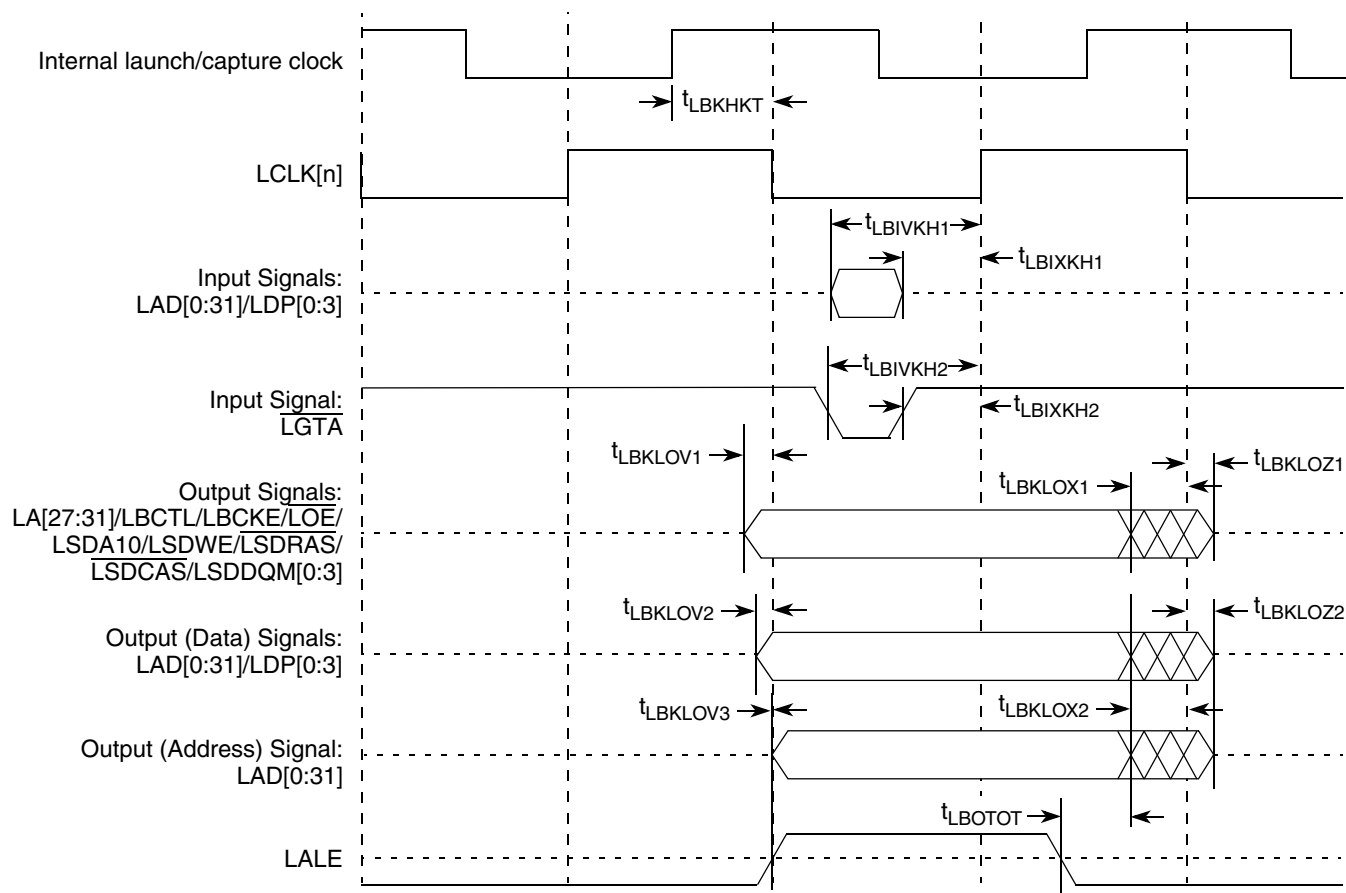
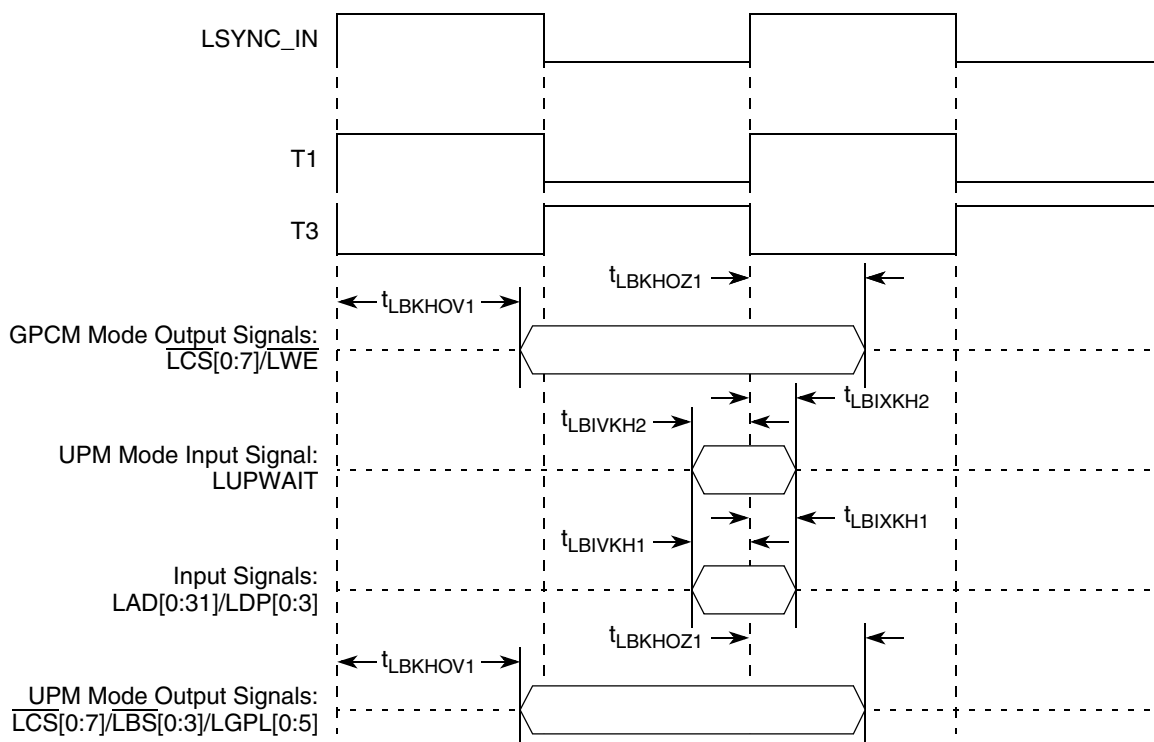
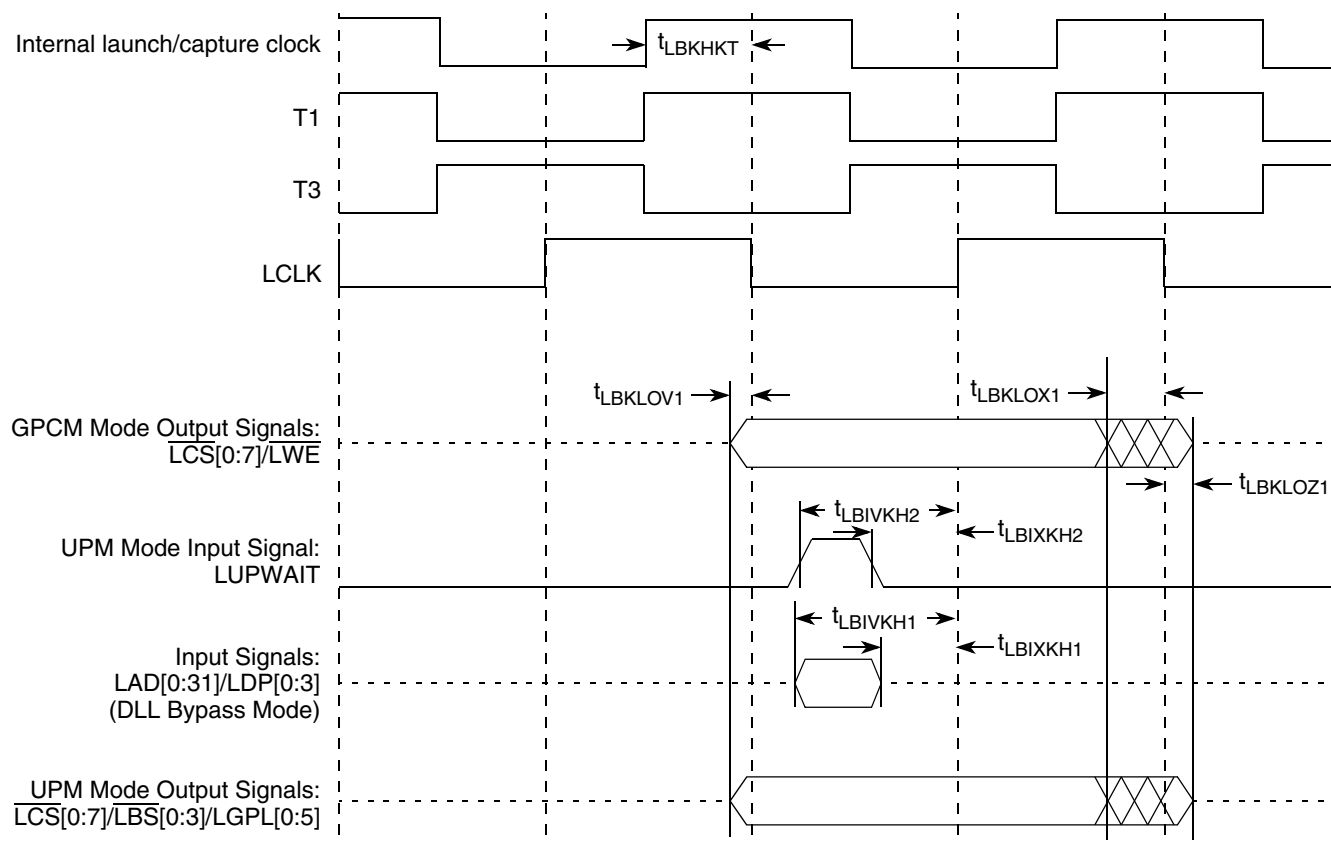


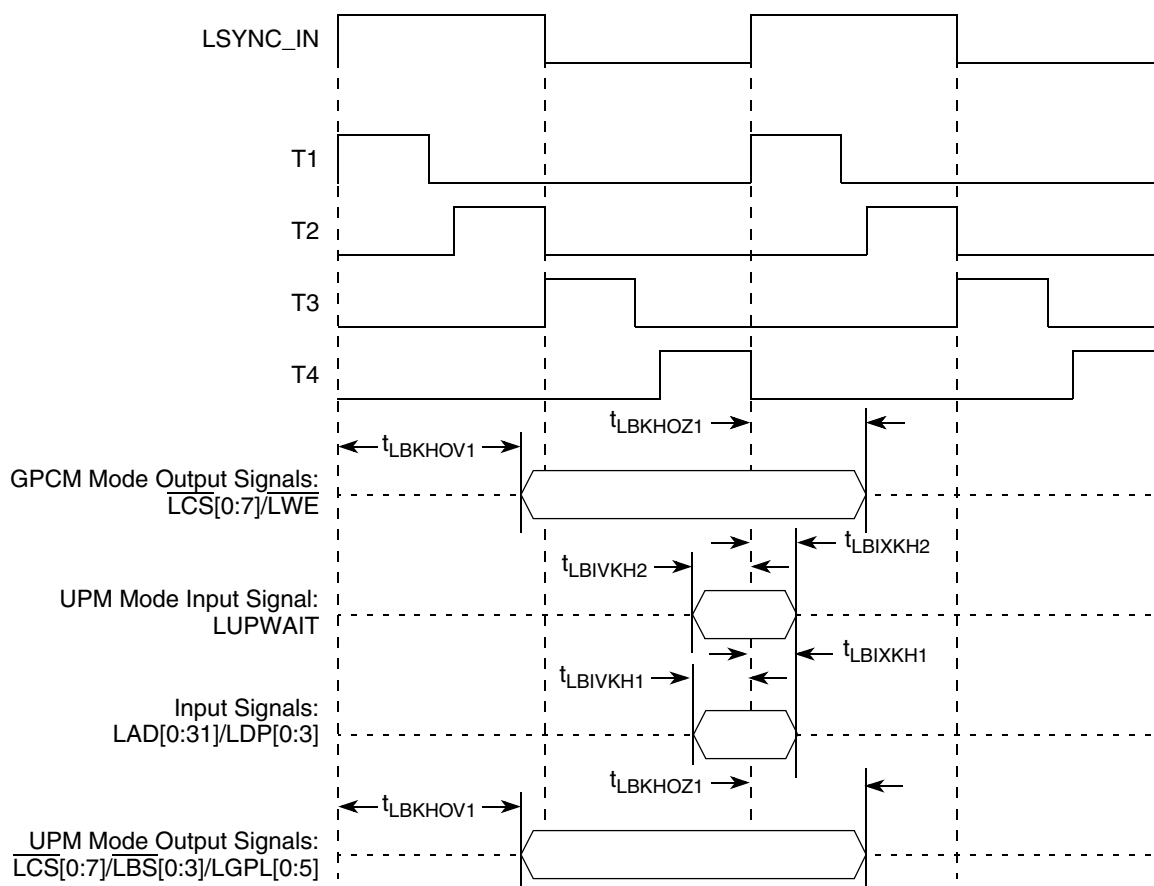
Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)



**Figure 18. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)**



**Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)**



**Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)**

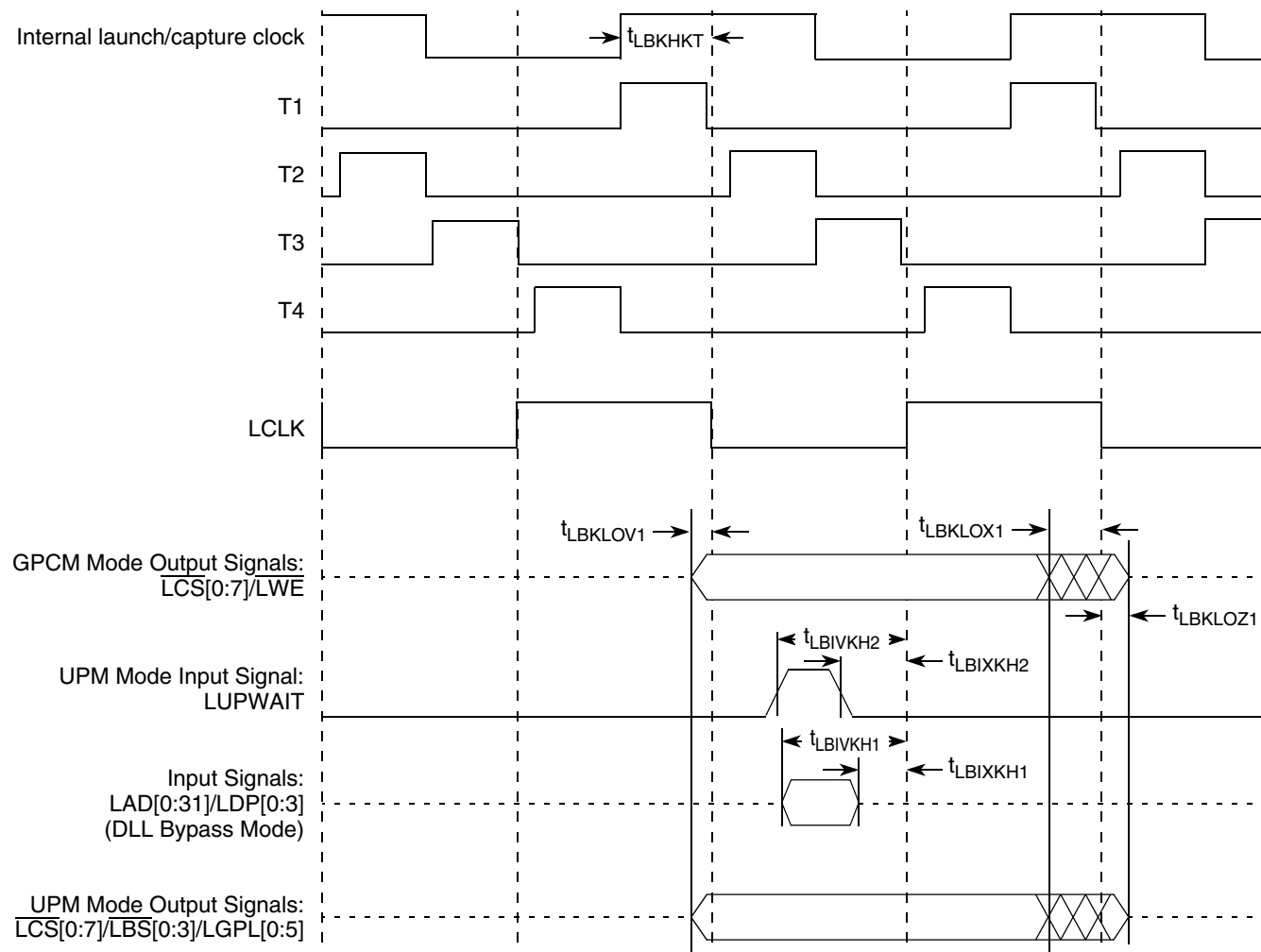


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)



## 10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8541E.

### 10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

**Table 32. CPM DC Electrical Characteristics**

| Characteristic      | Symbol   | Condition                  | Min | Max   | Unit | Notes |
|---------------------|----------|----------------------------|-----|-------|------|-------|
| Input high voltage  | $V_{IH}$ |                            | 2.0 | 3.465 | V    | 1     |
| Input low voltage   | $V_{IL}$ |                            | GND | 0.8   | V    | 1, 2  |
| Output high voltage | $V_{OH}$ | $I_{OH} = -8.0 \text{ mA}$ | 2.4 | —     | V    | 1     |
| Output low voltage  | $V_{OL}$ | $I_{OL} = 8.0 \text{ mA}$  | —   | 0.5   | V    | 1     |
| Output high voltage | $V_{OH}$ | $I_{OH} = -2.0 \text{ mA}$ | 2.4 | —     | V    | 1     |
| Output low voltage  | $V_{OL}$ | $I_{OL} = 3.2 \text{ mA}$  | —   | 0.4   | V    | 1     |

### 10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

**Table 33. CPM Input AC Timing Specifications <sup>1</sup>**

| Characteristic                                    | Symbol <sup>2</sup> | Min <sup>3</sup> | Unit |
|---|---------------------|------------------|------|
| FCC inputs—internal clock (NMSI) input setup time | $t_{FIIVKH}$        | 6                | ns   |
| FCC inputs—internal clock (NMSI) hold time        | $t_{FIIXKH}$        | 0                | ns   |
| FCC inputs—external clock (NMSI) input setup time | $t_{FEIVKH}$        | 2.5              | ns   |
| FCC inputs—external clock (NMSI) hold time        | $t_{FEIXKH}^b$      | 2                | ns   |
| SPI inputs—internal clock (NMSI) input setup time | $t_{NIIVKH}$        | 6                | ns   |
| SPI inputs—internal clock (NMSI) input hold time  | $t_{NIIXKH}$        | 0                | ns   |
| SPI inputs—external clock (NMSI) input setup time | $t_{NEIVKH}$        | 4                | ns   |
| SPI inputs—external clock (NMSI) input hold time  | $t_{NEIXKH}$        | 2                | ns   |
| PIO inputs—input setup time                       | $t_{PIIVKH}$        | 8                | ns   |

**Table 33. CPM Input AC Timing Specifications <sup>1</sup> (continued)**

| Characteristic             | Symbol <sup>2</sup> | Min <sup>3</sup> | Unit |
|----------------------------|---------------------|------------------|------|
| PIO inputs—input hold time | $t_{PIIXKH}$        | 1                | ns   |
| COL width high (FCC)       | $t_{FCCH}$          | 1.5              | CLK  |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{FIIVKH}$  symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock  $t_{FCC}$  (K) going to the high (H) state or setup time.
3. PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

**Table 34. CPM Output AC Timing Specifications <sup>1</sup>**

| Characteristic                          | Symbol <sup>2</sup> | Min | Max | Unit |
|---|---------------------|-----|-----|------|
| FCC outputs—internal clock (NMSI) delay | $t_{FIKHOX}$        | 1   | 5.5 | ns   |
| FCC outputs—external clock (NMSI) delay | $t_{FEKHOX}$        | 2   | 8   | ns   |
| SPI outputs—internal clock (NMSI) delay | $t_{NIKHOX}$        | 0.5 | 10  | ns   |
| SPI outputs—external clock (NMSI) delay | $t_{NEKHOX}$        | 2   | 8   | ns   |
| PIO outputs delay                       | $t_{PIKHOX}$        | 1   | 11  | ns   |

**Notes:**

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{FIKHOX}$  symbolizes the FCC inputs internal timing (FI) for the time  $t_{FCC}$  memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 22 provides the AC test load for the CPM.

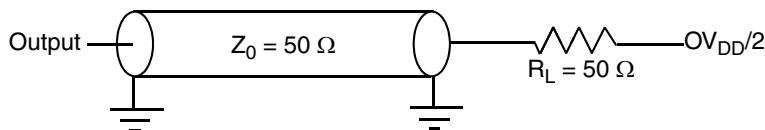
**Figure 22. CPM AC Test Load**

Figure 23 through Figure 28 represent the AC timing from Table 33 and Table 34. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 23 shows the FCC internal clock.

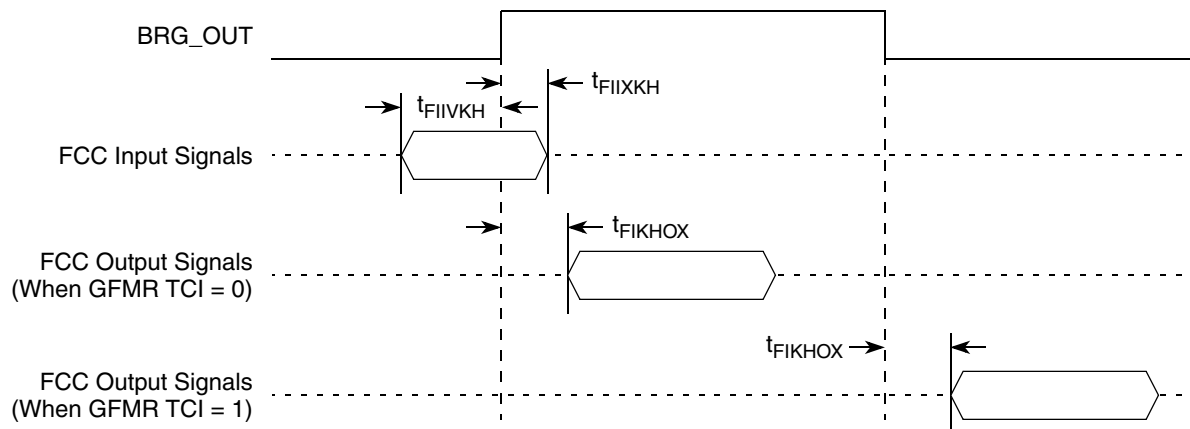


Figure 23. FCC Internal AC Timing Clock Diagram

Figure 24 shows the FCC external clock.

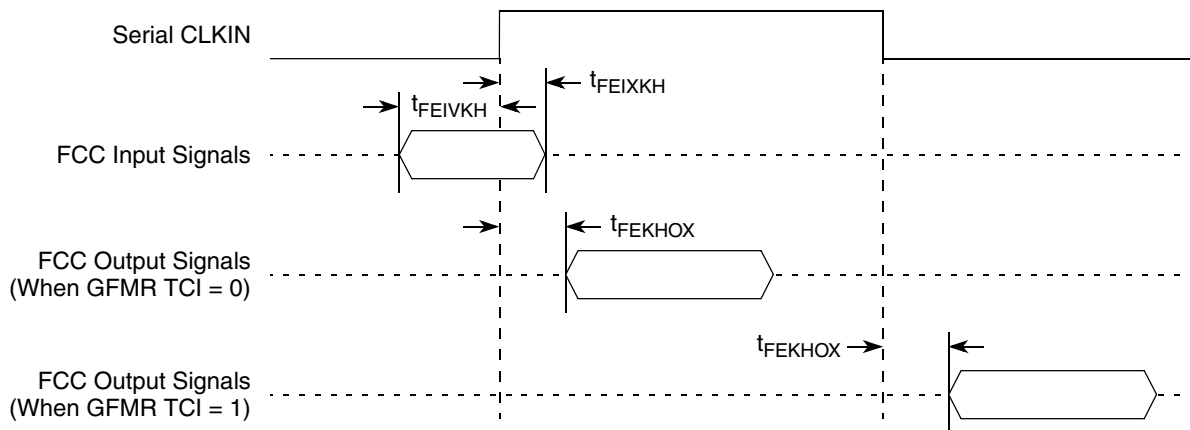


Figure 24. FCC External AC Timing Clock Diagram

Figure 25 shows Ethernet collision timing on FCCs.

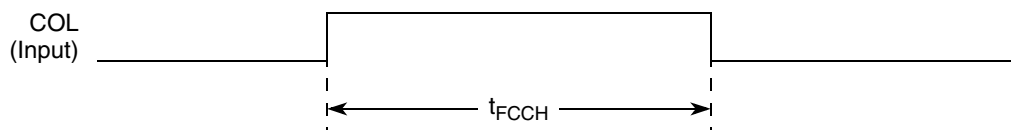
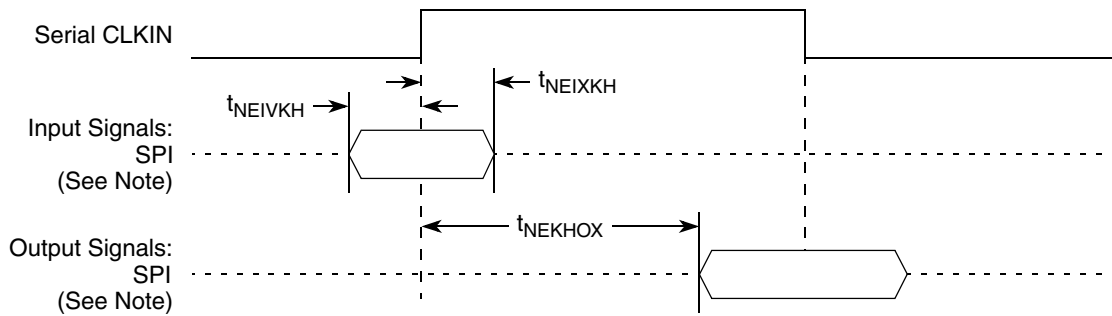


Figure 25. Ethernet Collision AC Timing Diagram (FCC)

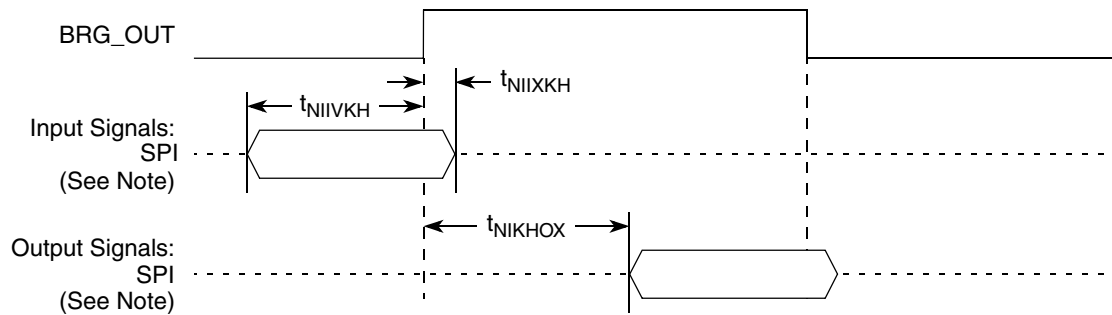
Figure 26 shows the SPI <sup>1,2</sup>external clock.



**Note:** The clock edge is selectable on SPI.

**Figure 26. SPI AC Timing External Clock Diagram**

Figure 27 shows the SPI <sup>1,2</sup>internal clock.

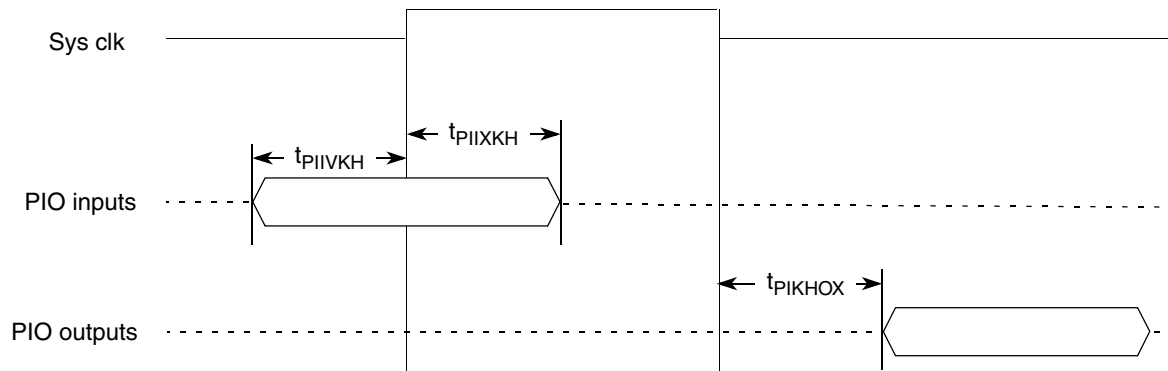


**Note:** The clock edge is selectable on SPI.

**Figure 27. SPI AC Timing Internal Clock Diagram**

<sup>1</sup> SPI AC timings are internal mode when it is master since SPICLK is an output, and external mode when it is slave.

<sup>2</sup> SPI AC timings refer always to SPICLK.



**Figure 28. PIO Signal Diagram**

## 10.3 CPM I2C AC Specification

Table 35. I2C Timing

| Characteristic                          | Expression  | All Frequencies                |                    | Unit |
|---|-------------|--------------------------------|--------------------|------|
|   |             | Min                            | Max                |      |
| SCL clock frequency (slave)             | $f_{SCL}$   | 0                              | $F_{MAX}^{(1)}$    | Hz   |
| SCL clock frequency (master)            | $f_{SCL}$   | BRGCLK/16512                   | BRGCLK/48          | Hz   |
| Bus free time between transmissions     | $t_{SDHDL}$ | $1/(2.2 * f_{SCL})$            | -                  | s    |
| Low period of SCL                       | $t_{SCLCH}$ | $1/(2.2 * f_{SCL})$            | -                  | s    |
| High period of SCL                      | $t_{SCHCL}$ | $1/(2.2 * f_{SCL})$            | -                  | s    |
| Start condition setup time <sup>2</sup> | $t_{SCHDL}$ | $2/(\text{divider} * f_{SCL})$ | - <sup>(2)</sup>   | s    |
| Start condition hold time <sup>2</sup>  | $t_{SDLCL}$ | $3/(\text{divider} * f_{SCL})$ | -                  | s    |
| Data hold time <sup>2</sup>             | $t_{SCLDX}$ | $2/(\text{divider} * f_{SCL})$ | -                  | s    |
| Data setup time <sup>2</sup>            | $t_{SDVCH}$ | $3/(\text{divider} * f_{SCL})$ | -                  | s    |
| SDA/SCL rise time                       | $t_{SRISE}$ | -                              | $1/(10 * f_{SCL})$ | s    |
| SDA/SCL fall time                       | $t_{SFALL}$ | -                              | $1/(33 * f_{SCL})$ | s    |
| Stop condition setup time               | $t_{SCHDH}$ | $2/(\text{divider} * f_{SCL})$ | -                  | s    |

**Notes:**

- $F_{MAX} = \text{BRGCLK}/(\text{min\_divider} * \text{prescaler})$ . Where prescaler=25-I2MODE[PDIV]; and min\_divider=12 if digital filter disabled and 18 if enabled.  
 Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then  $F_{MAX} = \text{BRGCLK}/48$   
 Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then  $F_{MAX} = \text{BRGCLK}/576$
- divider =  $f_{SCL}/\text{prescaler}$ .  
 In master mode: divider=BRGCLK/( $f_{SCL} * \text{prescaler}$ )=2\*(I2BRG[DIV]+3)  
 In slave mode: divider=BRGCLK/( $f_{SCL} * \text{prescaler}$ )

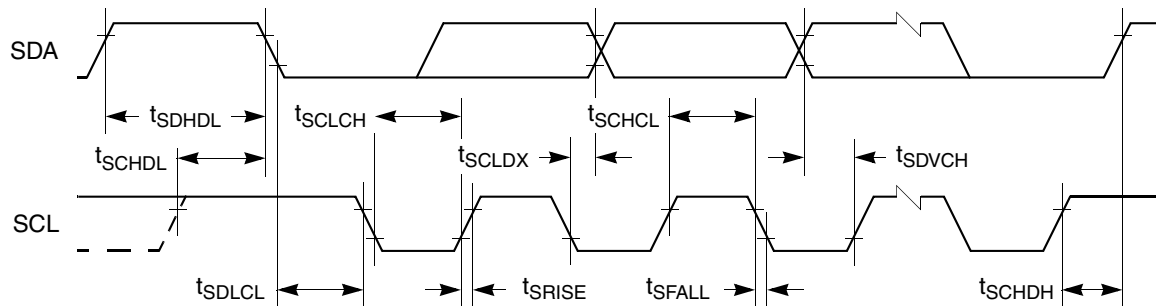


Figure 29. CPM I2C Bus Timing Diagram

The following two tables are examples of I2C AC parameters at I2C clock value of 100k and 400k respectively.

Table 36. CPM I2C Timing ( $f_{SCL}=100\text{KHz}$ )

| Characteristic                      | Expression  | Frequency = 100KHz |     | Unit          |
|-------------------------------------|-------------|--------------------|-----|---------------|
|                                     |             | Min                | Max |               |
| SCL clock frequency (slave)         | $f_{SCL}$   |                    | 100 | KHz           |
| SCL clock frequency (master)        | $f_{SCL}$   | -                  | 100 | KHz           |
| Bus free time between transmissions | $t_{SDHDL}$ | 4.7                | -   | $\mu\text{s}$ |
| Low period of SCL                   | $t_{SCLCH}$ | 4.7                | -   | $\mu\text{s}$ |

Table 36. CPM I2C Timing ( $f_{SCL}=100\text{KHz}$ ) (continued)

| Characteristic             | Expression  | Frequency = 100KHz |     | Unit          |
|----------------------------|-------------|--------------------|-----|---------------|
|                            |             | Min                | Max |               |
| High period of SCL         | $t_{SCHCL}$ | 4                  | -   | $\mu\text{s}$ |
| Start condition setup time | $t_{SCHDL}$ | 2                  | -   | $\mu\text{s}$ |
| Start condition hold time  | $t_{SDLCL}$ | 3                  | -   | $\mu\text{s}$ |
| Data hold time             | $t_{SCLDX}$ | 2                  | -   | $\mu\text{s}$ |
| Data setup time            | $t_{SDVCH}$ | 3                  | -   | $\mu\text{s}$ |
| SDA/SCL rise time          | $t_{SRISE}$ | -                  | 1   | $\mu\text{s}$ |
| SDA/SCL fall time (master) | $t_{SFALL}$ | -                  | 303 | ns            |
| Stop condition setup time  | $t_{SCHDH}$ | 2                  | -   | $\mu\text{s}$ |

Table 37. CPM I2C Timing ( $f_{SCL}=400\text{KHz}$ )

| Characteristic                      | Expression  | Frequency = 400KHz |     | Unit          |
|-------------------------------------|-------------|--------------------|-----|---------------|
|                                     |             | Min                | Max |               |
| SCL clock frequency (slave)         | $f_{SCL}$   |                    | 400 | KHz           |
| SCL clock frequency (master)        | $f_{SCL}$   | -                  | 400 | KHz           |
| Bus free time between transmissions | $t_{SDHDL}$ | 1.2                | -   | $\mu\text{s}$ |
| Low period of SCL                   | $t_{SCLCH}$ | 1.2                | -   | $\mu\text{s}$ |
| High period of SCL                  | $t_{SCHCL}$ | 1                  | -   | $\mu\text{s}$ |
| Start condition setup time          | $t_{SCHDL}$ | 420                | -   | ns            |
| Start condition hold time           | $t_{SDLCL}$ | 630                | -   | ns            |
| Data hold time                      | $t_{SCLDX}$ | 420                | -   | ns            |
| Data setup time                     | $t_{SDVCH}$ | 630                | -   | ns            |
| SDA/SCL rise time                   | $t_{SRISE}$ | -                  | 250 | ns            |
| SDA/SCL fall time                   | $t_{SFALL}$ | -                  | 75  | ns            |
| Stop condition setup time           | $t_{SCHDH}$ | 420                | -   | ns            |

## 11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8541E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 31 through Figure 34.

Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) <sup>1</sup>

At recommended operating conditions (see Table 2).

| Parameter   | Symbol <sup>2</sup>     | Min | Max  | Unit | Notes |
|---|-------------------------|-----|------|------|-------|
| JTAG external clock frequency of operation        | $f_{JTG}$               | 0   | 33.3 | MHz  |       |
| JTAG external clock cycle time                    | $t_{JTG}$               | 30  | —    | ns   |       |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$            | 15  | —    | ns   |       |
| JTAG external clock rise and fall times           | $t_{JTGR}$ & $t_{JTGF}$ | 0   | 2    | ns   |       |
| $\overline{\text{TRST}}$ assert time              | $t_{TRST}$              | 25  | —    | ns   | 3     |

**Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) <sup>1</sup> (continued)**

At recommended operating conditions (see Table 2).

| Parameter                                     | Symbol <sup>2</sup>                        | Min      | Max      | Unit | Notes |
|---|--|----------|----------|------|-------|
| Input setup times:                            |  |          |          | ns   |       |
| Boundary-scan data<br>TMS, TDI                | $t_{JTDV\text{KH}}$<br>$t_{JTIV\text{KH}}$ | 4<br>0   | —<br>—   |      | 4     |
| Input hold times:                             |  |          |          | ns   |       |
| Boundary-scan data<br>TMS, TDI                | $t_{JTD\text{XKH}}$<br>$t_{JTIX\text{KH}}$ | 20<br>25 | —<br>—   |      | 4     |
| Valid times:                                  |  |          |          | ns   |       |
| Boundary-scan data<br>TDO                     | $t_{JTKLDV}$<br>$t_{JTKLOV}$               | 4<br>4   | 20<br>25 |      | 5     |
| Output hold times:                            |  |          |          | ns   |       |
| Boundary-scan data<br>TDO                     | $t_{JTKLDX}$<br>$t_{JTKLOX}$               | —<br>—   | —<br>—   |      | 5     |
| JTAG external clock to output high impedance: |  |          |          | ns   |       |
| Boundary-scan data<br>TDO                     | $t_{JTKLDZ}$<br>$t_{JTKLOZ}$               | 3<br>3   | 19<br>9  |      | 5, 6  |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- $\Omega$  load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{JTDV\text{KH}}$  symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTD\text{XKH}}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3.  $\overline{TRST}$  is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to  $t_{TCLK}$ .
5. Non-JTAG signal output timing with respect to  $t_{TCLK}$ .
6. Guaranteed by design.

Figure 30 provides the AC test load for TDO and the boundary-scan outputs of the MPC8541E.

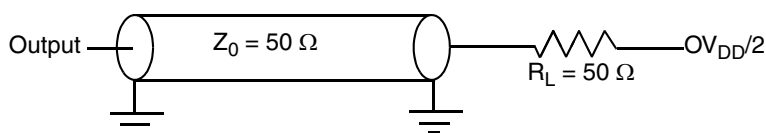
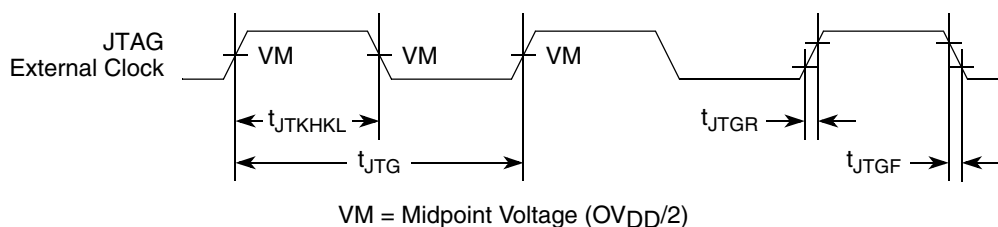
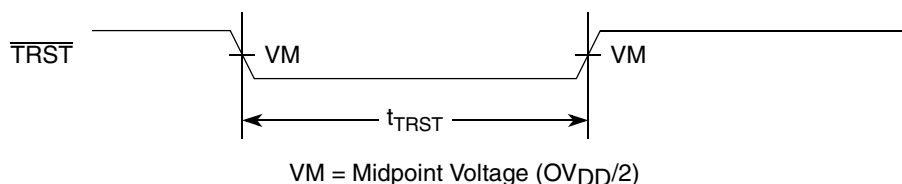
**Figure 30. AC Test Load for the JTAG Interface**

Figure 31 provides the JTAG clock input timing diagram.



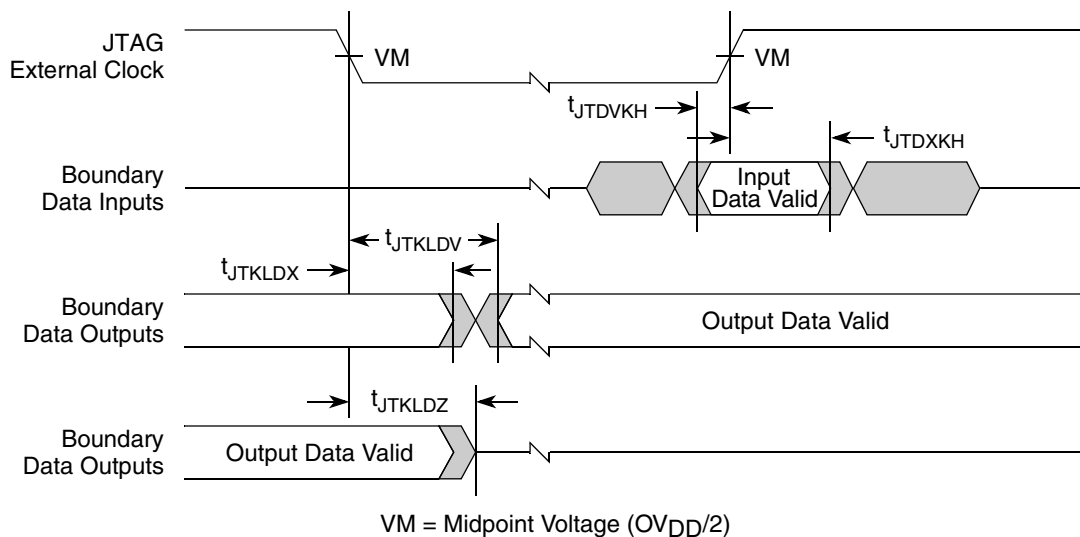
**Figure 31. JTAG Clock Input Timing Diagram**

Figure 32 provides the  $\overline{\text{TRST}}$  timing diagram.



**Figure 32.  $\overline{\text{TRST}}$  Timing Diagram**

Figure 33 provides the boundary-scan timing diagram.



**Figure 33. Boundary-Scan Timing Diagram**



Figure 34 provides the test access port timing diagram.

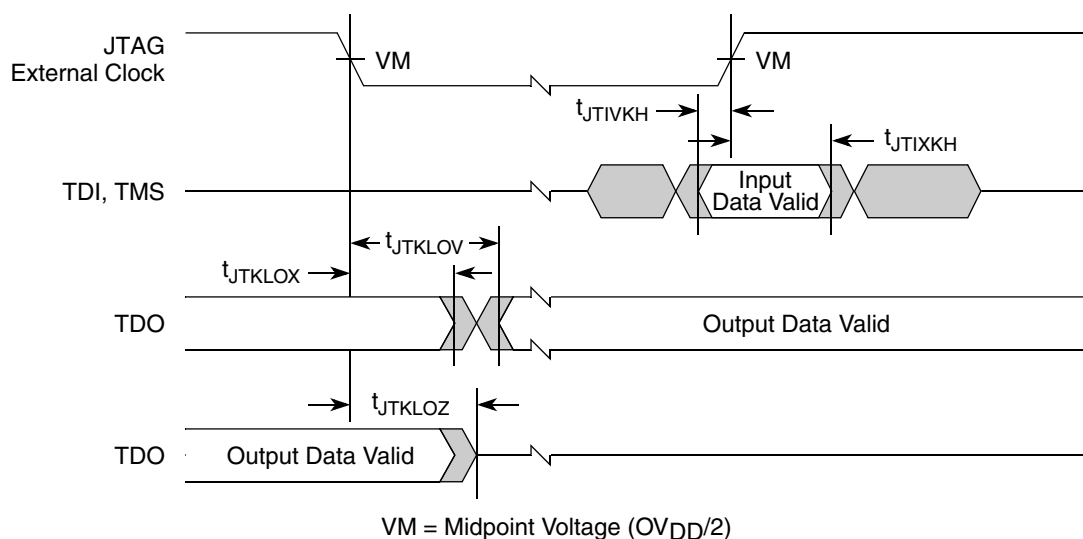


Figure 34. Test Access Port Timing Diagram

## 12 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the I<sup>2</sup>C interface of the MPC8541E.

### 12.1 I<sup>2</sup>C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I<sup>2</sup>C interface of the MPC8541E.

Table 39. I<sup>2</sup>C DC Electrical Characteristics

At recommended operating conditions with  $OV_{DD}$  of  $3.3\text{ V} \pm 5\%$ .

| Parameter  | Symbol       | Min                   | Max                  | Unit          | Notes |
|--|--------------|-----------------------|----------------------|---------------|-------|
| Input high voltage level   | $V_{IH}$     | $0.7 \times OV_{DD}$  | $OV_{DD} + 0.3$      | V             |       |
| Input low voltage level  | $V_{IL}$     | -0.3                  | $0.3 \times OV_{DD}$ | V             |       |
| Low level output voltage   | $V_{OL}$     | 0                     | $0.2 \times OV_{DD}$ | V             | 1     |
| Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF      | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250                  | ns            | 2     |
| Pulse width of spikes which must be suppressed by the input filter   | $t_{I2KHKL}$ | 0                     | 50                   | ns            | 3     |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$ ) | $I_I$        | -10                   | 10                   | $\mu\text{A}$ | 4     |
| Capacitance for each I/O pin   | $C_I$        | —                     | 10                   | pF            |       |

**Notes:**

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- $C_B$  = capacitance of one bus line in pF.
- Refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins will obstruct the SDA and SCL lines if  $OV_{DD}$  is switched off.

## 12.2 I<sup>2</sup>C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I<sup>2</sup>C interface of the MPC8541E.

**Table 40. I<sup>2</sup>C AC Electrical Specifications**

All values refer to  $V_{IH}$  (min) and  $V_{IL}$  (max) levels (see Table 39).

| Parameter  | Symbol <sup>1</sup>       | Min                         | Max                   | Unit |
|--|---------------------------|-----------------------------|-----------------------|------|
| SCL clock frequency  | $f_{I2C}$                 | 0                           | 400                   | kHz  |
| Low period of the SCL clock  | $t_{I2CL}$ <sup>6</sup>   | 1.3                         | —                     | μs   |
| High period of the SCL clock   | $t_{I2CH}$ <sup>6</sup>   | 0.6                         | —                     | μs   |
| Setup time for a repeated START condition  | $t_{I2SVKH}$ <sup>6</sup> | 0.6                         | —                     | μs   |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ <sup>6</sup> | 0.6                         | —                     | μs   |
| Data setup time  | $t_{I2DVKH}$ <sup>6</sup> | 100                         | —                     | ns   |
| Data hold time:<br>CBUS compatible masters<br>I <sup>2</sup> C bus devices                   | $t_{I2DXKL}$              | —<br>0 <sup>2</sup>         | —<br>0.9 <sup>3</sup> | μs   |
| Rise time of both SDA and SCL signals  | $t_{I2CR}$                | $20 + 0.1 C_b$ <sup>4</sup> | 300                   | ns   |
| Fall time of both SDA and SCL signals  | $t_{I2CF}$                | $20 + 0.1 C_b$ <sup>4</sup> | 300                   | ns   |
| Set-up time for STOP condition   | $t_{I2PVKH}$              | 0.6                         | —                     | μs   |
| Bus free time between a STOP and START condition   | $t_{I2KHDX}$              | 1.3                         | —                     | μs   |
| Noise margin at the LOW level for each connected device (including hysteresis)               | $V_{NL}$                  | $0.1 \times OV_{DD}$        | —                     | V    |
| Noise margin at the HIGH level for each connected device (including hysteresis)              | $V_{NH}$                  | $0.2 \times OV_{DD}$        | —                     | V    |

### Notes:

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{I2DVKH}$  symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{I2SXKL}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the  $t_{I2C}$  clock reference (K) going to the low (L) state or hold time. Also,  $t_{I2PVKH}$  symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the  $t_{I2C}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8541E provides a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum  $t_{I2DVKH}$  has only to be met if the device does not stretch the LOW period ( $t_{I2CL}$ ) of the SCL signal.
- $C_b$  = capacitance of one bus line in pF.
- Guaranteed by design.



## 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8541E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

### NOTE

PCI Clock can be PCI1\_CLK or SYSCLK based on POR config input.

### NOTE

The input setup time does not meet the PCI specification.

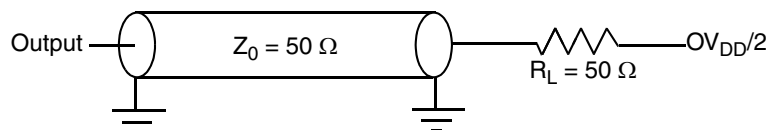
**Table 42. PCI AC Timing Specifications at 66 MHz**

| Parameter   | Symbol <sup>1</sup> | Min                 | Max | Unit   | Notes    |
|---|---------------------|---------------------|-----|--------|----------|
| Clock to output valid   | $t_{PCKHOV}$        | —                   | 6.0 | ns     | 2, 3     |
| Output hold from Clock  | $t_{PCKHOX}$        | 2.0                 | —   | ns     | 2, 9     |
| Clock to output high impedance                                    | $t_{PCKHOZ}$        | —                   | 14  | ns     | 2, 3, 10 |
| Input setup to Clock  | $t_{PCIVKH}$        | 3.3                 | —   | ns     | 2, 4, 9  |
| Input hold from Clock   | $t_{PCIXKH}$        | 0                   | —   | ns     | 2, 4, 9  |
| $\overline{REQ64}$ to $\overline{HRESET}$ <sup>9</sup> setup time | $t_{PCRVRH}$        | $10 \times t_{SYS}$ | —   | clocks | 5, 6, 10 |
| $\overline{HRESET}$ to $\overline{REQ64}$ hold time               | $t_{PCRHRX}$        | 0                   | 50  | ns     | 6, 10    |
| $\overline{HRESET}$ high to first $\overline{FRAME}$ assertion    | $t_{PCRHFV}$        | 10                  | —   | clocks | 7, 10    |

Notes:

- Note that the symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{PCIVKH}$  symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock,  $t_{SYS}$ , reference (K) going to the high (H) state or setup time. Also,  $t_{PCRHFV}$  symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter  $t_{SYS}$  indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
- The setup and hold time is with respect to the rising edge of  $\overline{HRESET}$ .
- The timing parameter  $t_{PCRHFV}$  is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for  $\overline{HRESET}$  is 100  $\mu s$ .
- Guaranteed by characterization.
- Guaranteed by design.

Figure 15 provides the AC test load for PCI.



**Figure 37. PCI AC Test Load**

Figure 38 shows the PCI input AC timing conditions.

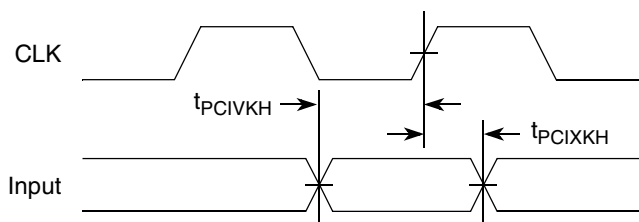


Figure 38. PCI Input AC Timing Measurement Conditions

Figure 39 shows the PCI output AC timing conditions.

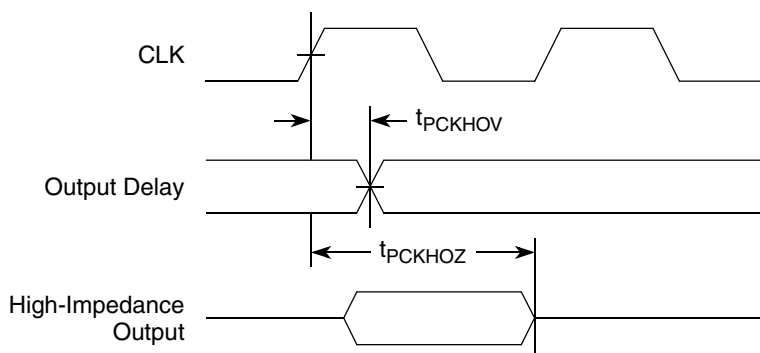


Figure 39. PCI Output AC Timing Measurement Condition

## 14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

### 14.1 Package Parameters for the MPC8541E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

|                         |                           |
|-------------------------|---------------------------|
| Die size                | 8.7 mm × 9.3 mm × 0.75 mm |
| Package outline         | 29 mm × 29 mm             |
| Interconnects           | 783                       |
| Pitch                   | 1 mm                      |
| Minimum module height   | 3.07 mm                   |
| Maximum module height   | 3.75 mm                   |
| Solder Balls            | 62 Sn/36 Pb/2 Ag          |
| Ball diameter (typical) | 0.5 mm                    |

## 14.2 Mechanical Dimensions of the FC-PBGA

Figure 40 the mechanical dimensions and bottom surface nomenclature of the MPC8541E 783 FC-PBGA package.

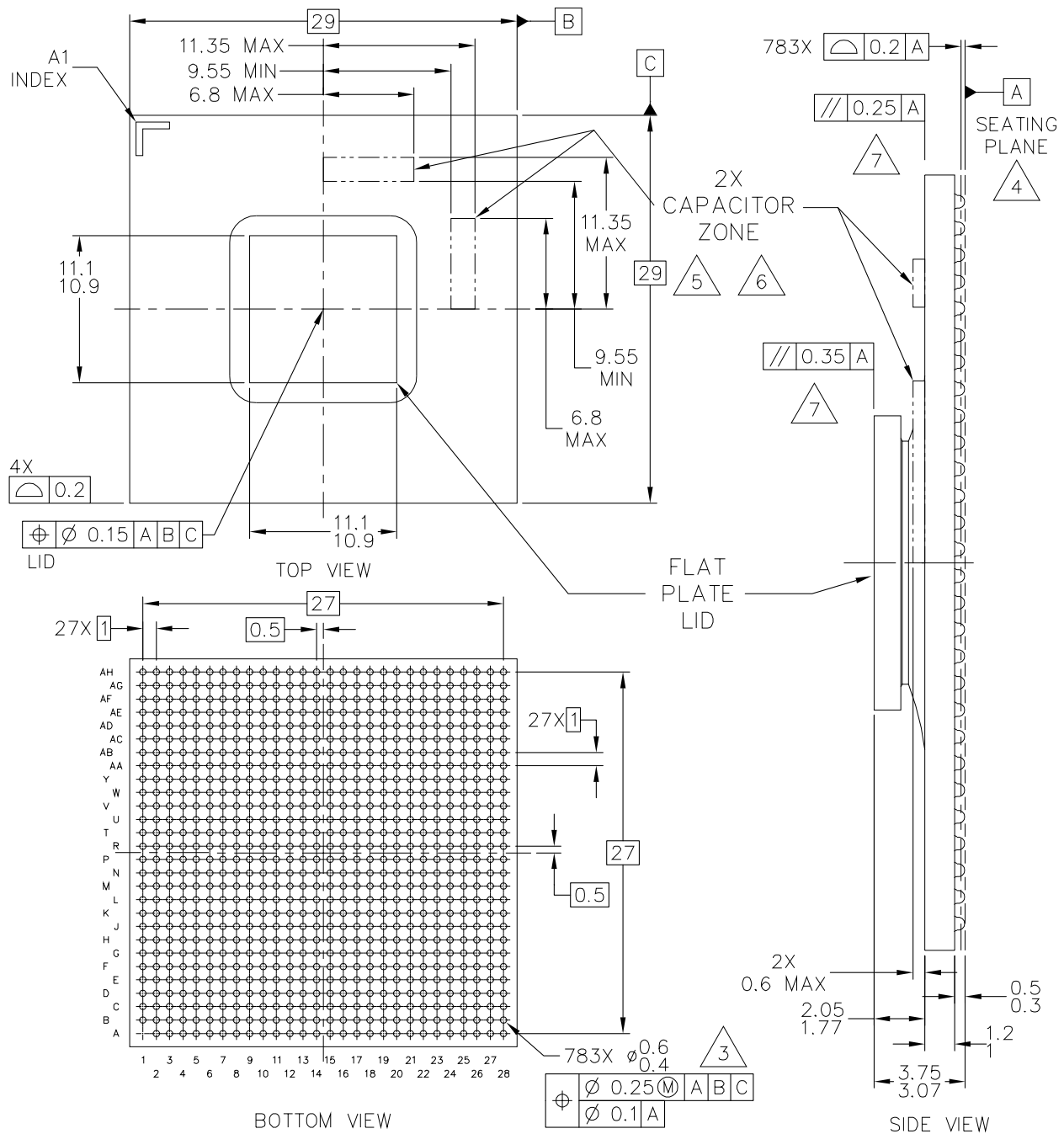


Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA

### NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

## 14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8541E, 783 FC-PBGA package.

**Table 43. MPC8541E Pinout Listing**

| Signal  | Package Pin Number  | Pin Type | Power Supply     | Notes |
|---|---|----------|------------------|-------|
| <b>PCI1 and PCI2 (one 64-bit or two 32-bit)</b> |   |          |                  |       |
| PCI1_AD[63:32],<br>PCI2_AD[31:0]                | AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14,<br>V15, W15, Y15, AA15, AB15, AC15, AD15, AG15,<br>AH15, V16, W16, AB16, AC16, AD16, AE16, AF16,<br>V17, W17, Y17, AA17, AB17, AE17, AF17, AF18 | I/O      | OV <sub>DD</sub> | 17    |
| PCI1_AD[31:0]                                   | AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9,<br>AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11,<br>AG11, AH11, V12, W12, Y12, AB12, AD12, AE12,<br>AG12, AH12, V13, Y13, AB13, AC13             | I/O      | OV <sub>DD</sub> | 17    |
| PCI_C_BE64[7:4]<br>PCI2_C_BE[3:0]               | AG13, AH13, V14, W14  | I/O      | OV <sub>DD</sub> | 17    |
| PCI_C_BE64[3:0]<br>PCI1_C_BE[3:0]               | AH8, AB10, AD11, AC12   | I/O      | OV <sub>DD</sub> | 17    |
| PCI1_PAR  | AA11  | I/O      | OV <sub>DD</sub> |       |
| PCI1_PAR64/PCI2_PAR                             | Y14   | I/O      | OV <sub>DD</sub> |       |
| PCI1_FRAME                                      | AC10  | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_TRDY                                       | AG10  | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_IRDY                                       | AD10  | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_STOP                                       | V11   | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_DEVSEL                                     | AH10  | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_IDSEL                                      | AA9   | I        | OV <sub>DD</sub> |       |
| PCI1_REQ64/PCI2_FRAME                           | AE13  | I/O      | OV <sub>DD</sub> | 5, 10 |
| PCI1_ACK64/PCI2_DEVSEL                          | AD13  | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_PERR                                       | W11   | I/O      | OV <sub>DD</sub> | 2     |
| PCI1_SERR                                       | Y11   | I/O      | OV <sub>DD</sub> | 2, 4  |
| PCI1_REQ[0]                                     | AF5   | I/O      | OV <sub>DD</sub> |       |
| PCI1_REQ[1:4]                                   | AF3, AE4, AG4, AE5  | I        | OV <sub>DD</sub> |       |

Table 43. MPC8541E Pinout Listing (continued)

| Signal                            | Package Pin Number   | Pin Type | Power Supply     | Notes |
|-----------------------------------|--|----------|------------------|-------|
| PCI1_GNT[0]                       | AE6  | I/O      | OV <sub>DD</sub> |       |
| PCI1_GNT[1:4]                     | AG5, AH5, AF6, AG6   | O        | OV <sub>DD</sub> | 5, 9  |
| PCI1_CLK                          | AH25   | I        | OV <sub>DD</sub> |       |
| PCI2_CLK                          | AH27   | I        | OV <sub>DD</sub> |       |
| PCI2_GNT[0]                       | AC18   | I/O      | OV <sub>DD</sub> |       |
| PCI2_GNT[1:4]                     | AD18, AE18, AE19, AD19   | O        | OV <sub>DD</sub> | 5, 9  |
| PCI2_IDSEL                        | AC22   | I        | OV <sub>DD</sub> |       |
| PCI2_IRDY                         | AD20   | I/O      | OV <sub>DD</sub> | 2     |
| PCI2_PERR                         | AC20   | I/O      | OV <sub>DD</sub> | 2     |
| PCI2_REQ[0]                       | AD21   | I/O      | OV <sub>DD</sub> |       |
| PCI2_REQ[1:4]                     | AE21, AD22, AE22, AC23   | I        | OV <sub>DD</sub> |       |
| PCI2_SERR                         | AE20   | I/O      | OV <sub>DD</sub> | 2,4   |
| PCI2_STOP                         | AC21   | I/O      | OV <sub>DD</sub> | 2     |
| PCI2_TRDY                         | AC19   | I/O      | OV <sub>DD</sub> | 2     |
| <b>DDR SDRAM Memory Interface</b> |  |          |                  |       |
| MDQ[0:63]                         | M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12 | I/O      | GV <sub>DD</sub> |       |
| MECC[0:7]                         | N20, M20, L19, E19, C21, A21, G19, A19   | I/O      | GV <sub>DD</sub> |       |
| MDM[0:8]                          | L24, H28, F24, L21, E18, E16, G14, B13, M19  | O        | GV <sub>DD</sub> |       |
| MDQS[0:8]                         | L26, J25, D25, A22, H18, F16, F14, C13, C20  | I/O      | GV <sub>DD</sub> |       |
| MBA[0:1]                          | B18, B19   | O        | GV <sub>DD</sub> |       |
| MA[0:14]                          | N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13  | O        | GV <sub>DD</sub> |       |
| MWE                               | D17  | O        | GV <sub>DD</sub> |       |
| MRAS                              | F17  | O        | GV <sub>DD</sub> |       |
| MCAS                              | J16  | O        | GV <sub>DD</sub> |       |
| MCS[0:3]                          | H16, G16, J15, H15   | O        | GV <sub>DD</sub> |       |
| MCKE[0:1]                         | E26, E28   | O        | GV <sub>DD</sub> | 11    |
| MCK[0:5]                          | J20, H25, A15, D20, F28, K14   | O        | GV <sub>DD</sub> |       |
| MCK[0:5]                          | F20, G27, B15, E20, F27, L14   | O        | GV <sub>DD</sub> |       |



Table 43. MPC8541E Pinout Listing (continued)

| Signal   | Package Pin Number  | Pin Type | Power Supply     | Notes   |
|--|---|----------|------------------|---------|
| MSYNC_IN   | M28   | I        | GV <sub>DD</sub> | 22      |
| MSYNC_OUT  | N28   | O        | GV <sub>DD</sub> | 22      |
| <b>Local Bus Controller Interface</b>                                      |   |          |                  |         |
| LA[27]   | U18   | O        | OV <sub>DD</sub> | 5, 9    |
| LA[28:31]  | T18, T19, T20, T21  | O        | OV <sub>DD</sub> | 5, 7, 9 |
| LAD[0:31]  | AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26 | I/O      | OV <sub>DD</sub> |         |
| LALE   | V21   | O        | OV <sub>DD</sub> | 5, 8, 9 |
| LBCTL  | V20   | O        | OV <sub>DD</sub> | 9       |
| LCKE   | U23   | O        | OV <sub>DD</sub> |         |
| LCLK[0:2]  | U27, U28, V18   | O        | OV <sub>DD</sub> |         |
| $\overline{\text{LCS}}[0:4]$   | Y27, Y28, W27, W28, R27   | O        | OV <sub>DD</sub> |         |
| $\overline{\text{LCS5/DMA\_DREQ2}}$  | R28   | I/O      | OV <sub>DD</sub> | 1       |
| $\overline{\text{LCS6/DMA\_DACK2}}$  | P27   | O        | OV <sub>DD</sub> | 1       |
| $\overline{\text{LCS7/DMA\_DDONE2}}$                                       | P28   | O        | OV <sub>DD</sub> | 1       |
| LDP[0:3]   | AA27, AA28, T26, P21  | I/O      | OV <sub>DD</sub> |         |
| LGPL0/LSDA10   | U19   | O        | OV <sub>DD</sub> | 5, 9    |
| LGPL1/ $\overline{\text{LSDWE}}$   | U22   | O        | OV <sub>DD</sub> | 5, 9    |
| LGPL2/ $\overline{\text{LOE/LSDRAS}}$                                      | V28   | O        | OV <sub>DD</sub> | 5, 8, 9 |
| LGPL3/ $\overline{\text{LSDCAS}}$  | V27   | O        | OV <sub>DD</sub> | 5, 9    |
| LGPL4/ $\overline{\text{LGT\AA/LUPWAIT/LPBSE}}$                            | V23   | I/O      | OV <sub>DD</sub> | 21      |
| LGPL5  | V22   | O        | OV <sub>DD</sub> | 5, 9    |
| LSYNC_IN   | T27   | I        | OV <sub>DD</sub> |         |
| LSYNC_OUT  | T28   | O        | OV <sub>DD</sub> |         |
| $\overline{\text{LWE}}[0:1]/\text{LSDDQM}[0:1]/\overline{\text{LBS}}[0:1]$ | AB28, AB27  | O        | OV <sub>DD</sub> | 1, 5, 9 |
| $\overline{\text{LWE}}[2:3]/\text{LSDDQM}[2:3]/\overline{\text{LBS}}[2:3]$ | T23, P24  | O        | OV <sub>DD</sub> | 1, 5, 9 |
| <b>DMA</b>   |   |          |                  |         |
| $\overline{\text{DMA\_DREQ}}[0:1]$   | H5, G4  | I        | OV <sub>DD</sub> |         |
| $\overline{\text{DMA\_DACK}}[0:1]$   | H6, G5  | O        | OV <sub>DD</sub> |         |

Table 43. MPC8541E Pinout Listing (continued)

| Signal  | Package Pin Number                           | Pin Type | Power Supply     | Notes    |
|---|--|----------|------------------|----------|
| DMA_DDONE[0:1]  | H7, G6                                       | O        | OV <sub>DD</sub> |          |
| <b>Programmable Interrupt Controller</b>                    |  |          |                  |          |
| MCP   | AG17   | I        | OV <sub>DD</sub> |          |
| UDE   | AG16   | I        | OV <sub>DD</sub> |          |
| IRQ[0:7]  | AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25 | I        | OV <sub>DD</sub> |          |
| IRQ8  | AB20   | I        | OV <sub>DD</sub> | 9        |
| IRQ9/DMA_DREQ3  | Y20  | I        | OV <sub>DD</sub> | 1        |
| IRQ10/DMA_DACK3   | AF26   | I/O      | OV <sub>DD</sub> | 1        |
| IRQ11/DMA_DDONE3  | AH24   | I/O      | OV <sub>DD</sub> | 1        |
| IRQ_OUT   | AB21   | O        | OV <sub>DD</sub> | 2, 4     |
| <b>Ethernet Management Interface</b>                        |  |          |                  |          |
| EC_MDC  | F1   | O        | OV <sub>DD</sub> | 5, 9     |
| EC_MDIO   | E1   | I/O      | OV <sub>DD</sub> |          |
| <b>Gigabit Reference Clock</b>                              |  |          |                  |          |
| EC_GTX_CLK125   | E2   | I        | LV <sub>DD</sub> |          |
| <b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b> |  |          |                  |          |
| TSEC1_TXD[7:4]  | A6, F7, D7, C7                               | O        | LV <sub>DD</sub> |          |
| TSEC1_TXD[3:0]  | B7, A7, G8, E8                               | O        | LV <sub>DD</sub> | 9, 18    |
| TSEC1_TX_EN   | C8   | O        | LV <sub>DD</sub> | 11       |
| TSEC1_TX_ER   | B8   | O        | LV <sub>DD</sub> |          |
| TSEC1_TX_CLK  | C6   | I        | LV <sub>DD</sub> |          |
| TSEC1_GTX_CLK   | B6   | O        | LV <sub>DD</sub> |          |
| TSEC1_CRS   | C3   | I        | LV <sub>DD</sub> |          |
| TSEC1_COL   | G7   | I        | LV <sub>DD</sub> |          |
| TSEC1_RXD[7:0]  | D4, B4, D3, D5, B5, A5, F6, E6               | I        | LV <sub>DD</sub> |          |
| TSEC1_RX_DV   | D2   | I        | LV <sub>DD</sub> |          |
| TSEC1_RX_ER   | E5   | I        | LV <sub>DD</sub> |          |
| TSEC1_RX_CLK  | D6   | I        | LV <sub>DD</sub> |          |
| <b>Three-Speed Ethernet Controller (Gigabit Ethernet 2)</b> |  |          |                  |          |
| TSEC2_TXD[7:4]  | B10, A10, J10, K11                           | O        | LV <sub>DD</sub> |          |
| TSEC2_TXD[3:0]  | J11, H11, G11, E11                           | O        | LV <sub>DD</sub> | 5, 9, 18 |

Table 43. MPC8541E Pinout Listing (continued)

| Signal                          | Package Pin Number               | Pin Type | Power Supply     | Notes    |
|---------------------------------|----------------------------------|----------|------------------|----------|
| TSEC2_TX_EN                     | B11                              | O        | LV <sub>DD</sub> | 11       |
| TSEC2_TX_ER                     | D11                              | O        | LV <sub>DD</sub> |          |
| TSEC2_TX_CLK                    | D10                              | I        | LV <sub>DD</sub> |          |
| TSEC2_GTX_CLK                   | C10                              | O        | LV <sub>DD</sub> |          |
| TSEC2_CRS                       | D9                               | I        | LV <sub>DD</sub> |          |
| TSEC2_COL                       | F8                               | I        | LV <sub>DD</sub> |          |
| TSEC2_RXD[7:0]                  | F9, E9, C9, B9, A9, H9, G10, F10 | I        | LV <sub>DD</sub> |          |
| TSEC2_RX_DV                     | H8                               | I        | LV <sub>DD</sub> |          |
| TSEC2_RX_ER                     | A8                               | I        | LV <sub>DD</sub> |          |
| TSEC2_RX_CLK                    | E10                              | I        | LV <sub>DD</sub> |          |
| <b>DUART</b>                    |                                  |          |                  |          |
| UART_CTS[0,1]                   | Y2, Y3                           | I        | OV <sub>DD</sub> |          |
| UART_RTS[0,1]                   | Y1, AD1                          | O        | OV <sub>DD</sub> |          |
| UART_SIN[0,1]                   | P11, AD5                         | I        | OV <sub>DD</sub> |          |
| UART_SOUT[0,1]                  | N6, AD2                          | O        | OV <sub>DD</sub> |          |
| <b>I<sup>2</sup>C interface</b> |                                  |          |                  |          |
| IIC_SDA                         | AH22                             | I/O      | OV <sub>DD</sub> | 4, 19    |
| IIC_SCL                         | AH23                             | I/O      | OV <sub>DD</sub> | 4, 19    |
| <b>System Control</b>           |                                  |          |                  |          |
| HRESET                          | AH16                             | I        | OV <sub>DD</sub> |          |
| HRESET_REQ                      | AG20                             | O        | OV <sub>DD</sub> | 18       |
| SRESET                          | AF20                             | I        | OV <sub>DD</sub> |          |
| CKSTP_IN                        | M11                              | I        | OV <sub>DD</sub> |          |
| CKSTP_OUT                       | G1                               | O        | OV <sub>DD</sub> | 2, 4     |
| <b>Debug</b>                    |                                  |          |                  |          |
| TRIG_IN                         | N12                              | I        | OV <sub>DD</sub> |          |
| TRIG_OUT/READY                  | G2                               | O        | OV <sub>DD</sub> | 6, 9, 18 |
| MSRCID[0:1]                     | J9, G3                           | O        | OV <sub>DD</sub> | 5, 6, 9  |
| MSRCID[2:3]                     | F3, F5                           | O        | OV <sub>DD</sub> | 6        |
| MSRCID4                         | F2                               | O        | OV <sub>DD</sub> | 6        |
| MDVAL                           | F4                               | O        | OV <sub>DD</sub> | 6        |

Table 43. MPC8541E Pinout Listing (continued)

| Signal                          | Package Pin Number | Pin Type                   | Power Supply       | Notes |
|---------------------------------|--------------------|----------------------------|--------------------|-------|
| <b>Clock</b>                    |                    |                            |                    |       |
| SYSCLK                          | AH21               | I                          | OV <sub>DD</sub>   |       |
| RTC                             | AB23               | I                          | OV <sub>DD</sub>   |       |
| CLK_OUT                         | AF22               | O                          | OV <sub>DD</sub>   |       |
| <b>JTAG</b>                     |                    |                            |                    |       |
| TCK                             | AF21               | I                          | OV <sub>DD</sub>   |       |
| TDI                             | AG21               | I                          | OV <sub>DD</sub>   | 12    |
| TDO                             | AF19               | O                          | OV <sub>DD</sub>   | 11    |
| TMS                             | AF23               | I                          | OV <sub>DD</sub>   | 12    |
| $\overline{\text{TRST}}$        | AG23               | I                          | OV <sub>DD</sub>   | 12    |
| <b>DFT</b>                      |                    |                            |                    |       |
| $\overline{\text{LSSD\_MODE}}$  | AG19               | I                          | OV <sub>DD</sub>   | 20    |
| L1_TSTCLK                       | AB22               | I                          | OV <sub>DD</sub>   | 20    |
| L2_TSTCLK                       | AG22               | I                          | OV <sub>DD</sub>   | 20    |
| TEST_SEL0                       | AH20               | I                          | OV <sub>DD</sub>   | 3     |
| TEST_SEL1                       | AG26               | I                          | OV <sub>DD</sub>   | 3     |
| <b>Thermal Management</b>       |                    |                            |                    |       |
| THERM0                          | AG2                | —                          | —                  | 14    |
| THERM1                          | AH3                | —                          | —                  | 14    |
| <b>Power Management</b>         |                    |                            |                    |       |
| ASLEEP                          | AG18               |                            |                    | 9, 18 |
| <b>Power and Ground Signals</b> |                    |                            |                    |       |
| AV <sub>DD</sub> 1              | AH19               | Power for e500 PLL (1.2 V) | AV <sub>DD</sub> 1 |       |
| AV <sub>DD</sub> 2              | AH18               | Power for CCB PLL (1.2 V)  | AV <sub>DD</sub> 2 |       |
| AV <sub>DD</sub> 3              | AH17               | Power for CPM PLL (1.2 V)  | AV <sub>DD</sub> 3 |       |
| AV <sub>DD</sub> 4              | AF28               | Power for PCI1 PLL (1.2 V) | AV <sub>DD</sub> 4 |       |
| AV <sub>DD</sub> 5              | AE28               | Power for PCI2 PLL (1.2 V) | AV <sub>DD</sub> 5 |       |

Table 43. MPC8541E Pinout Listing (continued)

| Signal            | Package Pin Number   | Pin Type   | Power Supply      | Notes |
|-------------------|--|--|-------------------|-------|
| GND               | A12, A17, B3, B14, B20, B26, B27, C2, C4, C11, C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7 | —  | —                 |       |
| GV <sub>DD</sub>  | A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21  | Power for DDR<br>DRAM I/O<br>Voltage<br>(2.5 V)                        | GV <sub>DD</sub>  |       |
| LV <sub>DD</sub>  | A4, C5, E7, H10  | Reference<br>Voltage;<br>Three-Speed<br>Ethernet I/O<br>(2.5 V, 3.3 V) | LV <sub>DD</sub>  |       |
| MV <sub>REF</sub> | N27  | Reference<br>Voltage Signal;<br>DDR                                    | MV <sub>REF</sub> |       |
| No Connects       | AA24, AA25, AA3, AA4, AA7, AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3   | —  | —                 | 16    |
| OV <sub>DD</sub>  | D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4  | PCI, 10/100<br>Ethernet, and<br>other Standard<br>(3.3 V)              | OV <sub>DD</sub>  |       |
| RESERVED          | C1, T11, U11, AF1  | —  | —                 | 15    |
| SENSEVDD          | L12  | Power for Core<br>(1.2 V)  | V <sub>DD</sub>   | 13    |
| SENSEVSS          | K12  | —  | —                 | 13    |
| V <sub>DD</sub>   | M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14   | Power for Core<br>(1.2 V)  | V <sub>DD</sub>   |       |
| <b>CPM</b>        |  |  |                   |       |
| PA[8:31]          | J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2  | I/O  | OV <sub>DD</sub>  |       |

Table 43. MPC8541E Pinout Listing (continued)

| Signal              | Package Pin Number  | Pin Type | Power Supply     | Notes |
|---------------------|---|----------|------------------|-------|
| PB[18:31]           | P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7  | I/O      | OV <sub>DD</sub> |       |
| PC[0, 1, 4-29]      | R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8 | I/O      | OV <sub>DD</sub> |       |
| PD[7, 14-25, 29-31] | Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2                                   | I/O      | OV <sub>DD</sub> |       |

**Notes:**

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA\_REQ2 is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as DMA\_REQ2.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV<sub>DD</sub>.
3. This pin must always be pulled down to GND.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8541E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See [Section 15.2, “Platform/System PLL Ratio.”](#)
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the [Section 15.3, “e500 Core PLL Ratio.”](#)
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V<sub>DD</sub>/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV<sub>DD</sub> when using 64-bit buffer mode (pins PCI\_AD[63:32] and PCI2\_C\_BE[7:4]).
18. If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
19. Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OV<sub>DD</sub>.
20. These are test signals for factory use only and must be pulled up (100Ω to 1kΩ) to OV<sub>DD</sub> for normal machine operation.
21. If this signal is used as both an input and an output, a weak pull-up (~10kΩ) is required on this pin.
22. MSYNC\_IN and MSYNC\_OUT should be connected together for proper operation.

# 15 Clocking

This section describes the PLL configuration of the MPC8541E. Note that the platform clock is identical to the CCB clock.

## 15.1 Clock Ranges

[Table 44](#) provides the clocking specifications for the processor core and [Table 45](#) provides the clocking specifications for the memory bus.

**Table 44. Processor Core Clocking Specifications**

| Characteristic                | Maximum Processor Core Frequency |     |         |     |         |     |         |     |          |      | Unit | Notes   |
|-------------------------------|----------------------------------|-----|---------|-----|---------|-----|---------|-----|----------|------|------|---------|
|                               | 533 MHz                          |     | 600 MHz |     | 667 MHz |     | 833 MHz |     | 1000 MHz |      |      |         |
|                               | Min                              | Max | Min     | Max | Min     | Max | Min     | Max | Min      | Max  |      |         |
| e500 core processor frequency | 400                              | 533 | 400     | 600 | 400     | 667 | 400     | 833 | 400      | 1000 | MHz  | 1, 2, 3 |

**Notes:**

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

**Table 45. Memory Bus Clocking Specifications**

| Characteristic       | Maximum Processor Core Frequency |     | Unit | Notes   |
|----------------------|----------------------------------|-----|------|---------|
|                      | 533, 600, 667, 883, 1000 MHz     |     |      |         |
|                      | Min                              | Max |      |         |
| Memory bus frequency | 100                              | 166 | MHz  | 1, 2, 3 |

**Notes:**

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

## 15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in [Table 46](#).

There is no default for this PLL ratio; these signals must be pulled to the desired values.

For specifications on the PCI\_CLK, refer to the PCI 2.2 Specification.

**Table 46. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | Ratio Description                      |
|-----------------------------------|--|
| 0000                              | 16:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0001                              | Reserved                               |
| 0010                              | 2:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 0011                              | 3:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 0100                              | 4:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 0101                              | 5:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 0110                              | 6:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 0111                              | Reserved                               |
| 1000                              | 8:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 1001                              | 9:1 ratio CCB clock: SYSCLK (PCI bus)  |
| 1010                              | 10:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1011                              | Reserved                               |
| 1100                              | 12:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1101                              | Reserved                               |
| 1110                              | Reserved                               |
| 1111                              | Reserved                               |



## 15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

**Table 47. e500 Core to CCB Ratio**

| Binary Value of LALE, LGPL2 Signals | Ratio Description |
|-------------------------------------|-------------------|
| 00                                  | 2:1 e500 core:CCB |
| 01                                  | 5:2 e500 core:CCB |
| 10                                  | 3:1 e500 core:CCB |
| 11                                  | 7:2 e500 core:CCB |

## 15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

**Table 48. Frequency Options with Respect to Memory Bus Speeds**

| CCB to SYSCLK Ratio | SYSCLK (MHz)                 |     |     |     |     |     |     |     |     |
|---------------------|------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
|                     | 17                           | 25  | 33  | 42  | 67  | 83  | 100 | 111 | 133 |
|                     | Platform/CCB Frequency (MHz) |     |     |     |     |     |     |     |     |
| 2                   |                              |     |     |     |     |     | 200 | 222 | 267 |
| 3                   |                              |     |     |     | 200 | 250 | 300 | 333 |     |
| 4                   |                              |     |     |     | 267 | 333 |     |     |     |
| 5                   |                              |     |     | 208 | 333 |     |     |     |     |
| 6                   |                              |     | 200 | 250 |     |     |     |     |     |
| 8                   |                              | 200 | 267 | 333 |     |     |     |     |     |
| 9                   |                              | 225 | 300 |     |     |     |     |     |     |
| 10                  |                              | 250 | 333 |     |     |     |     |     |     |
| 12                  | 200                          | 300 |     |     |     |     |     |     |     |
| 16                  | 267                          |     |     |     |     |     |     |     |     |

## 16 Thermal

This section describes the thermal specifications of the MPC8541E.

### 16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8541E.

**Table 49. Package Thermal Characteristics**

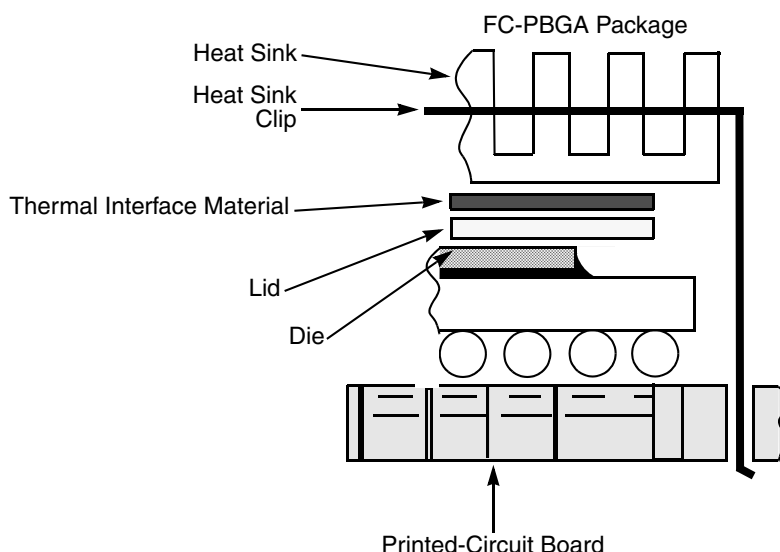
| Characteristic  | Symbol           | Value | Unit | Notes |
|---|------------------|-------|------|-------|
| Junction-to-ambient Natural Convection on four layer board (2s2p)       | $R_{\theta JMA}$ | 17    | °C/W | 1, 2  |
| Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p) | $R_{\theta JMA}$ | 14    | °C/W | 1, 2  |
| Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p) | $R_{\theta JMA}$ | 13    | °C/W | 1, 2  |
| Junction-to-board thermal   | $R_{\theta JB}$  | 10    | °C/W | 3     |
| Junction-to-case thermal  | $R_{\theta JC}$  | 0.96  | °C/W | 4     |

#### Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

### 16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 41. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.



**Figure 41. Package Exploded Cross-Sectional View with Several Heat Sink Options**

The system board designer can choose between several types of heat sinks to place on the MPC8541E. There are several commercially-available heat sinks from the following vendors:

|  |              |
|--|--------------|
| Aavid Thermalloy   | 603-224-9988 |
| 80 Commercial St.  |              |
| Concord, NH 03301  |              |
| Internet: <a href="http://www.aavidthermalloy.com">www.aavidthermalloy.com</a> |              |

|  |              |
|--|--------------|
| Alpha Novatech   | 408-749-7601 |
| 473 Sapena Ct. #15   |              |
| Santa Clara, CA 95054  |              |
| Internet: <a href="http://www.alphanovatech.com">www.alphanovatech.com</a> |              |

|  |              |
|--|--------------|
| International Electronic Research Corporation (IERC)           | 818-842-7277 |
| 413 North Moss St.   |              |
| Burbank, CA 91502  |              |
| Internet: <a href="http://www.ctscorp.com">www.ctscorp.com</a> |              |

|  |              |
|--|--------------|
| Millennium Electronics (MEI)   | 408-436-8770 |
| Loroco Sites   |              |
| 671 East Brokaw Road   |              |
| San Jose, CA 95112   |              |
| Internet: <a href="http://www.mei-millennium.com">www.mei-millennium.com</a> |              |

|  |              |
|--|--------------|
| Tyco Electronics   | 800-522-6752 |
| Chip Coolers™  |              |
| P.O. Box 3668  |              |
| Harrisburg, PA 17105-3668  |              |
| Internet: <a href="http://www.chipcoolers.com">www.chipcoolers.com</a> |              |

|  |              |
|--|--------------|
| Wakefield Engineering  | 603-635-5102 |
| 33 Bridge St.  |              |
| Pelham, NH 03076   |              |
| Internet: <a href="http://www.wakefield.com">www.wakefield.com</a> |              |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8541E to function in various environments.

## 16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8541E thermal model is shown in Figure 42. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

| Conductivity   | Value | Unit      |
|--|-------|-----------|
| <b>Lid<br/>(11 × 11 × 1 mm)</b>                                      |       |           |
| $k_x$  | 360   | W/(m × K) |
| $k_y$  | 360   |           |
| $k_z$  | 360   |           |
| <b>Lid Adhesive—Collapsed resistance<br/>(8.7 × 9.3 × 0.05 mm)</b>   |       |           |
| $k_z$  | 1.07  |           |
| <b>Die<br/>(8.7 × 9.3 × 0.75 mm)</b>                                 |       |           |
| <b>Bump/Underfill—Collapsed resistance<br/>(8.7 × 9.3 × 0.07 mm)</b> |       |           |
| $k_z$  | 4.4   |           |
| <b>Substrate and Solder Balls<br/>(25 × 25 × 1.6 mm)</b>             |       |           |
| $k_x$  | 14.2  |           |
| $k_y$  | 14.2  |           |
| $k_z$  | 1.2   |           |

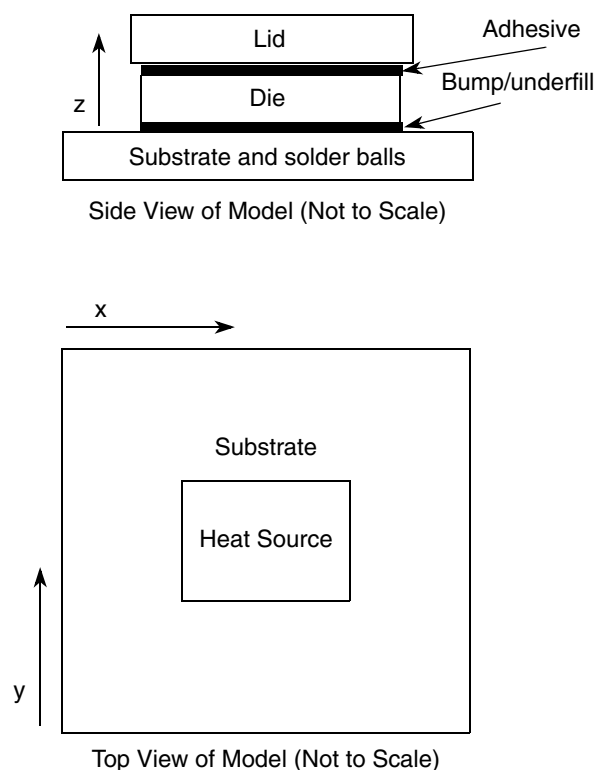


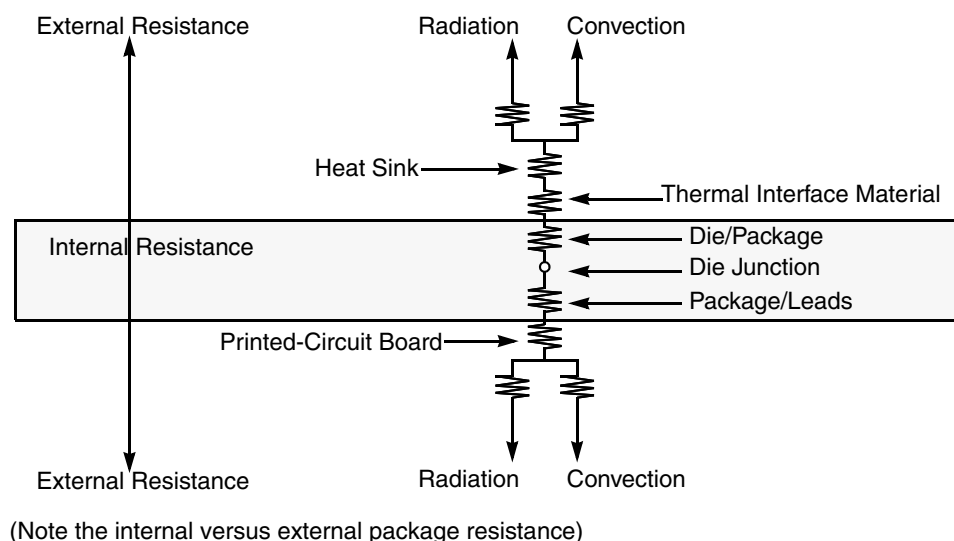
Figure 42. MPC8541E Thermal Model

## 16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 43 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



**Figure 43. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

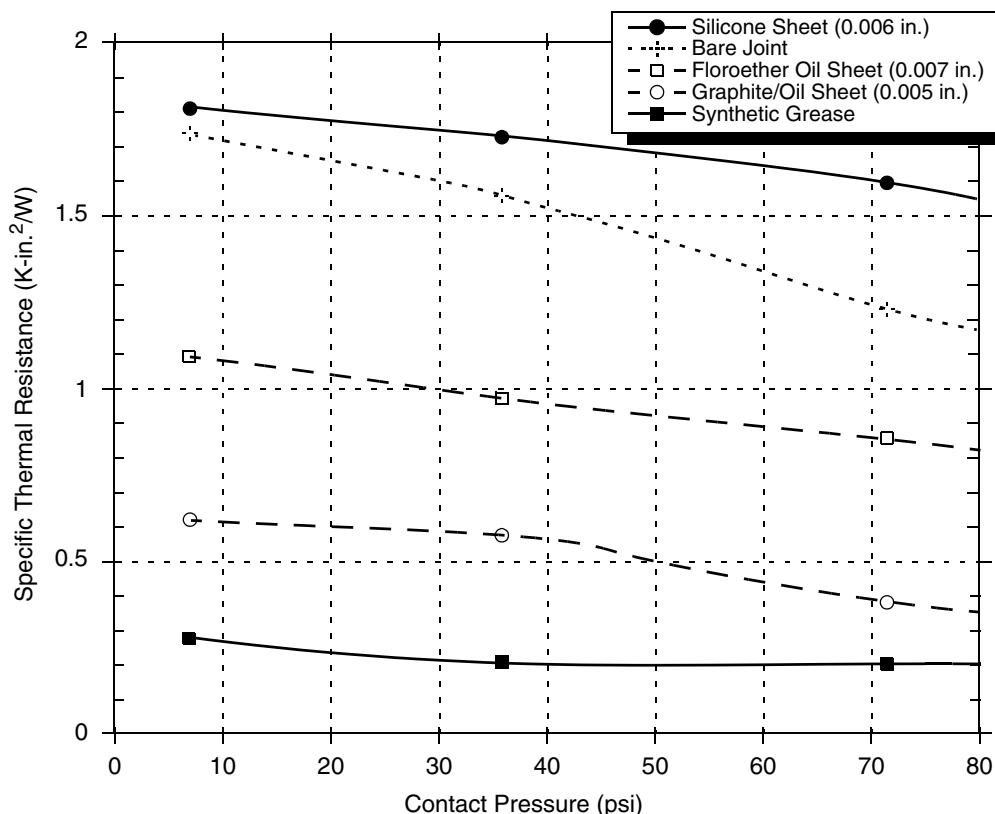
## 16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 44 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 40). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.



**Figure 44. Thermal Performance of Select Thermal Interface Materials**

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

|   |              |
|---|--------------|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01888-4014<br>Internet: <a href="http://www.chomerics.com">www.chomerics.com</a>   | 781-935-4850 |
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>2200 W. Salzburg Rd.<br>Midland, MI 48686-0997<br>Internet: <a href="http://www.dowcorning.com">www.dowcorning.com</a> | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: <a href="http://www.microsi.com">www.microsi.com</a>   | 888-642-7674 |
| The Bergquist Company<br>18930 West 78 <sup>th</sup> St.  | 800-347-4572 |

Chanhassen, MN 55317  
 Internet: [www.bergquistcompany.com](http://www.bergquistcompany.com)  
 Thermagon Inc.  
 4707 Detroit Ave.  
 Cleveland, OH 44102  
 Internet: [www.thermagon.com](http://www.thermagon.com)

888-246-9050

## 16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

### 16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

$T_J$  is the die-junction temperature

$T_I$  is the inlet cabinet ambient temperature

$T_R$  is the air temperature rise within the computer cabinet

$\theta_{JC}$  is the junction-to-case thermal resistance

$\theta_{INT}$  is the adhesive or interface material thermal resistance

$\theta_{SA}$  is the heat sink base-to-ambient thermal resistance

$P_D$  is the power dissipated by the device. See [Table 4](#) and [Table 5](#).

During operation the die-junction temperatures ( $T_J$ ) should be maintained within the range specified in [Table 2](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ( $T_A$ ) may range from 30° to 40°C. The air temperature rise within a cabinet ( $T_R$ ) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material ( $\theta_{INT}$ ) may be about 1°C/W. For the purposes of this example, the  $\theta_{JC}$  value given in [Table 49](#) that includes the thermal grease interface and is documented in note 4 is used. If a thermal pad is used,  $\theta_{INT}$  must be added.

Assuming a  $T_I$  of 30 °C, a  $T_R$  of 5 °C, a FC-PBGA package  $\theta_{JC} = 0.96$ , and a power consumption ( $P_D$ ) of 8.0 W, the following expression for  $T_J$  is obtained:

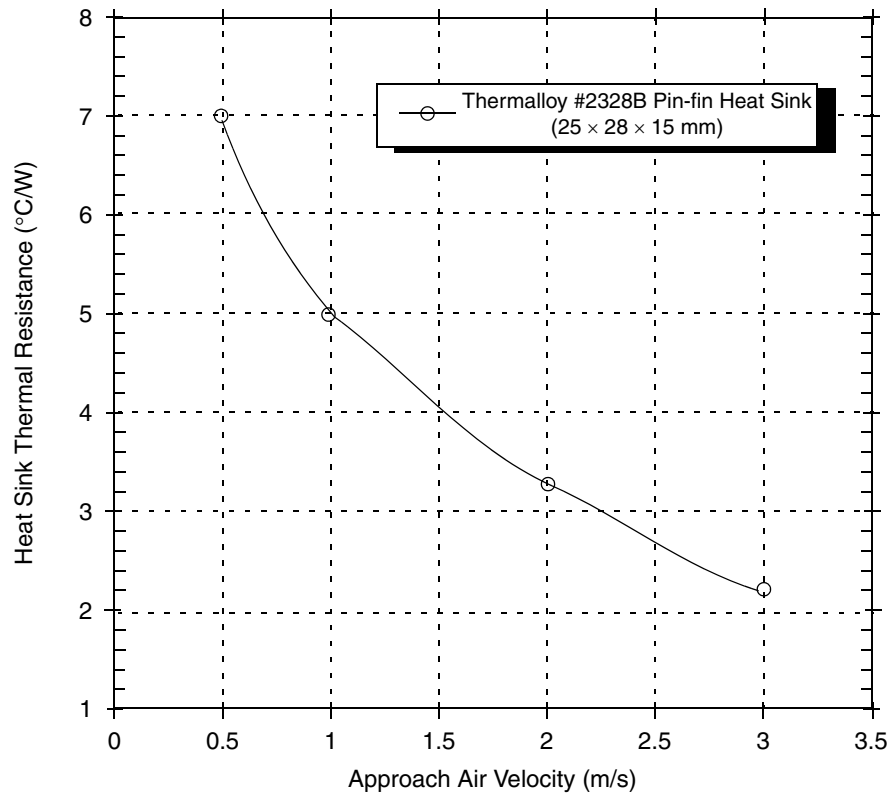
$$\text{Die-junction temperature: } T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + \theta_{SA}) \times 8.0 \text{ W}$$

The heat sink-to-ambient thermal resistance ( $\theta_{SA}$ ) versus airflow velocity for a Thermalloy heat sink #2328B is shown in [Figure 45](#).

Assuming an air velocity of 2 m/s, we have an effective  $\theta_{SA+}$  of about 3.3 °C/W, thus

$$T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + 3.3^\circ\text{C/W}) \times 8.0 \text{ W},$$

resulting in a die-junction temperature of approximately 69 °C which is well within the maximum operating temperature of the component.



**Figure 45. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

#### 16.2.4.2 Case 2

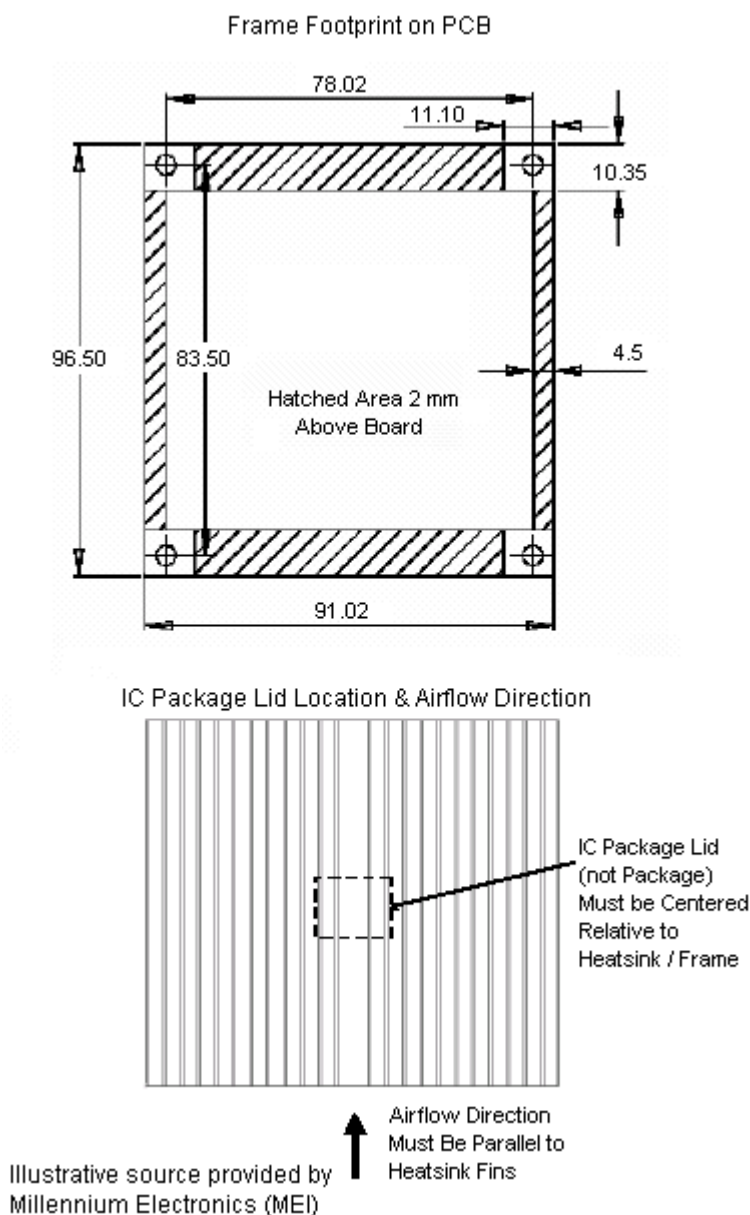
Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in [Table 49](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 46](#) and [Figure 47](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

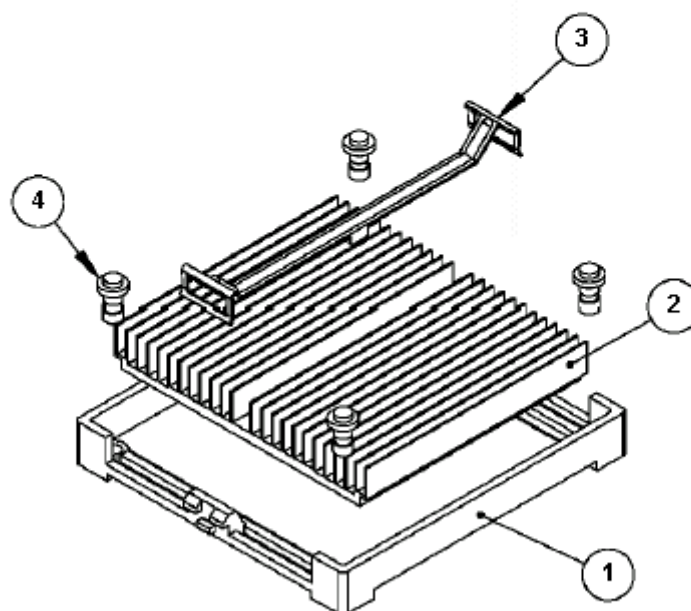


The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 46 and provide exploded views of the plastic fence, heat sink, and spring clip.



**Figure 46. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence**

| Item No | QTY | MEI PN      | Description           |
|---------|-----|-------------|-----------------------|
| 1       | 1   | MFRAME-2000 | HEATSINK FRAME        |
| 2       | 1   | MSNK-1120   | EXTRUDED HEATSINK     |
| 3       | 1   | MCLIP-1013  | CLIP                  |
| 4       | 4   | MPPINS-1000 | FRAME ATTACHMENT PINS |



Illustrative source provided by  
Millennium Electronics (MEI)

**Figure 47. Exploded Views (2) of a Heat Sink Attachment using a Plastic Force**

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

## 17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8541E.

### 17.1 System Clocking

The MPC8541E includes five PLLs.

1. The platform PLL ( $AV_{DD1}$ ) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL ( $AV_{DD2}$ ) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL ( $AV_{DD3}$ ) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL ( $AV_{DD4}$ ) generates the clocking for the first PCI bus.
5. The PCI2 PLL ( $AV_{DD5}$ ) generates the clock for the second PCI bus.

### 17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ( $AV_{DD1}$ ,  $AV_{DD2}$ ,  $AV_{DD3}$ ,  $AV_{DD4}$ , and  $AV_{DD5}$  respectively). The  $AV_{DD}$  level should always be equivalent to  $V_{DD}$ , and preferably these voltages will be derived directly from  $V_{DD}$  through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 48](#), one to each of the five  $AV_{DD}$  pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific  $AV_{DD}$  pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 48 shows the PLL power supply filter circuit.

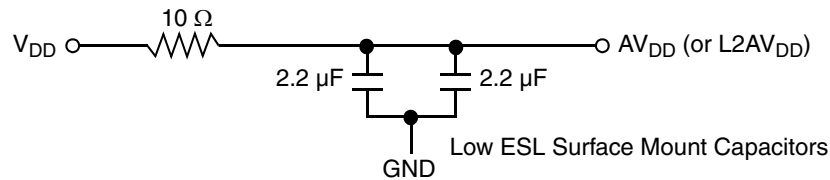


Figure 48. PLL Power Supply Filter Circuit

## 17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8541E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8541E system, and the MPC8541E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  pins of the MPC8541E. These decoupling capacitors should receive their power from separate  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1  $\mu\text{F}$ . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330  $\mu\text{F}$  (AVX TPS tantalum or Sanyo OSCON).

## 17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to  $OV_{DD}$ ,  $GV_{DD}$ , or  $LV_{DD}$  as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

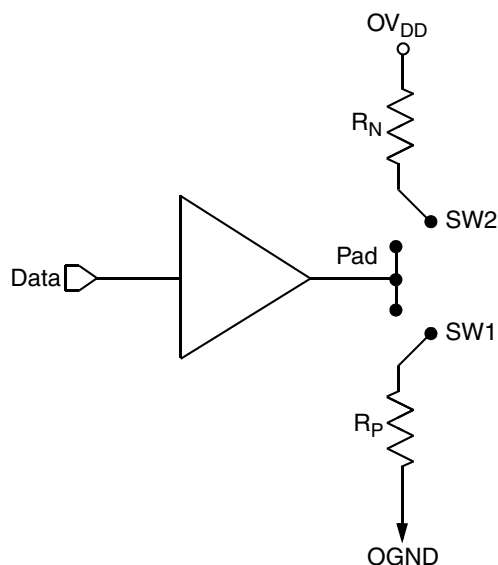
Power and ground connections must be made to all external  $V_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ ,  $OV_{DD}$ , and GND pins of the MPC8541E.

## 17.5 Output Buffer DC Impedance

The MPC8541E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for  $I^2\text{C}$ ).

To measure  $Z_0$  for the single-ended drivers, an external resistor is connected from the chip pad to  $OV_{DD}$  or GND. Then, the value of each resistor is varied until the pad voltage is  $OV_{DD}/2$  (see Figure 49). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices.

When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N)/2$ .



**Figure 49. Driver Impedance Measurement**

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is  $V_2 = 1/(1/R_1 + 1/R_2) \times I_{source}$ . Solving for the output impedance gives  $R_{source} = R_{term} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{source} = V_1/R_{source}$ .

[Table 50](#) summarizes the signal impedance targets. The driver impedance are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

**Table 50. Impedance Characteristics**

| Impedance    | Local Bus, Ethernet, UART, Control, Configuration, Power Management | PCI       | DDR DRAM  | Symbol     | Unit     |
|--------------|---|-----------|-----------|------------|----------|
| $R_N$        | 43 Target   | 25 Target | 20 Target | $Z_0$      | $\Omega$ |
| $R_P$        | 43 Target   | 25 Target | 20 Target | $Z_0$      | $\Omega$ |
| Differential | NA  | NA        | NA        | $Z_{DIFF}$ | $\Omega$ |

**Note:** Nominal supply voltages. See [Table 1](#),  $T_j = 105^\circ\text{C}$ .

## 17.6 Configuration Pin Multiplexing

The MPC8541E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k $\Omega$ . This value should permit the 4.7-k $\Omega$  resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform/system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 17.7 Pull-Up Resistor Requirements

The MPC8541E requires high resistance pull-up resistors (10 k $\Omega$  is recommended) on open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 51](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1\_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

## 17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The  $\overline{\text{TRST}}$  signal is optional in the IEEE Std 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires  $\overline{\text{TRST}}$  to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert  $\overline{\text{TRST}}$  during the power-on reset flow. Simply tying  $\overline{\text{TRST}}$  to  $\overline{\text{HRESET}}$  is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$  in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 50](#) allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in [Figure 50](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in [Figure 50](#) is common to all known emulators.

|                                      |    |               |                                     |
|--------------------------------------|----|---------------|-------------------------------------|
| COP_TDO                              | 1  | 2             | NC                                  |
| COP_TDI                              | 3  | 4             | $\overline{\text{COP\_TRST}}$       |
| NC                                   | 5  | 6             | COP_VDD_SENSE                       |
| COP_TCK                              | 7  | 8             | $\overline{\text{COP\_CHKSTP\_IN}}$ |
| COP_TMS                              | 9  | 10            | NC                                  |
| $\overline{\text{COP\_SRESET}}$      | 11 | 12            | NC                                  |
| $\overline{\text{COP\_HRESET}}$      | 13 | KEY<br>No pin |                                     |
| $\overline{\text{COP\_CHKSTP\_OUT}}$ | 15 | 16            | GND                                 |

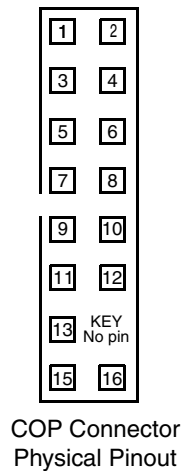
Figure 50. COP Connector Physical Pinout

### 17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$  should be tied to  $\overline{\text{HRESET}}$  through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal ( $\overline{\text{HRESET}}$ ) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 51. If this is not possible, the isolation resistor will allow future access to  $\overline{\text{TRST}}$  in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV<sub>DD</sub> through a 10 k $\Omega$  resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.





1. The COP port and target board should be able to independently assert  $\overline{\text{HRESET}}$  and  $\overline{\text{TRST}}$  to the processor in order to fully control the processor as shown here.
2. Populate this with a 10  $\Omega$  resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the  $\overline{\text{TRST}}$  line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting  $\overline{\text{SRESET}}$  causes a machine check interrupt to the e500 core.

### Figure 51. JTAG Interface Connection

## 18 Document Revision History

Table 51 provides a revision history for this hardware specification.

**Table 51. Document Revision History**

| Rev. No. | Date      | Substantive Change(s)   |
|----------|-----------|---|
| 4        |           | Updated <a href="#">Section 2.1.2, “Power Sequencing.”</a><br>Updated back page information.  |
| 3.2      | 11/2006   | Updated <a href="#">Section 2.1.2, “Power Sequencing.”</a><br>Replaced <a href="#">Section 17.8, “JTAG Configuration Signals.”</a>  |
| 3.1      | 10/2005   | <a href="#">Table 4</a> : Added footnote 2 about junction temperature.<br><a href="#">Table 4</a> : Added max. power values for 1000 MHz core frequency.<br>Removed <a href="#">Figure 6, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.”</a><br><a href="#">Table 30</a> : Modified note to $t_{LBKSKEW}$ from 8 to 9<br><a href="#">Table 30</a> : Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values.<br><a href="#">Table 30</a> : Added note 3 to $t_{LBKHOV1}$ .<br><a href="#">Table 30</a> and <a href="#">Table 31</a> : Modified note 3.<br><a href="#">Table 31</a> : Added note 3 to $t_{LBKLOV1}$ .<br><a href="#">Table 31</a> : Modified values for $t_{LBKHKT}$ , $t_{LBKLOV1}$ , $t_{LBKLOV2}$ , $t_{LBKLOV3}$ , $t_{LBKLOZ1}$ , and $t_{LBKLOZ2}$ .<br><a href="#">Figure 20</a> : Changed Input Signals: LAD[0:31]/LDP[0:3].<br><a href="#">Table 43</a> : Modified note for signal CLK_OUT.<br><a href="#">Table 43</a> : PCI1_CLK and PCI2_CLK changed from I/O to I.<br><a href="#">Table 52</a> : Added column for Encryption Acceleration. |
| 3        | 8/29/2005 | <a href="#">Table 4</a> : Modified max. power values.<br><a href="#">Table 43</a> : Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, and MDVAL.  |
| 2        | 8/2005    | Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as <a href="#">Table 27</a> and Table 31 is now listed as <a href="#">Table 31</a> .<br><a href="#">Table 7</a> : Added note 2.<br><a href="#">Table 14</a> : Modified min and max values for $t_{DDKHMP}$   |
| 1        | 6/2005    | <a href="#">Table 27</a> : Changed $LV_{dd}$ to $OV_{dd}$ for the supply voltage Ethernet management interface.<br><a href="#">Table 4</a> : Modified footnote 4 and changed typical power for the 1000MHz core frequency.<br><a href="#">Table 31</a> : Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state.  |
| 0        | 6/2005    | Initial Release.  |

## 19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in [Section 19.1, “Nomenclature of Parts Fully Addressed by this Document.”](#)

## 19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8541E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 52. Part Numbering Nomenclature**

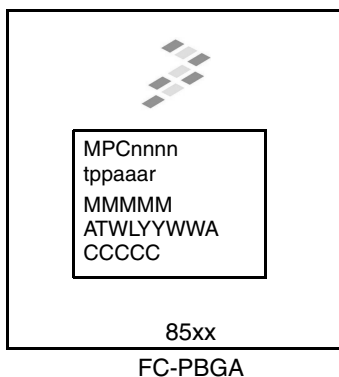
| MPC          | nnnn            |                                      | t                                      | pp                                       | aa  | a   | r                           |
|--------------|-----------------|--------------------------------------|--|--|---|---|-----------------------------|
| Product Code | Part Identifier | Encryption Acceleration              | Temperature Range <sup>1</sup>         | Package <sup>2</sup>                     | Processor Frequency <sup>3</sup>  | Platform Frequency                        | Revision Level <sup>4</sup> |
| MPC          | 8541            | Blank = not included<br>E = included | Blank = 0 to 105°C<br>C = -40 to 105°C | PX = FC-PBGA<br>VT = FC-PBGA (lead free) | AJ = 533 MHz<br>AK = 600 MHz<br>AL = 667 MHz<br>AP = 833 MHz<br>AQ = 1000 MHz | D = 266 MHz<br>E = 300 MHz<br>F = 333 MHz |                             |

**Notes:**

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See Section 14, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).

## 19.2 Part Marking

Parts are marked as the example shown in Figure 52.



**Notes:**

- MMMMM is the 5-digit mask number.
- ATWLYYWWA is the traceability code.
- CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 52. Part Marking for FC-PBGA Device**

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Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku  
Tokyo 153-0064  
Japan  
0120 191014 or  
+81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor  
Literature Distribution Center  
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