June 2011

FDS89161LZ

Dual N-Channel PowerTrench® MOSFET

100 V, 2.7 A, 105 mΩ

Features

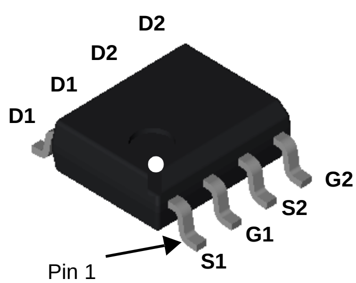
- Max $r_{DS(on)}$ = 105 mΩ at V_{GS} = 10 V, I_D = 2.7 A
- Max $r_{DS(on)}$ = 160 mΩ at V_{GS} = 4.5 V, I_D = 2.1 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- CDM ESD protection level > 2KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

General Description

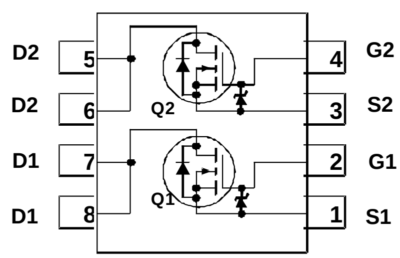
This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced Power Trench® process that has been special tailored to minimize the on-state resisitance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

Application

- DC-DC conversion



SO-8



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous	2.7	A
	-Pulsed	15	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	13	mJ
P_D	Power Dissipation T_C = 25 °C	31	W
	Power Dissipation T_A = 25 °C (Note1a)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

Package Marking and Ordering Information

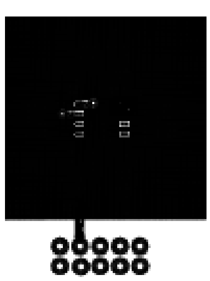
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS89161LZ	FDS89161LZ	SO-8	13 ”	12 mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

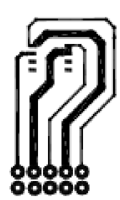
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		68		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.7	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.7 A		81	105	mΩ
		V_{GS} = 4.5 V, I_D = 2.1 A		110	160	
		V_{GS} = 10 V, I_D = 2.7 A, T_J = 125 °C		140	182	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 2.7 A		7.8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1MHz		227	302	pF
C_{oss}	Output Capacitance			44	58	pF
C_{rss}	Reverse Transfer Capacitance			3	4	pF
R_g	Gate Resistance			0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 2.7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		3.8	10	ns
t_r	Rise Time			1.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			9.5	17	ns
t_f	Fall Time			1.6	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 2.7 A		3.8	5.3	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 2.7 A		2.1	2.9	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 2.7 A		0.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.7 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 2.7 A, di/dt = 100 A/μs		31	56	ns
Q_{rr}	Reverse Recovery Charge			20	36	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 135°C/W when mounted on a minimun pad

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3. Starting TJ = 25 °C, L = 0.3 mH, IAS =25 A, VDD = 27 V, VGS = 10V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

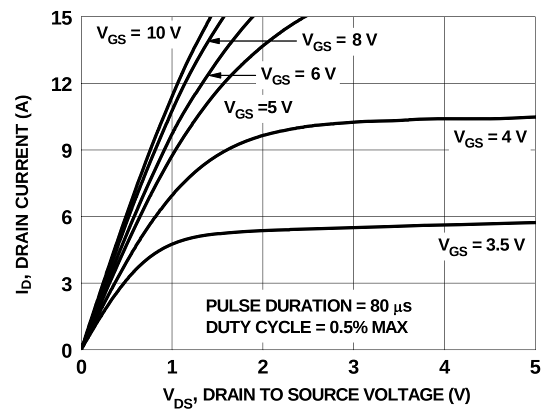


Figure 1. On-Region Characteristics

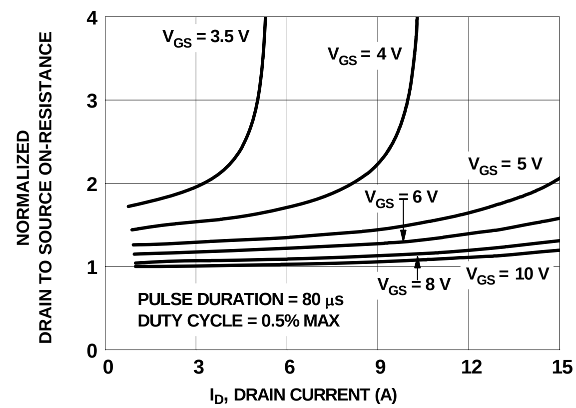


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

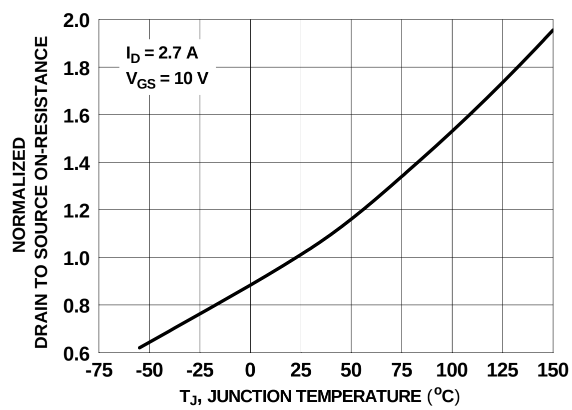


Figure 3. Normalized On-Resistance vs Junction Temperature

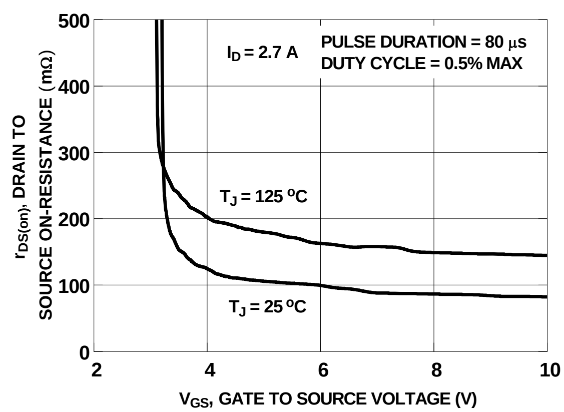


Figure 4. On-Resistance vs Gate to Source Voltage

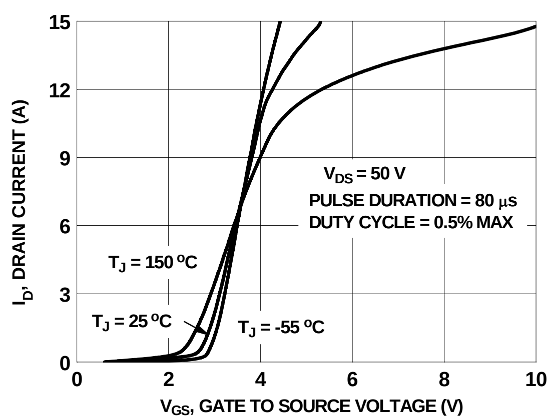


Figure 5. Transfer Characteristics

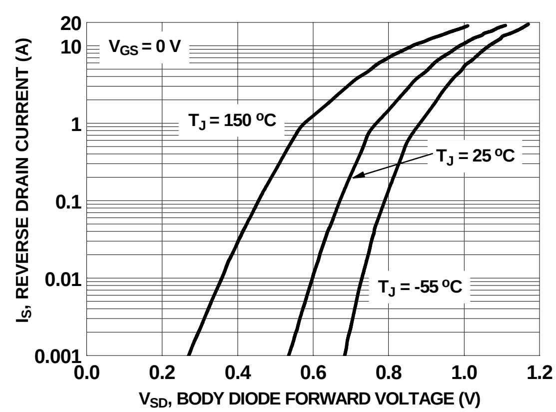


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

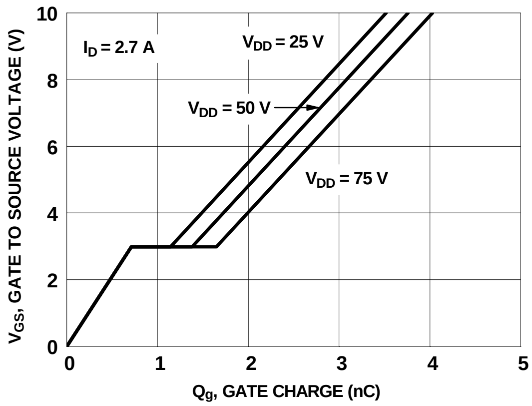


Figure 7. Gate Charge Characteristics

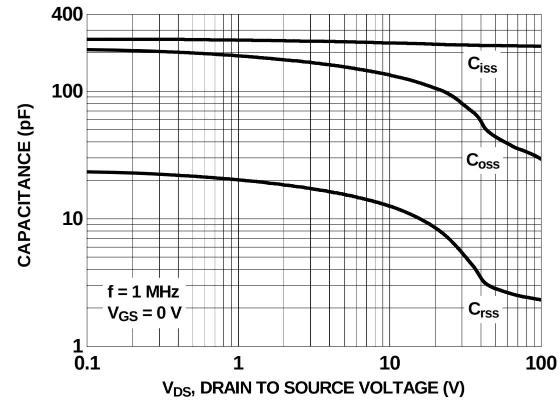


Figure 8. Capacitance vs Drain to Source Voltage

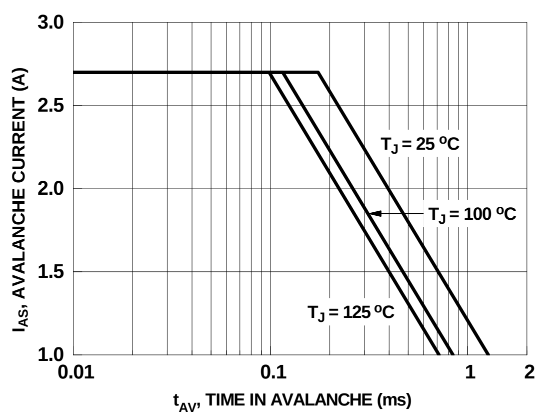


Figure 9. Unclamped Inductive Switching Capability

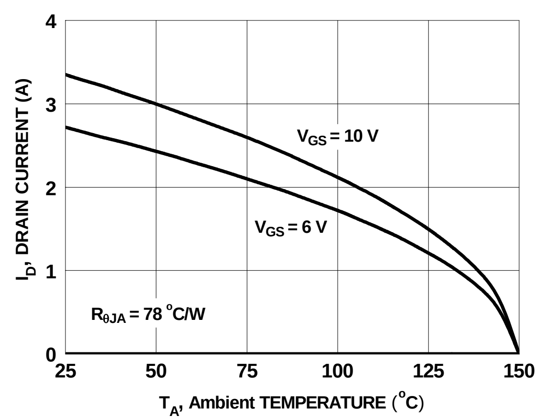


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

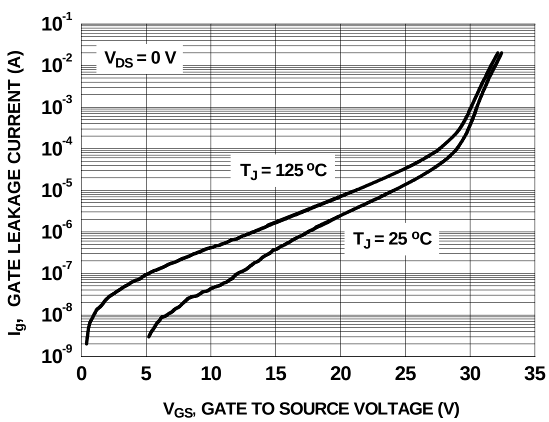


Figure 11. Gate Leakage Current vs Gate to Source Voltage

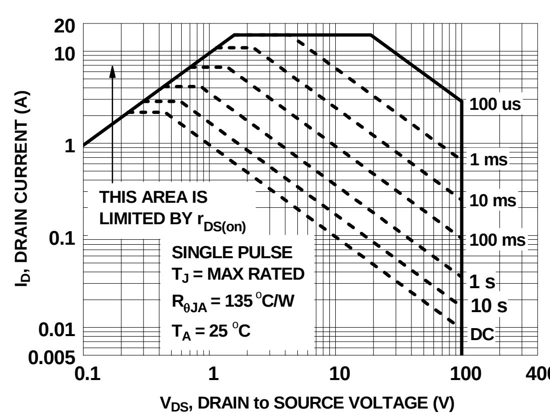


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics (N-Channel) T_J = 25°C unless otherwise noted

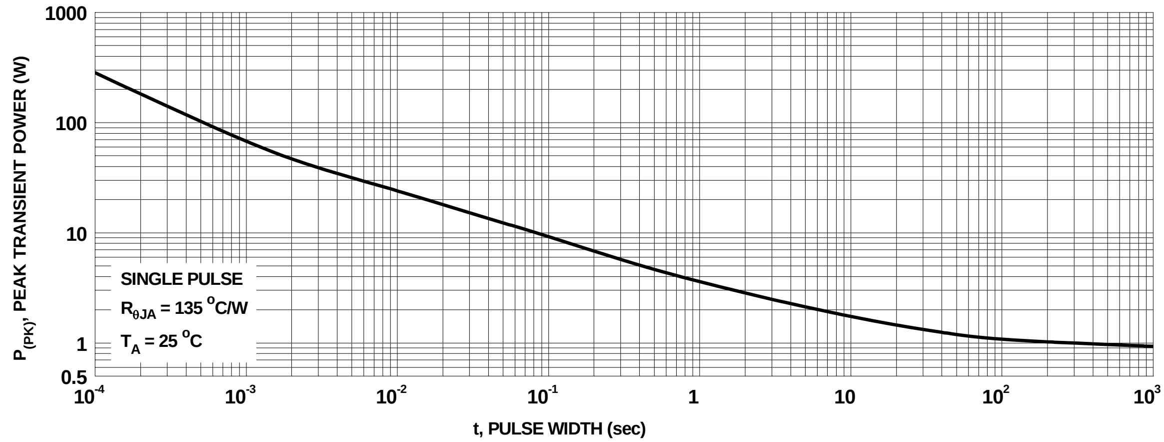


Figure 13. Single Pulse Maximum Power Dissipation

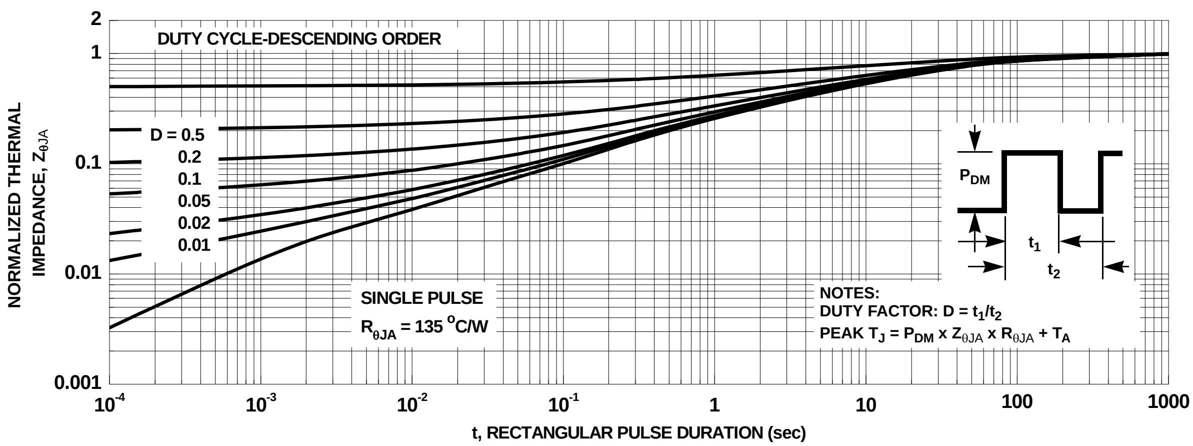


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

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