

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC174FN

Hex D-Type Flip Flop with Clear

The TC74AC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

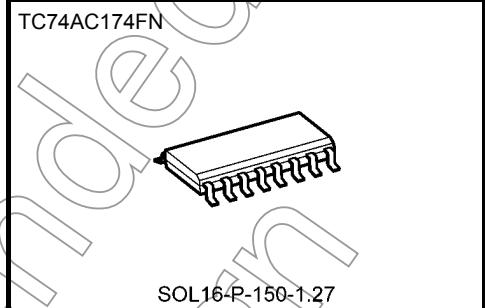
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the CLR input is held low, the Q output are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Note: xxxFN (JEDEC SOP) is not available in Japan.



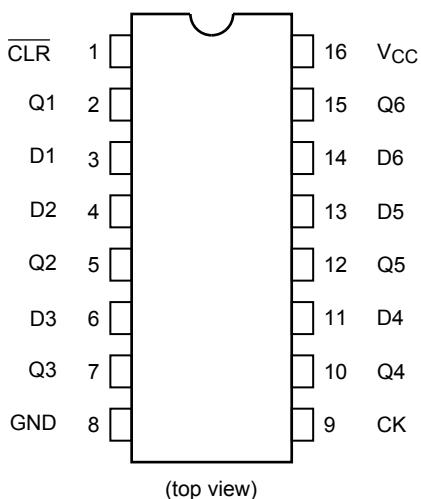
Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

Features

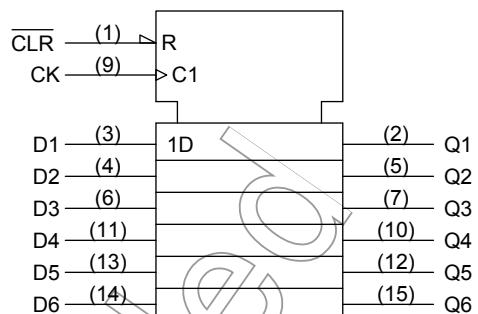
- High speed: $f_{max} = 180$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC(\text{opr})} = 2$ to 5.5 V
- Pin and function compatible with 74F174

Not for New Design

Pin Assignment



IEC Logic Symbol

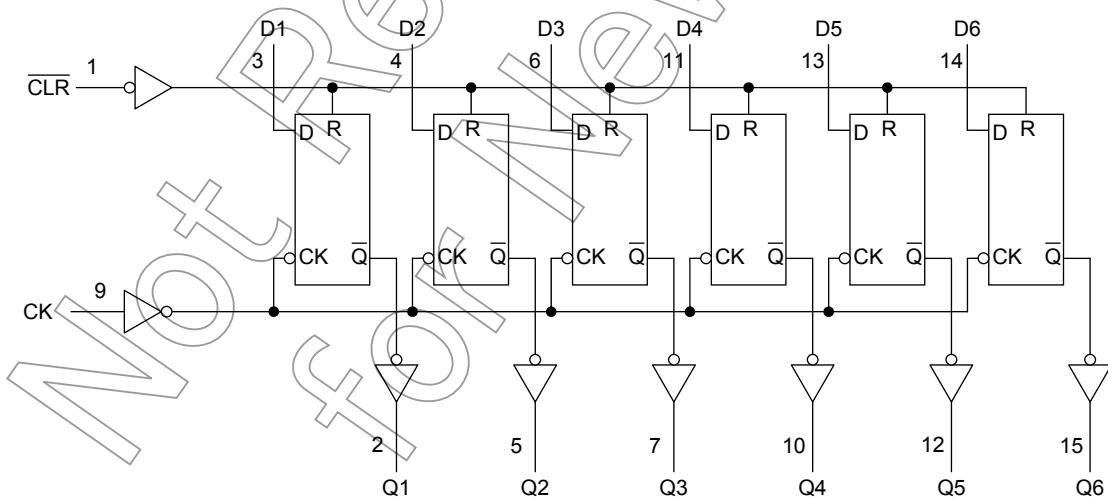


Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 150	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{OPR}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—	2.0	1.50	—	—	1.50	—	V
			3.0	2.10	—	—	2.10	—	
			5.5	3.85	—	—	3.85	—	
Low-level input voltage	V _{IL}	—	2.0	—	—	0.50	—	0.50	V
			3.0	—	—	0.90	—	0.90	
			5.5	—	—	1.65	—	1.65	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	2.0	1.9	2.0	—	1.9	V
			I _{OH} = -4 mA	3.0	2.9	3.0	—	2.9	
			I _{OH} = -24 mA	4.5	4.4	4.5	—	4.4	
			I _{OH} = -75 mA (Note)	3.0	2.58	—	—	2.48	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	2.0	—	0.0	0.1	—	V
			I _{OL} = 12 mA	3.0	—	0.0	0.1	—	
			I _{OL} = 24 mA	4.5	—	0.0	0.1	—	
			I _{OL} = 75 mA (Note)	5.5	—	—	—	—	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	µA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C		Unit
			V _{CC} (V)	Limit	Limit			
Minimum pulse width (CK)	t _w (L) t _w (H)	—	3.3 ± 0.3	7.0	7.0	ns	ns	ns
			5.0 ± 0.5	5.0	5.0			
Minimum pulse width (CLR)	t _w (L)	—	3.3 ± 0.3	7.0	7.0	ns	ns	ns
			5.0 ± 0.5	5.0	5.0			
Minimum set-up time	t _s	—	3.3 ± 0.3	7.0	7.0	ns	ns	ns
			5.0 ± 0.5	4.0	4.0			
Minimum hold time	t _h	—	3.3 ± 0.3	1.0	1.0	ns	ns	ns
			5.0 ± 0.5	1.0	1.0			
Minimum removal time (CLR)	t _{rem}	—	3.3 ± 0.3	6.0	6.0	ns	ns	ns
			5.0 ± 0.5	3.5	3.5			

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{PLH}	—	3.3 ± 0.3	—	8.5	14.4	1.0	16.6	ns
	t_{PHL}		5.0 ± 0.5	—	6.7	9.6	1.0	11.0	
Propagation delay time (CLR-Q)	t_{PHL}	—	3.3 ± 0.3	—	8.2	13.9	1.0	16.0	ns
			5.0 ± 0.5	—	6.3	9.0	1.0	10.4	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	60	110	—	60	—	MHz
Input capacitance	C_{IN}	—	5.0 ± 0.5	90	150	—	90	—	—
Power dissipation capacitance	C_{PD}	(Note)		—	74	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

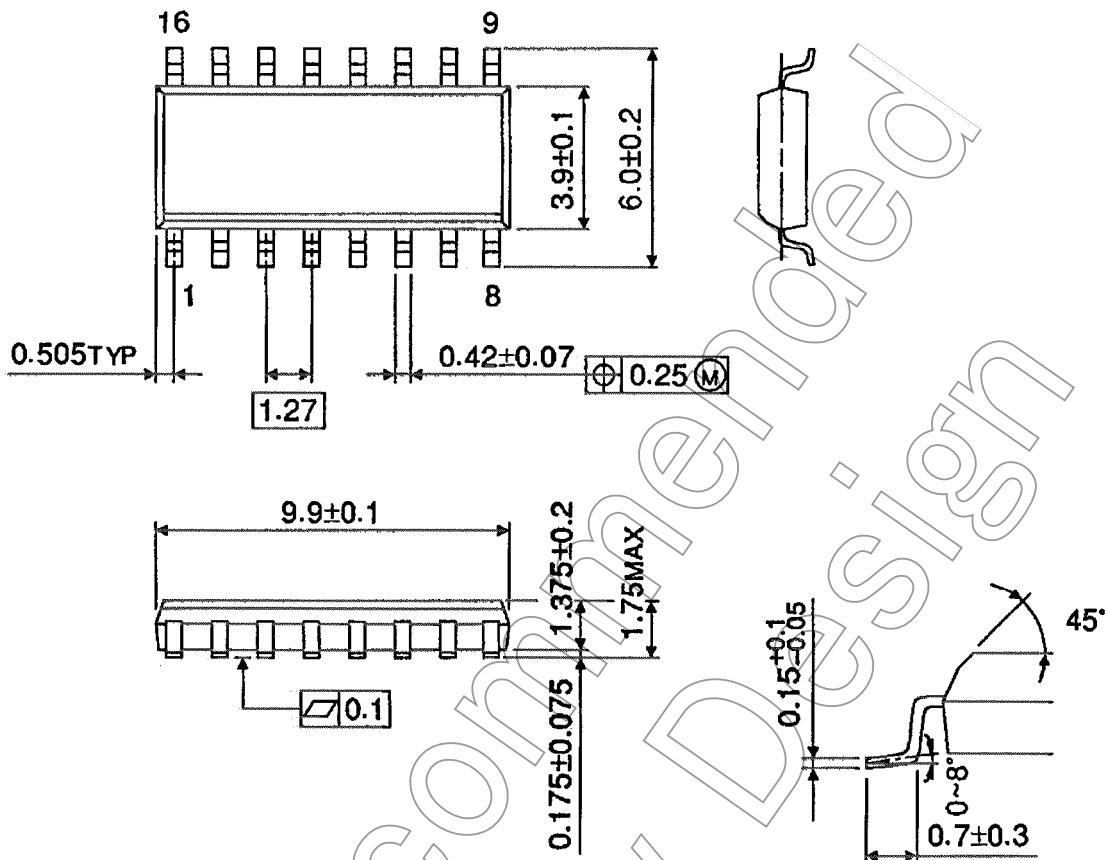
And the total C_{PD} when n pcs of flip flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 34 + 40 \cdot n$$

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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