

# **SP623**

# **Spartan-6 FPGA**

# **GTP Transceiver**

# **Characterization Board**

## ***User Guide***

UG751 (v1.1) September 15, 2010



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## Revision History

The following table shows the revision history for this document.

| Date     | Version | Revision                                                                                                                                                                                                                                                                                            |
|----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 05/22/10 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                             |
| 09/15/10 | 1.1     | Added information about the Intersil power module to the paragraphs under <a href="#">GTP Transceiver Power Module, page 13</a> , and to <a href="#">Table 1-2</a> . Removed spaces between net names and associated closing quote marks in the <a href="#">SP623 Master UCF Listing, page 39</a> . |

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# About This Guide

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This document describes the basic setup, features, and operation of the SP623 Spartan-6® FPGA GTP transceiver characterization board. The SP623 board provides the hardware environment for characterizing and evaluating the GTP transceivers available on the Spartan-6 XC6SLX150T-3FGG676 FPGA.

## Guide Contents

This user guide contains the following chapters and appendices:

- [Chapter 1, SP623 Board Features and Operation](#) describes the components, features, and operation of the SP623 Spartan-6 FPGA GTP transceiver characterization board.
- [Appendix A, Default Jumper Positions](#) lists the jumpers that must be installed on the board for proper operation.
- [Appendix B, VITA 57.1 FMC HPC Connector Pinout](#) provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- [Appendix C, SP623 Master UCF Listing](#) provides a listing of the SP623 master user constraints file (UCF).
- [Appendix D, References](#) provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

## Conventions

This document uses the following conventions. An example illustrates each convention.

### Typographical

The following typographical conventions are used in this document:

| Convention            | Meaning or Use                                                   | Example                                                                                            |
|-----------------------|------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| Courier font          | Messages, prompts, and program files that the system displays    | speed grade: - 100                                                                                 |
| <b>Courier bold</b>   | Literal commands that you enter in a syntactical statement       | <b>ngdbuild</b> <i>design_name</i>                                                                 |
| <b>Helvetica bold</b> | Commands that you select from a menu                             | <b>File → Open</b>                                                                                 |
|                       | Keyboard shortcuts                                               | <b>Ctrl+C</b>                                                                                      |
| <i>Italic font</i>    | Variables in a syntax statement for which you must supply values | <b>ngdbuild</b> <i>design_name</i>                                                                 |
|                       | References to other manuals                                      | See the <i>Command Line Tools User Guide</i> for more information.                                 |
|                       | Emphasis in text                                                 | If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected. |

## Online Document

The following conventions are used in this document:

| Convention                            | Meaning or Use                                             | Example                                                                                                                                                       |
|---------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Blue text                             | Cross-reference link to a location in the current document | See the section “ <a href="#">Additional Resources</a> ” for details.<br>Refer to “ <a href="#">Title Formats</a> ” in <a href="#">Chapter 1</a> for details. |
| <a href="#">Blue, underlined text</a> | Hyperlink to a website (URL)                               | Go to <a href="http://www.xilinx.com">http://www.xilinx.com</a> for the latest speed files.                                                                   |

## *SP623 Board Features and Operation*

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This chapter describes the components, features, and operation of the SP623 Spartan®-6 FPGA GTP transceiver characterization board. The SP623 board provides the hardware environment for characterizing and evaluating the GTP transceivers available on the Spartan-6 XC6SLX150T-3FGG676 FPGA.

### SP623 Board Features

- Spartan-6 XC6SLX150T-3FGG676 FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Power module supporting all Spartan-6 FPGA GTP transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- One pair of global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- 16 pairs of SMA connectors for the GTP transceivers
- 8 pairs of SMA connectors for GTP transceiver clock inputs
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FMC HPC connectors
- USB to UART bridge
- I<sup>2</sup>C Bus

The SP623 board block diagram is shown in [Figure 1-1](#).

**Caution!** The SP623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

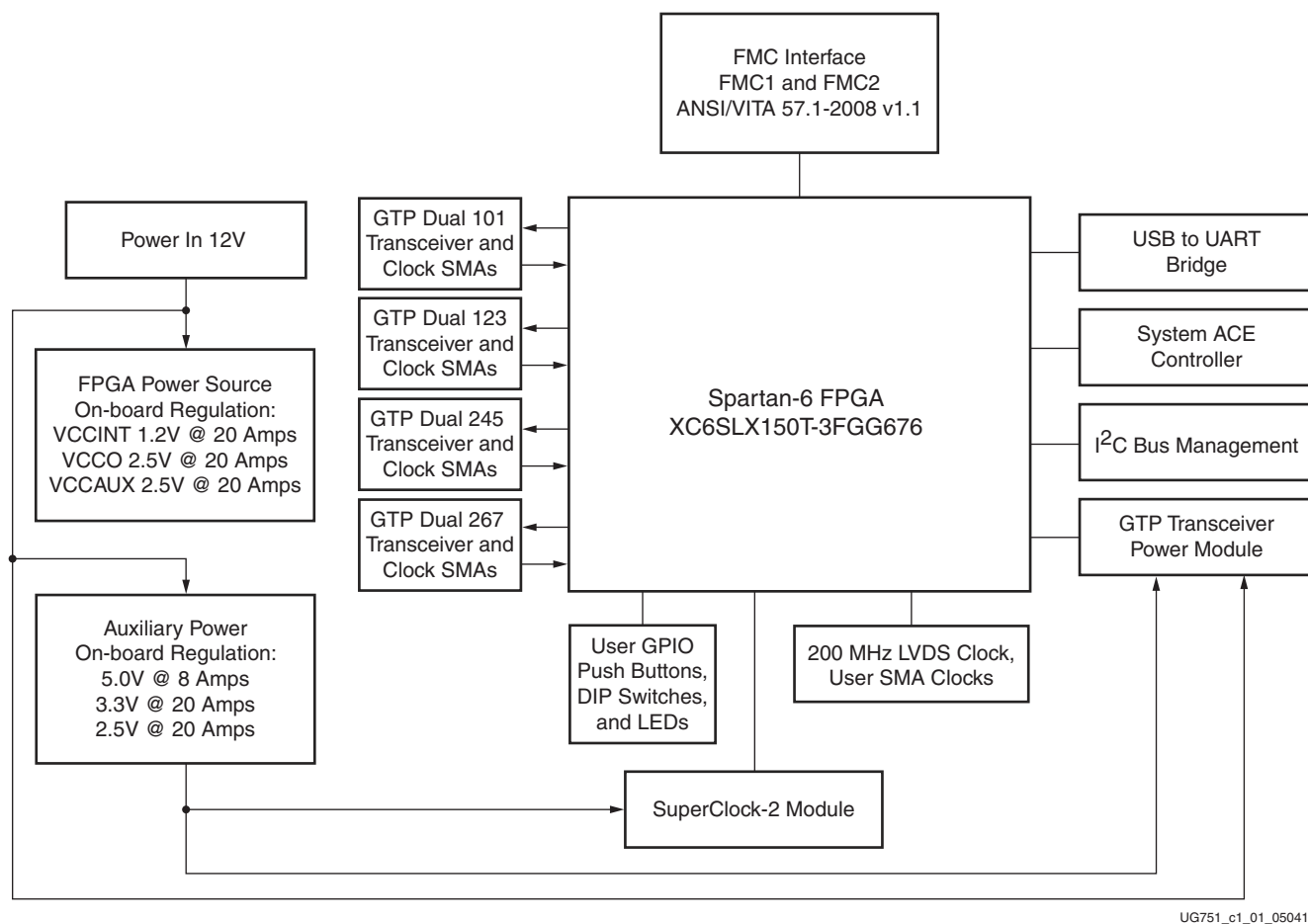
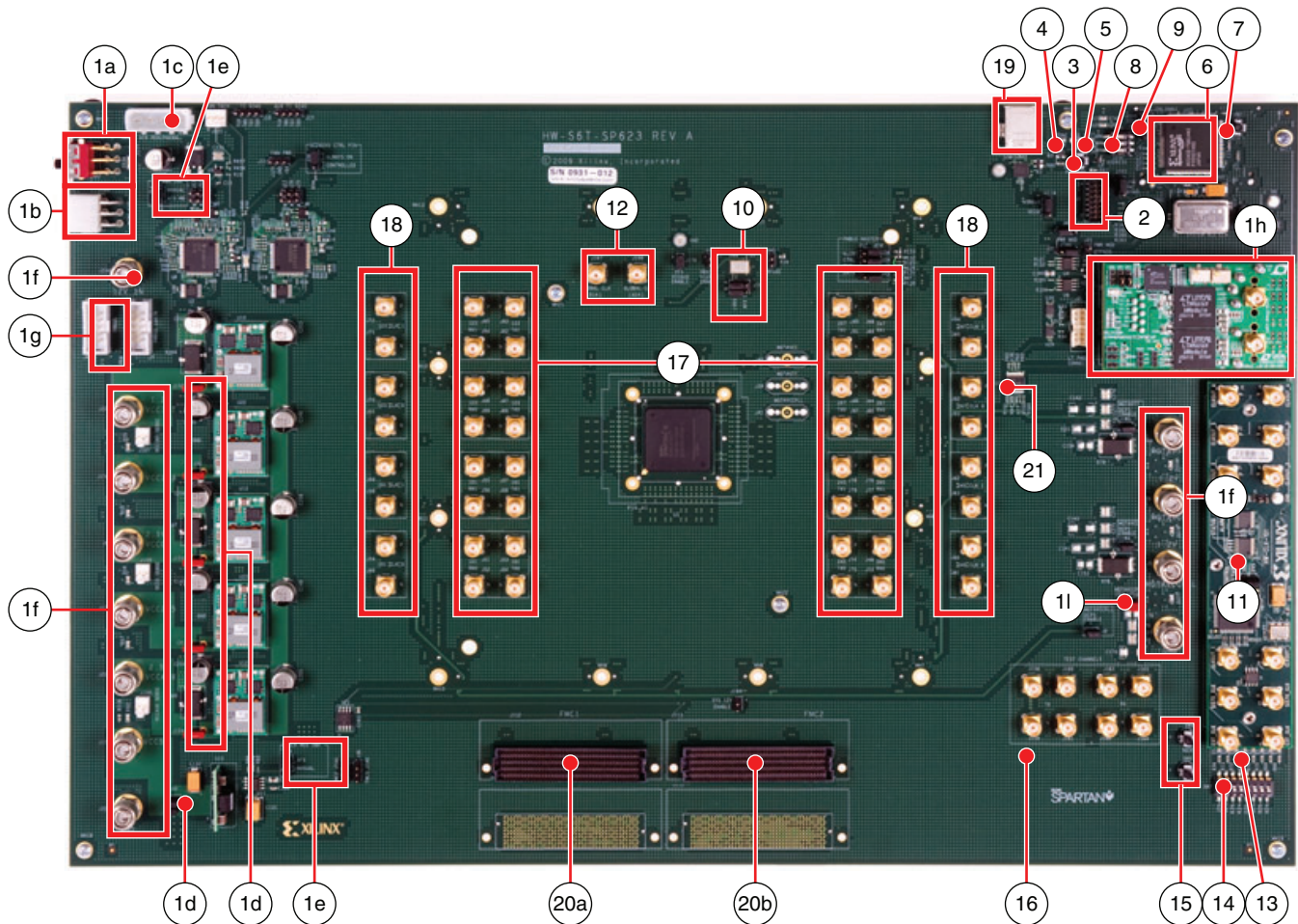


Figure 1-1: SP623 Board Block Diagram

## Detailed Description

Figure 1-2 shows the SP623 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

**Note:** The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.



- |                                                               |                                                 |
|---------------------------------------------------------------|-------------------------------------------------|
| 1a Main power switch (SW1)                                    | 8 Configuration address DIP switch (SW3)        |
| 1b 12V mini-fit connector (J122)                              | 9 JTAG isolation jumpers (J22, J23, J195, J196) |
| 1c 12V ATX connector (J141)                                   | 10 200 MHz 2.5V LVDS oscillator (U7)            |
| 1d Power regulation jumpers (J30, J31, J33, J102, J104, J105) | 11 SuperClock-2 module                          |
| 1e Regulation inhibit (J14, J19)                              | 12 User SMA global clock inputs (J167, J168)    |
| 1f External power supply jacks                                | 13 User LEDs, active-High (DS10 - DS17)         |
| 1g TI PMBus connector (J6)                                    | 14 User DIP switches, active-High (SW1 - SW8)   |
| 1h GTP transceiver power supply module                        | 15 User push buttons, active-High (SW4, SW6)    |
| 1i MGTAVCCPLL isolation jumper (J3)                           | 16 User test I/O (J44)                          |
| 2 FPGA configuration connector (J1)                           | 17 GTP transceiver pins                         |
| 3 PROG push button, active-Low (SW5)                          | 18 GTP transceiver clock input SMAs             |
| 4 DONE LED (DS6)                                              | 19 USB to UART bridge (U26)                     |
| 5 INIT LED (DS20)                                             | 20a FMC1 (J112)                                 |
| 6 System ACE controller (U25)                                 | 20b FMC2 (J113)                                 |
| 7 System ACE reset, active-Low (SW2)                          | 21 I2C bus management (U14)                     |

UG751\_c1\_02\_041310

Figure 1-2: Detailed Description of SP623 Board Components

## Power Management

Numbers 1a through 1i refer to the callouts in [Figure 1-2](#):

1a: Main power switch (SW1)

1b: 12V mini-fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J31, J33, J102, J104, J105)

1e: Regulation inhibit (J14, J19)

1f: External power supply jacks (J5, J98, J173, J174, J175, J177, J178, J189, J220, J223, J227, J234)

1g: TI PMBus cable connector (J6)

1h: GTP power supply module

1i: MGTAVCCPLL isolation jumper (J3)

## Board Power and Switch

The SP623 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 × 3) right angle Mini-Fit type connector.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

**Caution!** Do NOT plug a PC ATX power supply 6-pin connector into J122 on the SP623 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the SP623 board and void the board warranty.

**Caution!** Do NOT apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the SP623 board.

The SP623 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

## Onboard Power Regulation

Figure 1-3 shows the on-board power supply architecture.

**Note:** Power regulation jumpers are not shown in Figure 1-3.

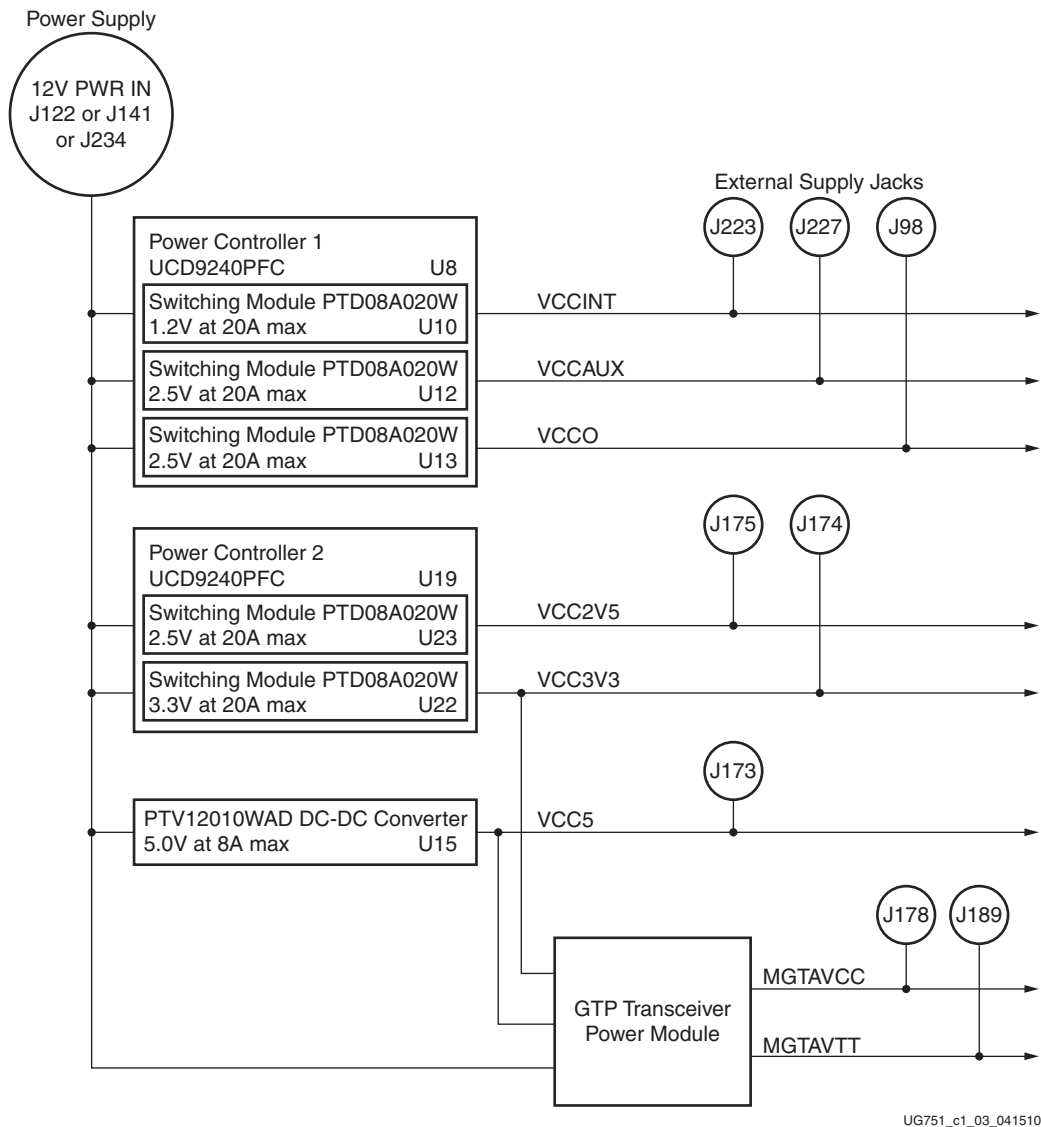


Figure 1-3: SP623 Board Power Supply Block Diagram

The SP623 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See [Using External Power Sources](#).

Table 1-1: Onboard Power System Devices

| Device                                             | Reference Designator | Description                                                  | Power Rail Net Name | Typical Voltage | Power Regulation Jumper | External Supply Jack |
|----------------------------------------------------|----------------------|--------------------------------------------------------------|---------------------|-----------------|-------------------------|----------------------|
| <b>Core voltage controller and regulators</b>      |                      |                                                              |                     |                 |                         |                      |
| UCD9240PFC                                         | U8                   | PMBus compliant digital PWM system controller (address = 52) |                     |                 |                         |                      |
| PTD08A020W                                         | U10                  | Adjustable switching regulator 20A, 0.6V to 3.6V             | VCCINT              | 1.2V            | J102                    | J223                 |
| PTD08A020W                                         | U12                  | Adjustable switching regulator 20A, 0.6V to 3.6V             | VCCAUX              | 2.5V            | J104                    | J227                 |
| PTD08A020W                                         | U13                  | Adjustable switching regulator 20A, 0.6V to 3.6V             | VCCO                | 2.5V            | J105                    | J98                  |
| <b>Auxiliary voltage controller and regulators</b> |                      |                                                              |                     |                 |                         |                      |
| UCD9240PFC                                         | U19                  | PMBus compliant digital PWM system controller (address = 53) |                     |                 |                         |                      |
| PTD08A020W                                         | U23                  | Adjustable switching regulator 20A, 0.6V to 3.6V             | VCC2V5              | 2.5V            | J31                     | J175                 |
| PTD08A020W                                         | U22                  | Adjustable switching regulator 20A, 0.6V to 3.6V             | VCC3V3              | 3.3V            | J30                     | J174                 |
| <b>5V auxiliary power</b>                          |                      |                                                              |                     |                 |                         |                      |
| PTV12010WAD                                        | U15                  | Adjustable switching regulator 8A, 1.2V to 5.5V              | VCC5                | 5.0V            | J33                     | J173                 |

### Using External Power Sources

The maximum output current rating for each power regulator is listed in [Table 1-1](#). If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in [Table 1-1](#).

**Caution!** The power regulation jumper must be removed before applying external power to the power rail through its corresponding supply jack.

### Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, and U23 are disabled by installing a jumper across pins 2–3 of header J14. Voltage regulator U15 is disabled by installing a jumper across pins 2–3 of header J19.

### Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in [Appendix A, Default Jumper Positions](#).

## Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). Both onboard TI power controllers are wired to the same PMBus. The PMBus connector, J6, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

## References

More information about the power system components used by the SP623 board are available from the Texas Instruments digital power website at:

<http://www.ti.com/ww/en/analog/digital-power/index.html>

## GTP Transceiver Power Module

The GTP transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTP transceivers. Three power modules are provided with the SP623 board. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-4.

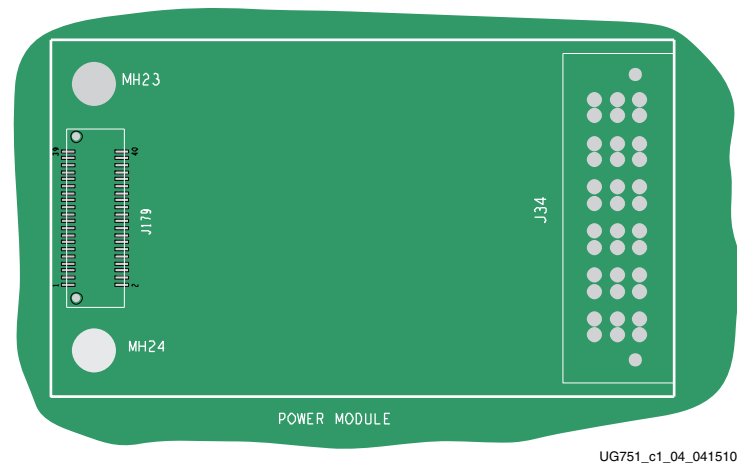


Figure 1-4: Mounting Location, GTP Transceiver Power Module

Table 1-2 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by either module included with the SP623 board.

Table 1-2: GTP Transceiver Power Module

| Power Supply Rail Net Name | Typical Voltage | Maximum Current Rating   |                          |                 | Regulation Jumper        |                          |                 | External Supply Jack |
|----------------------------|-----------------|--------------------------|--------------------------|-----------------|--------------------------|--------------------------|-----------------|----------------------|
|                            |                 | Linear Technology Module | Texas Instruments Module | Intersil Module | Linear Technology Module | Texas Instruments Module | Intersil Module |                      |
| MGTAVCC                    | 1.2V            | 16A                      | 8A                       | 8A              | JP1                      | N/A                      | N/A             | J178                 |
| MGTAVTT                    | 1.2V            | 12A                      | 6A                       | 6A              | JP2                      | N/A                      | N/A             | J189                 |

The GTP transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (See External Supply Jack column in Table 1-2). To supply power externally to one or both rails when the

Linear Technology Module is installed, place jumpers on JP1 and/or JP2 across pins 2–3 (OFF position).

**Note:** The power regulation jumper must be placed in the OFF position before connecting an external supply to its corresponding supply jack.

The Texas Instruments and Intersil modules do not have voltage regulation jumpers and *must* be removed from the board before providing external power to the GTP transceiver rails.

**Note:** The Intersil module features an MGTAVCC voltage adjust header, J1. Verify that a jumper is connected across J1 before powering the board with the Intersil module installed. Failure to do so may prevent your design from running properly.

### MGTAVCCPLL Rail

The GTP transceiver power module also supplies the MGTAVCCPLL rail through the J3 shorting plug (Figure 1-5). This jumper connects MGTAVCC and MGTAVCCPLL rails by default. The MGTAVCCPLL rail can also be supplied from an external 1.2V (nominal) power supply by removing the J3 shorting plug and then connecting the power supply output to J5.

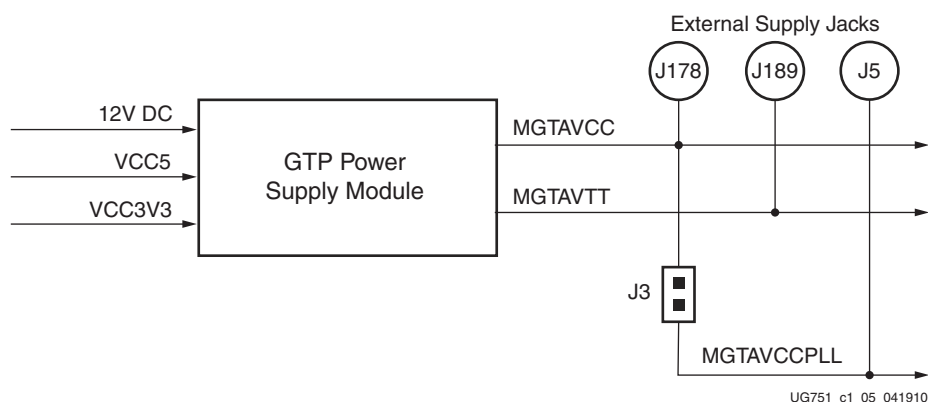


Figure 1-5: MGTAVCCPLL Isolation Jumper

## FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

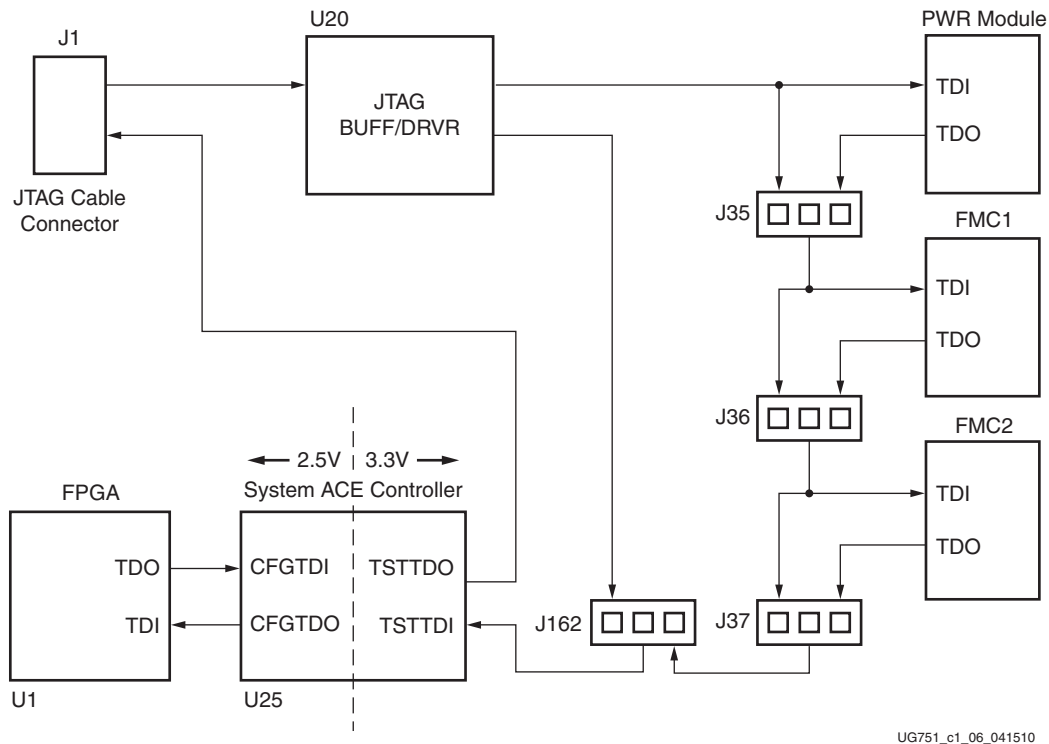
Detailed information on the System ACE controller is available in [DS080, System ACE CompactFlash Solution](#).

The FPGA is configured through one of the aforementioned cables by connecting the cable to the download cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see [Configuration Address DIP Switches, page 16](#)).

**Note:** The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, causing no disruption in the JTAG chain.

The JTAG chain of the board is illustrated in [Figure 1-6](#) (the four System ACE interface isolation jumpers described in [JTAG Isolation Jumpers](#) are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules and the GTP transceiver power supply module in the chain.



*Figure 1-6: JTAG Chain*

## PROG Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the status of the DONE pin of the FPGA. When the DONE pin is high, DS6 lights indicating the FPGA is successfully configured.

## INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

## System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back-side of the board.

## System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

## Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are identified in Table 1-3.

Table 1-3: SW3 DIP Switch Configuration

| Address | ADR2             | ADR1 | ADR0             |
|---------|------------------|------|------------------|
| 0       | O <sup>(1)</sup> | O    | O                |
| 1       | O                | O    | C <sup>(2)</sup> |
| 2       | O                | C    | O                |
| 3       | O                | C    | C                |
| 4       | C                | O    | O                |
| 5       | C                | O    | C                |
| 6       | C                | C    | O                |
| 7       | C                | C    | C                |

**Notes:**

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

## JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-7 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-7 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-6.

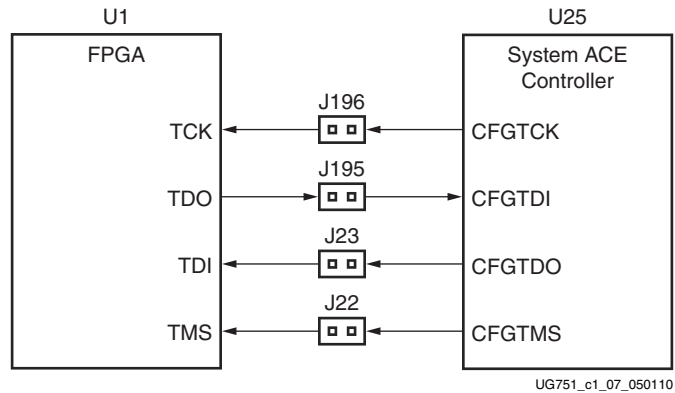


Figure 1-7: JTAG Isolation Jumpers

Table 1-4 indicates the FPGA pin name associated with each jumper.

Table 1-4: JTAG Isolation Jumpers

| Reference Designator | FPGA Pin Name |
|----------------------|---------------|
| J22                  | TMS           |
| J23                  | TDI           |
| J195                 | TDO           |
| J196                 | TCK           |

## 200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The SP623 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-5 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

Table 1-5: LVDS Oscillator Global Clock Connections

| FPGA Pin | Net Name      | U7 Pin |
|----------|---------------|--------|
| V23      | IO_LVDS_CLK_P | 4      |
| W24      | IO_LVDS_CLK_N | 5      |

## SuperClock-2 Module

[Figure 1-2, callout 11]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise clock source for the SP623 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-6 shows the FPGA I/O mapping for the SuperClock-2 module interface. The SP623 board also supplies VCC5, VCC3V3, VCC2V5, and VCCO input power to the clock module interface.

Table 1-6: SuperClock-2 FPGA I/O Mapping

| FPGA Pin | Net Name   | J32 Pin |
|----------|------------|---------|
| F12      | CM_LVDS1_P | 1       |
| E12      | CM_LVDS1_N | 3       |
| V12      | CM_LVDS2_P | 9       |
| W12      | CM_LVDS2_N | 11      |
| G12      | CM_LVDS3_P | 17      |
| F11      | CM_LVDS3_N | 19      |
| U25      | CM_GCLK_P  | 25      |
| U26      | CM_GCLK_N  | 27      |
| U20      | CM_CTRL_0  | 61      |
| U19      | CM_CTRL_1  | 63      |
| AA24     | CM_CTRL_2  | 65      |
| AA23     | CM_CTRL_3  | 67      |
| T20      | CM_CTRL_4  | 69      |
| T19      | CM_CTRL_5  | 71      |
| U22      | CM_CTRL_6  | 73      |
| U21      | CM_CTRL_7  | 75      |
| AE26     | CM_CTRL_8  | 77      |
| AE25     | CM_CTRL_9  | 79      |
| Y26      | CM_CTRL_10 | 81      |
| Y24      | CM_CTRL_11 | 83      |
| AC26     | CM_CTRL_12 | 85      |
| AC25     | CM_CTRL_13 | 87      |
| AB26     | CM_CTRL_14 | 89      |
| AB24     | CM_CTRL_15 | 91      |
| AD26     | CM_CTRL_16 | 93      |
| AD24     | CM_CTRL_17 | 95      |
| AA26     | CM_CTRL_18 | 97      |
| AA25     | CM_CTRL_19 | 99      |
| W26      | CM_CTRL_20 | 101     |
| W25      | CM_CTRL_21 | 103     |
| V24      | CM_CTRL_22 | 105     |
| T23      | CM_CTRL_23 | 107     |
| T22      | CM_RST     | 66      |

## User SMA Global Clock Inputs

[Figure 1-2, callout 12]

The SP623 board provides two single-ended clock input SMAs that can be used for connecting to an external function generator. These clock inputs can alternatively be used as a differential pair. The FPGA clock pins are connected to the SMAs as shown in Table 1-7.

**Note:** Jumpers should NOT be installed on AFX SEL headers J99 and J100 if these clock inputs are used.

Table 1-7: SMA Clock Input Connections

| FPGA Pin | Net Name  | SMA Connector |
|----------|-----------|---------------|
| R25      | SMA_CLK_P | J167          |
| R26      | SMA_CLK_N | J168          |

## User LEDs (Active High)

[Figure 1-2, callout 13]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O on the FPGA as shown in Table 1-8. These LEDs can be used to indicate status, or any other purpose determined by the user.

Table 1-8: User LEDs

| FPGA Pin | Net Name | Reference Designator |
|----------|----------|----------------------|
| L21      | LED1     | DS17                 |
| L20      | LED2     | DS16                 |
| M23      | LED3     | DS15                 |
| M21      | LED4     | DS14                 |
| N26      | LED5     | DS13                 |
| N25      | LED6     | DS12                 |
| L26      | LED7     | DS11                 |
| L25      | LED8     | DS10                 |

## User DIP Switches (Active High)

[Figure 1-2, callout 14]

DIP switch SW7 provides a set of eight active-High switches that connect to user I/O on the FPGA, as shown in Table 1-9. These pins can be used to set control pins, or other functions determined by the user.

Table 1-9: User DIP Switches

| FPGA Pin | Net Name | Reference Designator |
|----------|----------|----------------------|
| J26      | SW1      | SW7                  |
| J25      | SW2      |                      |
| K26      | SW3      |                      |
| K24      | SW4      |                      |
| G26      | SW5      |                      |
| G25      | SW6      |                      |
| H26      | SW7      |                      |
| H24      | SW8      |                      |

## User Push Buttons (Active High)

[Figure 1-2, callout 15]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA, as identified in Table 1-10. These switches can be used for any purpose determined by the user.

Table 1-10: User Push Buttons

| FPGA Pin | Net Name | Reference Designator |
|----------|----------|----------------------|
| M26      | PB_SW1   | SW6                  |
| M24      | PB_SW2   | SW4                  |

## User Test I/O

[Figure 1-2, callout 16]

A standard 2 x 6, 100-mil pitch header (J44) brings out 6 FPGA I/O for test purposes. Table 1-11 lists these pins.

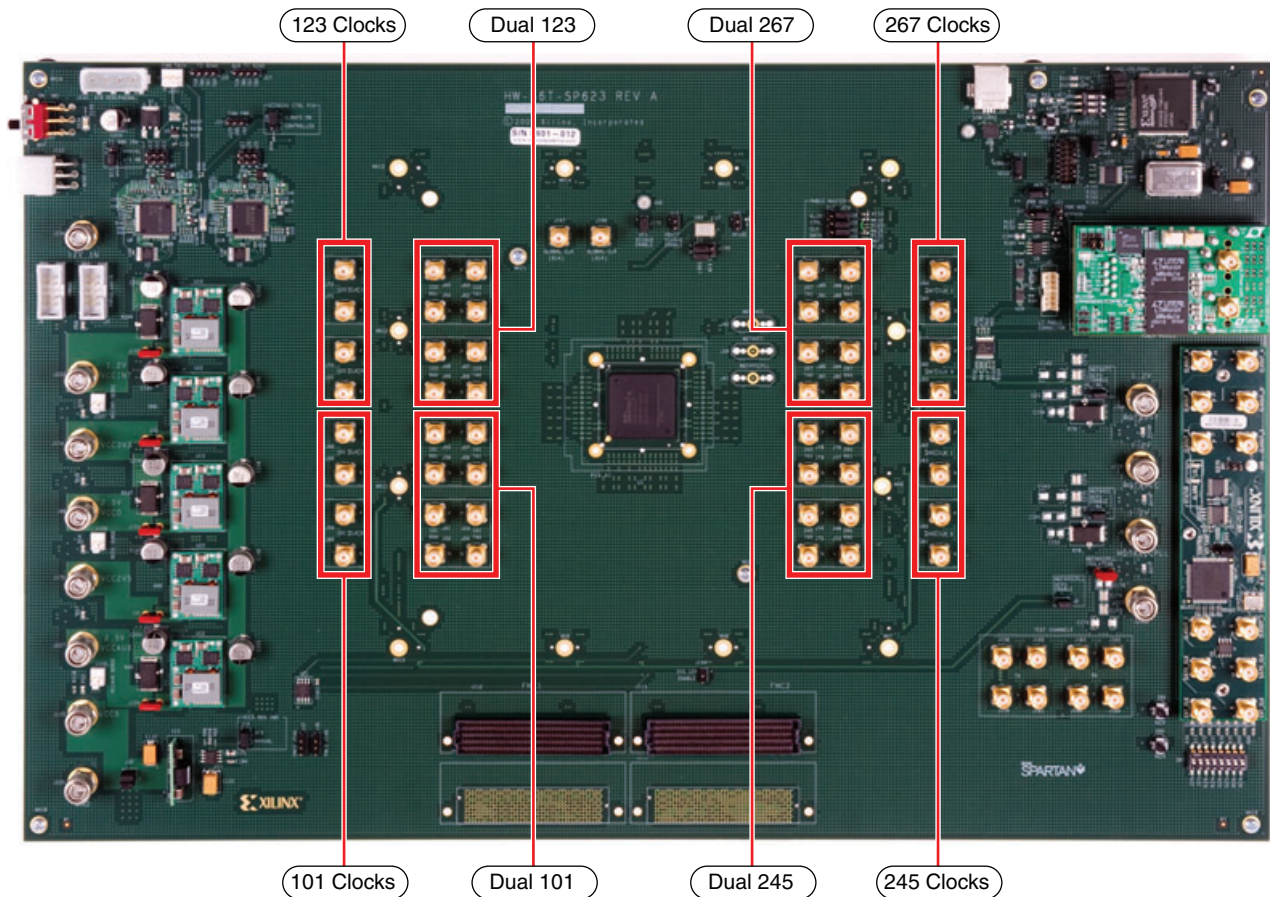
Table 1-11: User Test I/O

| FPGA Pin | Net Name             | J44 Pin |
|----------|----------------------|---------|
| U1       | IO_L40N_M3DQ7_3_U1   | 2       |
| U2       | IO_L40P_M3DQ6_3_U2   | 4       |
| V1       | IO_L39N_M3LDQSN_3_V1 | 6       |
| V3       | IO_L39P_M3LDQS_3_V3  | 8       |
| AA13     | IO_L36N_2_AA13       | 10      |
| AB13     | IO_L36P_2_AB13       | 12      |

## GTP Transceiver Pins

[Figure 1-2, callout 17]

All FPGA GTP transceiver pins are connected to differential SMA connector pairs. The GTP transceivers are grouped into four sets of two (referred to as *Duals*) which share two differential reference clock pin-pairs (Figure 1-8). The transceiver pins and their corresponding SMA connector are identified in Table 1-12.



UG751\_c1\_07\_052210

Figure 1-8: GTP Transceiver and Reference Clock SMA Locations

Table 1-12: GTP Transceiver Pins

| FPGA Pin | Net Name  | SMA Connector | Trace Length (Mils) |
|----------|-----------|---------------|---------------------|
| D7       | 101_RX0_P | J51           | 4,253               |
| C7       | 101_RX0_N | J52           | 4,253               |
| B6       | 101_TX0_P | J53           | 3,634               |
| A6       | 101_TX0_N | J54           | 3,633               |
| D9       | 101_RX1_P | J55           | 3,861               |
| C9       | 101_RX1_N | J56           | 3,861               |

Table 1-12: GTP Transceiver Pins (Cont'd)

| FGPA Pin | Net Name  | SMA Connector | Trace Length (Mils) |
|----------|-----------|---------------|---------------------|
| B8       | 101_TX1_P | J57           | 2,503               |
| A8       | 101_TX1_N | J58           | 2,502               |
| D17      | 123_RX0_P | J68           | 3,531               |
| C17      | 123_RX0_N | J69           | 3,531               |
| B18      | 123_TX0_P | J67           | 3,340               |
| A18      | 123_TX0_N | J66           | 3,340               |
| D19      | 123_RX1_P | J65           | 3,665               |
| C19      | 123_RX1_N | J64           | 3,664               |
| B20      | 123_TX1_P | J63           | 2,939               |
| A20      | 123_TX1_N | J62           | 2,941               |
| AC8      | 245_RX0_P | J48           | 4,316               |
| AD8      | 245_RX0_N | J73           | 4,315               |
| AE7      | 245_TX0_P | J74           | 3,616               |
| AF7      | 245_TX0_N | J75           | 3,615               |
| AC10     | 245_RX1_P | J76           | 3,865               |
| AD10     | 245_RX1_N | J77           | 3,865               |
| AE9      | 245_TX1_P | J78           | 2,563               |
| AF9      | 245_TX1_N | J79           | 2,562               |
| AC18     | 267_RX0_P | J84           | 3,328               |
| AD18     | 267_RX0_N | J85           | 3,327               |
| AE19     | 267_TX0_P | J86           | 3,719               |
| AF19     | 267_TX0_N | J87           | 3,718               |
| AC20     | 267_RX1_P | J88           | 3,952               |
| AD20     | 267_RX1_N | J89           | 3,952               |
| AE21     | 267_TX1_P | J90           | 3,238               |
| AF21     | 267_TX1_N | J91           | 3,239               |

## GTP Transceiver Clock Input SMAs

[Figure 1-2, callout 18]

The SP623 board provides differential SMA connectors that can be used for connecting an external function generator to all GTP transceiver reference clock inputs of the FPGA. The FPGA reference clock pins are connected to the SMA connectors as shown in Table 1-13.

**Table 1-13: GTP Transceiver Clock Inputs to the FPGA**

| FPGA Pin | Net Name      | SMA Connector |
|----------|---------------|---------------|
| B10      | 101_REFCLK0_P | J59           |
| A10      | 101_REFCLK0_N | J60           |
| D11      | 101_REFCLK1_P | J49           |
| C11      | 101_REFCLK1_N | J50           |
| D15      | 123_REFCLK0_P | J70           |
| C15      | 123_REFCLK0_N | J61           |
| B16      | 123_REFCLK1_P | J72           |
| A16      | 123_REFCLK1_N | J71           |
| AE11     | 245_REFCLK0_P | J80           |
| AF11     | 245_REFCLK0_N | J81           |
| AC12     | 245_REFCLK1_P | J82           |
| AD12     | 245_REFCLK1_N | J83           |
| AC16     | 267_REFCLK0_P | J92           |
| AD16     | 267_REFCLK0_N | J93           |
| AE17     | 267_REFCLK1_P | J94           |
| AF17     | 267_REFCLK1_N | J95           |

## USB to UART Bridge

[Figure 1-2, callout 19]

Communications between the SP623 board and a host computer are through a USB Mini-B cable connected to J9. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-14 lists the pin assignments and signals for the USB connector J9.

**Table 1-14: USB Mini-B Connector Pin Assignments and Signals**

| J9 Pin | Signal Name | Description                                     |
|--------|-------------|-------------------------------------------------|
| 1      | VBUS        | +5V from host system (not used)                 |
| 2      | USB_DATA_N  | Bidirectional differential serial data (N-side) |
| 3      | USB_DATA_P  | Bidirectional differential serial data (P-side) |
| 4      | GROUND      | Signal ground                                   |

The CP2103 supports an IO voltage range of 1.8V to 2.5V on the SP623 board. The connections between the FPGA and CP2103 should use the LVCMOS25 IO standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA fabric. The FPGA supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS).

Connections of these signals between the FPGA and the CP2103 at U26 are listed in [Table 1-15](#).

**Table 1-15: FPGA to U26 (CP2103 USB to UART Bridge) Connections**

| FPGA Pin | FPGA Function | Net Name | U26 Pin | U26 Function  |
|----------|---------------|----------|---------|---------------|
| L23      | RTS, output   | USB_CTS  | 22      | CTS, input    |
| L23      | CTS, input    | USB_RTS  | 23      | RTS, output   |
| N20      | TX, data out  | USB_RX   | 24      | RXD, data in  |
| N19      | RX, data in   | USB_TX   | 25      | TXD, data out |

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information ([Table 1-16](#)).

**Table 1-16: CP2103 USB to UART Bridge User GPIO**

| FPGA Pin | Net Name  | U26 Pin |
|----------|-----------|---------|
| P22      | USB_GPIO0 | 19      |
| P21      | USB_GPIO1 | 18      |
| N22      | USB_GPIO2 | 17      |
| N21      | USB_GPIO3 | 16      |

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the SP623 board.

## FMC HPC Connectors

[[Figure 1-2](#), callouts [20a](#), and [20b](#)]

The SP623 board features two high pin count (HPC) connectors as defined by the VITA 57.1.1 FMC specification. Each FMC HPC connector is a 10 x 40 position socket that is fully populated with 400 pins. See [Appendix B, VITA 57.1 FMC HPC Connector Pinout](#) for a cross-reference of signal names to pin coordinates.

The FMC1 HPC connector at J112 on the SP623 board provides connectivity for:

- 58 differential user-defined pairs:
  - 34 LA pairs
  - 24 HA pairs

- 3 differential clocks

The FMC2 HPC connector at J113 on the SP623 board provides connectivity for:

- 57 differential user-defined pairs:
  - 34 LA pairs
  - 23 HA pairs
- 2 differential clocks

**Note:** The  $V_{ADJ}$  voltage for the FMC HPC connectors on the SP623 board is fixed at 2.5V (non-adjustable). The 2.5V rail cannot be turned off. The VITA 57.1 FMC interfaces on the SP623 board are compatible with 2.5V mezzanine cards capable of supporting 2.5V  $V_{ADJ}$ .

The connections for the FMC1 and FMC2 connectors are identified in [Table 1-17](#) and [Table 1-18](#), respectively.

**Table 1-17: Vita 57.1 FMC1 HPC Connections at J112**

| FPGA Pin | Net Name        | FMC Pin |
|----------|-----------------|---------|
| T3       | FMC1_CLK0_M2C_P | H4      |
| T1       | FMC1_CLK0_M2C_N | H5      |
| B14      | FMC1_CLK1_M2C_P | G2      |
| A14      | FMC1_CLK1_M2C_N | G3      |
| V4       | FMC1_CLK2_M2C_P | K4      |
| W3       | FMC1_CLK2_M2C_N | K5      |
| R2       | FMC1_HA00_CC_P  | F4      |
| R1       | FMC1_HA00_CC_N  | F5      |
| M4       | FMC1_HA01_CC_P  | E2      |
| N3       | FMC1_HA01_CC_N  | E3      |
| N2       | FMC1_HA02_P     | K7      |
| N1       | FMC1_HA02_N     | K8      |
| M3       | FMC1_HA03_P     | J6      |
| M1       | FMC1_HA03_N     | J7      |
| L2       | FMC1_HA04_P     | F7      |
| L1       | FMC1_HA04_N     | F8      |
| K3       | FMC1_HA05_P     | E6      |
| K1       | FMC1_HA05_N     | E7      |
| J2       | FMC1_HA06_P     | K10     |
| J1       | FMC1_HA06_N     | K11     |
| H3       | FMC1_HA07_P     | J9      |
| H1       | FMC1_HA07_N     | J10     |
| G2       | FMC1_HA08_P     | F10     |
| G1       | FMC1_HA08_N     | F11     |

Table 1-17: Vita 57.1 FMC1 HPC Connections at J112 (Cont'd)

| FPGA Pin | Net Name                    | FMC Pin |
|----------|-----------------------------|---------|
| F3       | FMC1_HA09_P                 | E9      |
| F1       | FMC1_HA09_N                 | E10     |
| E2       | FMC1_HA10_P                 | K13     |
| E1       | FMC1_HA10_N                 | K14     |
| D3       | FMC1_HA11_P                 | J12     |
| D1       | FMC1_HA11_N                 | J13     |
| J4       | FMC1_HA12_P                 | F13     |
| J3       | FMC1_HA12_N                 | F14     |
| L9       | FMC1_HA13_P                 | E12     |
| L8       | FMC1_HA13_N                 | E13     |
| L4       | FMC1_HA14_P                 | J15     |
| L3       | FMC1_HA14_N                 | J16     |
| M8       | FMC1_HA15_P                 | F16     |
| M6       | FMC1_HA15_N                 | F17     |
| K5       | FMC1_HA16_P                 | E15     |
| J5       | FMC1_HA16_N                 | E16     |
| L7       | FMC1_HA17_CC_P              | K16     |
| L6       | FMC1_HA17_CC_N              | K17     |
| B2       | FMC1_HA18_P                 | J18     |
| B1       | FMC1_HA18_N                 | J19     |
| L10      | FMC1_HA19_P                 | F19     |
| K10      | FMC1_HA19_N                 | F20     |
| G4       | FMC1_HA20_P                 | E18     |
| G3       | FMC1_HA20_N                 | E19     |
| J9       | FMC1_HA21_P                 | K19     |
| J7       | FMC1_HA21_N                 | K20     |
| C2       | FMC1_HA22_P                 | J21     |
| C1       | FMC1_HA22_N                 | J22     |
| K9       | FMC1_HA23_P                 | K22     |
| K8       | FMC1_HA23_N                 | K23     |
| U14.13   | FMC1_I2C_SCL <sup>(1)</sup> | C30     |
| U14.12   | FMC1_I2C_SDA <sup>(1)</sup> | C31     |
| E13      | FMC1_LA00_CC_P              | G6      |

Table 1-17: Vita 57.1 FMC1 HPC Connections at J112 (Cont'd)

| FPGA Pin | Net Name       | FMC Pin |
|----------|----------------|---------|
| D13      | FMC1_LA00_CC_N | G7      |
| C13      | FMC1_LA01_CC_P | D8      |
| A13      | FMC1_LA01_CC_N | D9      |
| H9       | FMC1_LA02_P    | H7      |
| G9       | FMC1_LA02_N    | H8      |
| A3       | FMC1_LA03_P    | G9      |
| A2       | FMC1_LA03_N    | G10     |
| F9       | FMC1_LA04_P    | H10     |
| E8       | FMC1_LA04_N    | H11     |
| D5       | FMC1_LA05_P    | D11     |
| C5       | FMC1_LA05_N    | D12     |
| H7       | FMC1_LA06_P    | C10     |
| G7       | FMC1_LA06_N    | C11     |
| H10      | FMC1_LA07_P    | H13     |
| G10      | FMC1_LA07_N    | H14     |
| B4       | FMC1_LA08_P    | G12     |
| A4       | FMC1_LA08_N    | G13     |
| F10      | FMC1_LA09_P    | D14     |
| E10      | FMC1_LA09_N    | D15     |
| B5       | FMC1_LA10_P    | C14     |
| A5       | FMC1_LA10_N    | C15     |
| H8       | FMC1_LA11_P    | H16     |
| G8       | FMC1_LA11_N    | H17     |
| J11      | FMC1_LA12_P    | G15     |
| G11      | FMC1_LA12_N    | G16     |
| H12      | FMC1_LA13_P    | D17     |
| G13      | FMC1_LA13_N    | D18     |
| K12      | FMC1_LA14_P    | C18     |
| J12      | FMC1_LA14_N    | C19     |
| F7       | FMC1_LA15_P    | H19     |
| F6       | FMC1_LA15_N    | H20     |
| J15      | FMC1_LA16_P    | G18     |
| H15      | FMC1_LA16_N    | G19     |

Table 1-17: Vita 57.1 FMC1 HPC Connections at J112 (Cont'd)

| FPGA Pin | Net Name       | FMC Pin |
|----------|----------------|---------|
| B12      | FMC1_LA17_CC_P | D20     |
| A12      | FMC1_LA17_CC_N | D21     |
| J16      | FMC1_LA18_CC_P | C22     |
| J17      | FMC1_LA18_CC_N | C23     |
| F16      | FMC1_LA19_P    | H22     |
| E16      | FMC1_LA19_N    | H23     |
| C3       | FMC1_LA20_P    | G21     |
| B3       | FMC1_LA20_N    | G22     |
| G15      | FMC1_LA21_P    | H25     |
| F15      | FMC1_LA21_N    | H26     |
| F18      | FMC1_LA22_P    | G24     |
| E18      | FMC1_LA22_N    | G25     |
| G16      | FMC1_LA23_P    | D23     |
| F17      | FMC1_LA23_N    | D24     |
| F20      | FMC1_LA24_P    | H28     |
| E20      | FMC1_LA24_N    | H29     |
| H17      | FMC1_LA25_P    | G27     |
| G17      | FMC1_LA25_N    | G28     |
| C21      | FMC1_LA26_P    | D26     |
| B21      | FMC1_LA26_N    | D27     |
| G6       | FMC1_LA27_P    | C26     |
| F5       | FMC1_LA27_N    | C27     |
| H18      | FMC1_LA28_P    | H31     |
| H19      | FMC1_LA28_N    | H32     |
| B22      | FMC1_LA29_P    | G30     |
| A22      | FMC1_LA29_N    | G31     |
| G19      | FMC1_LA30_P    | H34     |
| F19      | FMC1_LA30_N    | H35     |
| B23      | FMC1_LA31_P    | G33     |
| A23      | FMC1_LA31_N    | G34     |
| D21      | FMC1_LA32_P    | H37     |
| D22      | FMC1_LA32_N    | H38     |
| E6       | FMC1_LA33_P    | G36     |

Table 1-17: Vita 57.1 FMC1 HPC Connections at J112 (Cont'd)

| FPGA Pin                                                                                                                                                                                            | Net Name                    | FMC Pin |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------|
| E5                                                                                                                                                                                                  | FMC1_LA33_N                 | G37     |
| E3                                                                                                                                                                                                  | FMC1_PRSENT_M2C             | H2      |
| U20.13                                                                                                                                                                                              | FMC1_TCK_BUF <sup>(1)</sup> | D29     |
| J36.1                                                                                                                                                                                               | FMC1_TDI <sup>(1)</sup>     | D30     |
| J36.3                                                                                                                                                                                               | FMC1_TDO <sup>(1)</sup>     | D31     |
| U20.16                                                                                                                                                                                              | TMS_BUF <sup>(1)</sup>      | D33     |
| <b>Notes:</b><br>1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U14.13 = U14 pin 13. |                             |         |

Table 1-18: Vita 57.1 FMC2 HPC Connections at J113

| FPGA Pin | Net Name        | FMC Pin |
|----------|-----------------|---------|
| U23      | FMC2_CLK0_M2C_P | H4      |
| U24      | FMC2_CLK0_M2C_N | H5      |
| AD14     | FMC2_CLK1_M2C_P | G2      |
| AF14     | FMC2_CLK1_M2C_N | G3      |
| R7       | FMC2_HA00_CC_P  | F4      |
| R6       | FMC2_HA00_CC_N  | F5      |
| U4       | FMC2_HA02_P     | K7      |
| U3       | FMC2_HA02_N     | K8      |
| V5       | FMC2_HA03_P     | J6      |
| W5       | FMC2_HA03_N     | J7      |
| U9       | FMC2_HA04_P     | F7      |
| U8       | FMC2_HA04_N     | F8      |
| U7       | FMC2_HA05_P     | E6      |
| T6       | FMC2_HA05_N     | E7      |
| AB3      | FMC2_HA06_P     | K10     |
| AB1      | FMC2_HA06_N     | K11     |
| AD3      | FMC2_HA07_P     | J9      |
| AD1      | FMC2_HA07_N     | J10     |
| AC2      | FMC2_HA08_P     | F10     |
| AC1      | FMC2_HA08_N     | F11     |
| AE2      | FMC2_HA09_P     | E9      |

Table 1-18: Vita 57.1 FMC2 HPC Connections at J113 (Cont'd)

| FPGA Pin | Net Name                    | FMC Pin |
|----------|-----------------------------|---------|
| AE1      | FMC2_HA09_N                 | E10     |
| AA2      | FMC2_HA10_P                 | K13     |
| AA1      | FMC2_HA10_N                 | K14     |
| Y3       | FMC2_HA11_P                 | J12     |
| Y1       | FMC2_HA11_N                 | J13     |
| W2       | FMC2_HA12_P                 | F13     |
| W1       | FMC2_HA12_N                 | F14     |
| R10      | FMC2_HA13_P                 | E12     |
| T9       | FMC2_HA13_N                 | E13     |
| P3       | FMC2_HA14_P                 | J15     |
| P1       | FMC2_HA14_N                 | J16     |
| N6       | FMC2_HA15_P                 | F16     |
| P6       | FMC2_HA15_N                 | F17     |
| P5       | FMC2_HA16_P                 | E15     |
| R5       | FMC2_HA16_N                 | E16     |
| N8       | FMC2_HA17_CC_P              | K16     |
| N7       | FMC2_HA17_CC_N              | K17     |
| R4       | FMC2_HA18_P                 | J18     |
| R3       | FMC2_HA18_N                 | J19     |
| R9       | FMC2_HA19_P                 | F19     |
| P8       | FMC2_HA19_N                 | F20     |
| N5       | FMC2_HA20_P                 | E18     |
| N4       | FMC2_HA20_N                 | E19     |
| P10      | FMC2_HA21_P                 | K19     |
| N9       | FMC2_HA21_N                 | K20     |
| M10      | FMC2_HA22_P                 | J21     |
| M9       | FMC2_HA22_N                 | J22     |
| Y6       | FMC2_HA23_P                 | K22     |
| Y5       | FMC2_HA23_N                 | K23     |
| U14.13   | FMC2_I2C_SCL <sup>(1)</sup> | C30     |
| U14.12   | FMC2_I2C_SDA <sup>(1)</sup> | C31     |
| AB14     | FMC2_LA00_CC_P              | G6      |
| AC14     | FMC2_LA00_CC_N              | G7      |

Table 1-18: Vita 57.1 FMC2 HPC Connections at J113 (Cont'd)

| FPGA Pin | Net Name       | FMC Pin |
|----------|----------------|---------|
| AE13     | FMC2_LA01_CC_P | D8      |
| AF13     | FMC2_LA01_CC_N | D9      |
| V18      | FMC2_LA02_P    | H7      |
| W19      | FMC2_LA02_N    | H8      |
| W17      | FMC2_LA03_P    | G9      |
| W18      | FMC2_LA03_N    | G10     |
| AA21     | FMC2_LA04_P    | H10     |
| AB21     | FMC2_LA04_N    | H11     |
| Y17      | FMC2_LA05_P    | D11     |
| AA17     | FMC2_LA05_N    | D12     |
| U15      | FMC2_LA06_P    | C10     |
| V16      | FMC2_LA06_N    | C11     |
| AA19     | FMC2_LA07_P    | H13     |
| AB19     | FMC2_LA07_N    | H14     |
| W16      | FMC2_LA08_P    | G12     |
| Y16      | FMC2_LA08_N    | G13     |
| AA18     | FMC2_LA09_P    | D14     |
| AB17     | FMC2_LA09_N    | D15     |
| Y15      | FMC2_LA10_P    | C14     |
| AA16     | FMC2_LA10_N    | C15     |
| V14      | FMC2_LA11_P    | H16     |
| V15      | FMC2_LA11_N    | H17     |
| U13      | FMC2_LA12_P    | G15     |
| V13      | FMC2_LA12_N    | G16     |
| AA15     | FMC2_LA13_P    | D17     |
| AB15     | FMC2_LA13_N    | D18     |
| Y21      | FMC2_LA14_P    | C18     |
| AA22     | FMC2_LA14_N    | C19     |
| Y12      | FMC2_LA15_P    | H19     |
| AA12     | FMC2_LA15_N    | H20     |
| W14      | FMC2_LA16_P    | G18     |
| Y13      | FMC2_LA16_N    | G19     |
| AE15     | FMC2_LA17_CC_P | D20     |

Table 1-18: Vita 57.1 FMC2 HPC Connections at J113 (Cont'd)

| FPGA Pin | Net Name       | FMC Pin |
|----------|----------------|---------|
| AF15     | FMC2_LA17_CC_N | D21     |
| AD23     | FMC2_LA18_CC_P | C22     |
| AF23     | FMC2_LA18_CC_N | C23     |
| Y11      | FMC2_LA19_P    | H22     |
| AA11     | FMC2_LA19_N    | H23     |
| V11      | FMC2_LA20_P    | G21     |
| V10      | FMC2_LA20_N    | G22     |
| AA9      | FMC2_LA21_P    | H25     |
| AB9      | FMC2_LA21_N    | H26     |
| AA10     | FMC2_LA22_P    | G24     |
| AB11     | FMC2_LA22_N    | G25     |
| AD6      | FMC2_LA23_P    | D23     |
| AF6      | FMC2_LA23_N    | D24     |
| W20      | FMC2_LA24_P    | H28     |
| Y20      | FMC2_LA24_N    | H29     |
| W10      | FMC2_LA25_P    | G27     |
| W9       | FMC2_LA25_N    | G28     |
| AE5      | FMC2_LA26_P    | D26     |
| AF5      | FMC2_LA26_N    | D27     |
| Y9       | FMC2_LA27_P    | C26     |
| AA8      | FMC2_LA27_N    | C27     |
| AB7      | FMC2_LA28_P    | H31     |
| AC6      | FMC2_LA28_N    | H32     |
| AB22     | FMC2_LA29_P    | G30     |
| AC22     | FMC2_LA29_N    | G31     |
| AC5      | FMC2_LA30_P    | H34     |
| AD5      | FMC2_LA30_N    | H35     |
| W8       | FMC2_LA31_P    | G33     |
| W7       | FMC2_LA31_N    | G34     |
| AD4      | FMC2_LA32_P    | H37     |
| AF4      | FMC2_LA32_N    | H38     |
| AA7      | FMC2_LA33_P    | G36     |
| AA6      | FMC2_LA33_N    | G37     |

Table 1-18: Vita 57.1 FMC2 HPC Connections at J113 (Cont'd)

| FPGA Pin                                                                                                                                                                                            | Net Name                    | FMC Pin |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------|
| AC3                                                                                                                                                                                                 | FMC2_PRSENT_M2C             | H2      |
| U20.13                                                                                                                                                                                              | FMC2_TCK_BUF <sup>(1)</sup> | D29     |
| J36.1                                                                                                                                                                                               | FMC2_TDI <sup>(1)</sup>     | D30     |
| J36.3                                                                                                                                                                                               | FMC2_TDO <sup>(1)</sup>     | D31     |
| U20.16                                                                                                                                                                                              | TMS_BUF <sup>(1)</sup>      | D33     |
| <b>Notes:</b><br>1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U14.13 = U14 pin 13. |                             |         |

Table 1-19: Power Supply Voltages for the HPC Connector

| Voltage Supply      | Allowable Voltage Range | Number of Pins | Maximum Amps | Tolerance | Maximum Capacitive Load |
|---------------------|-------------------------|----------------|--------------|-----------|-------------------------|
| V <sub>ADJ</sub>    | Fixed 2.5V              | 4              | 4            | ±5%       | 1,000 µF                |
| 3P3V <sub>AUX</sub> | 3.3V                    | 1              | 0.020        | ±5%       | 150 µF                  |
| 3P3V                | 3.3V                    | 4              | 3            | ±5%       | 1,000 µF                |
| 12P0V               | 12V                     | 2              | 1            | ±5%       | 1,000 µF                |

## I<sup>2</sup>C Bus Management

[Figure 1-2, callout 21]

The I<sup>2</sup>C bus is controlled through U14, a four-channel I<sup>2</sup>C-bus multiplexer (Texas Instruments PCA9544A). The FPGA communicates with the multiplexer through I<sup>2</sup>C data and clock signals mapped to FPGA pins J24 and J23, respectively. The I<sup>2</sup>C idcode for the PCA9544A device is 0x70. The bus hosts four components:

- GTP transceiver power supply module
- SuperClock-2 module
- FMC1
- FMC2

An I<sup>2</sup>C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-20.

Table 1-20: I<sup>2</sup>C Channel Assignments

| U27 Channel | I <sup>2</sup> C Component          |
|-------------|-------------------------------------|
| 0           | GTP transceiver power supply module |
| 1           | SuperClock-2 module                 |
| 2           | FMC1                                |
| 3           | FMC2                                |



## Default Jumper Positions

Table A-1 shows the 23 standard (black) shunts that must be installed on the board for proper operation. There are an additional six (red) shorting plugs that must be installed to enable the output of on-board, regulated power and to connect the MGTAVCCPLL and MGTAVCC rails. These shunts and shorting plugs must always be installed except where specifically noted in this user guide. Refer to PCB Assembly Drawing 0431556 for the default placement of all on-board jumpers and their respective connectors, as located on the board.

Table A-1: Standard Shunts

| Connector | Name                                   | Shunt Position         | Quantity | Pins (Jumper Label) |
|-----------|----------------------------------------|------------------------|----------|---------------------|
| J14       | TI PWR INH                             | Installed              | 1        | 1-2 (AFX MB)        |
| J38       | UCD9240 CTRL PIN                       | Installed              | 1        | 1-2 (ALWAYS ON)     |
| J33       | VCC5 REG ENABLE <sup>(1)</sup>         | Installed Horizontally | 2        | 1-2, 3-4            |
| J19       | VCC5 REG INH                           | Installed              | 1        | 1-2 (AFX)           |
| J176      | VFS VCCAUX ENABLE                      | Installed              | 1        | 1-2                 |
| J188      | SYSTEM CLOCK <sup>(1)</sup>            | Installed Horizontally | 2        | 1-3, 2-4 (LVDS)     |
| J28       | PMBUS ALERT                            | Installed              | 1        | 2-3 (AFX)           |
| J29       | PMBUS CTRL                             | Installed              | 1        | 2-3 (AFX)           |
| J42       | PMBUS CLK                              | Installed              | 1        | 2-3 (AFX)           |
| J43       | PMBUS DATA                             | Installed              | 1        | 2-3 (AFX)           |
| J47       | PMBUS LEVEL TRANSLATION <sup>(1)</sup> | Installed              | 1        | 1-2 (AFX)           |
| J119      | PMBUS LEVEL TRANSLATION <sup>(1)</sup> | Installed              | 1        | 1-2 (VSMBUS)        |
| J35       | PWR MOD JTAG                           | Installed              | 1        | 2-3                 |
| J162      | JTAG FMC BYPASS                        | Installed              | 1        | 1-2                 |
| J4        | SYSTEM ACE CLOCK                       | Installed              | 1        | 1-2 (ON)            |
| J22       | SYSACE JTAG ENABLE                     | Installed              | 1        | 1-2                 |
| J23       | SYSACE JTAG ENABLE                     | Installed              | 1        | 1-2                 |
| J195      | SYSACE JTAG ENABLE                     | Installed              | 1        | 1-2                 |
| J196      | SYSACE JTAG ENABLE                     | Installed              | 1        | 1-2                 |
| J36       | FMC1 JTAG                              | Installed              | 1        | 2-3                 |

Table A-1: Standard Shunts (Cont'd)

| Connector | Name      | Shunt Position | Quantity | Pins (Jumper Label) |
|-----------|-----------|----------------|----------|---------------------|
| J37       | FMC2 JTAG | Installed      | 1        | 2-3                 |

**Notes:**

1. These entries are not visible in the PCB silkscreen labels.

Table A-2: Digital Power Shorting Plugs

| Connector | Name       | Shorting Plug Position |
|-----------|------------|------------------------|
| J3        | MGTAVCCPLL | Installed              |
| J30       | VCC3V3     | Installed              |
| J31       | VCC2V5     | Installed              |
| J102      | VCCINT     | Installed              |
| J104      | VCCAUX     | Installed              |
| J105      | VCCO       | Installed              |

## VITA 57.1 FMC HPC Connector Pinout

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

|    | K          | J          | H           | G          | F         | E         | D            | C         | B            | A         |
|----|------------|------------|-------------|------------|-----------|-----------|--------------|-----------|--------------|-----------|
| 1  | VREF_B_M2C | GND        | VREF_A_M2C  | GND        | PG_M2C    | GND       | PG_C2M       | GND       | RES1         | GND       |
| 2  | GND        | CLK3_M2C_P | PRSNT_M2C_L | CLK1_M2C_P | GND       | HA01_P_CC | GND          | DP0_C2M_P | GND          | DP1_M2C_P |
| 3  | GND        | CLK3_M2C_N | GND         | CLK1_M2C_N | GND       | HA01_N_CC | GND          | DP0_C2M_N | GND          | DP1_M2C_N |
| 4  | CLK2_M2C_P | GND        | CLK0_M2C_P  | GND        | HA00_P_CC | GND       | GBCLK0_M2C_P | GND       | DP9_M2C_P    | GND       |
| 5  | CLK2_M2C_N | GND        | CLK0_M2C_N  | GND        | HA00_N_CC | GND       | GBCLK0_M2C_N | GND       | DP9_M2C_N    | GND       |
| 6  | GND        | HA03_P     | GND         | LA00_P_CC  | GND       | HA05_P    | GND          | DP0_M2C_P | GND          | DP2_M2C_P |
| 7  | HA02_P     | HA03_N     | LA02_P      | LA00_N_CC  | HA04_P    | HA05_N    | GND          | DP0_M2C_N | GND          | DP2_M2C_N |
| 8  | HA02_N     | GND        | LA02_N      | GND        | HA04_N    | GND       | LA01_P_CC    | GND       | DP8_M2C_P    | GND       |
| 9  | GND        | HA07_P     | GND         | LA03_P     | GND       | HA09_P    | GND          | LA01_N_CC | GND          | DP8_M2C_N |
| 10 | HA06_P     | HA07_N     | LA04_P      | LA03_N     | HA08_P    | HA09_N    | GND          | LA06_P    | GND          | DP3_M2C_P |
| 11 | HA06_N     | GND        | LA04_N      | GND        | HA08_N    | GND       | LA05_P       | LA06_N    | GND          | DP3_M2C_N |
| 12 | GND        | HA11_P     | GND         | LA08_P     | GND       | HA13_P    | LA05_N       | GND       | DP7_M2C_P    | GND       |
| 13 | HA10_P     | HA11_N     | LA07_P      | LA08_N     | HA12_P    | HA13_N    | GND          | GND       | DP7_M2C_N    | GND       |
| 14 | HA10_N     | GND        | LA07_N      | GND        | HA12_N    | GND       | LA09_P       | LA10_P    | GND          | DP4_M2C_P |
| 15 | GND        | HA14_P     | GND         | LA12_P     | GND       | HA16_P    | LA09_N       | LA10_N    | GND          | DP4_M2C_N |
| 16 | HA17_P_CC  | HA14_N     | LA11_P      | LA12_N     | HA15_P    | HA16_N    | GND          | GND       | DP6_M2C_P    | GND       |
| 17 | HA17_N_CC  | GND        | LA11_N      | GND        | HA15_N    | GND       | LA13_P       | GND       | DP6_M2C_N    | GND       |
| 18 | GND        | HA18_P     | GND         | LA16_P     | GND       | HA20_P    | LA13_N       | LA14_P    | GND          | DP5_M2C_P |
| 19 | HA21_P     | HA18_N     | LA15_P      | LA16_N     | HA19_P    | HA20_N    | GND          | LA14_N    | GND          | DP5_M2C_N |
| 20 | HA21_N     | GND        | LA15_N      | GND        | HA19_N    | GND       | LA17_P_CC    | GND       | GBCLK1_M2C_P | GND       |
| 21 | GND        | HA22_P     | GND         | LA20_P     | GND       | HB03_P    | LA17_N_CC    | GND       | GBCLK1_M2C_N | GND       |
| 22 | HA23_P     | HA22_N     | LA19_P      | LA20_N     | HB02_P    | HB03_N    | GND          | LA18_P_CC | GND          | DP1_C2M_P |
| 23 | HA23_N     | GND        | LA19_N      | GND        | HB02_N    | GND       | LA23_P       | LA18_N_CC | GND          | DP1_C2M_N |
| 24 | GND        | HB01_P     | GND         | LA22_P     | GND       | HB05_P    | LA23_N       | GND       | DP9_C2M_P    | GND       |
| 25 | HB00_P_CC  | HB01_N     | LA21_P      | LA22_N     | HB04_P    | HB05_N    | GND          | GND       | DP9_C2M_N    | GND       |
| 26 | HB00_N_CC  | GND        | LA21_N      | GND        | HB04_N    | GND       | LA26_P       | LA27_P    | GND          | DP2_C2M_P |
| 27 | GND        | HB07_P     | GND         | LA25_P     | GND       | HB09_P    | LA26_N       | LA27_N    | GND          | DP2_C2M_N |
| 28 | HB06_P_CC  | HB07_N     | LA24_P      | LA25_N     | HB08_P    | HB09_N    | GND          | GND       | DP8_C2M_P    | GND       |
| 29 | HB06_N_CC  | GND        | LA24_N      | GND        | HB08_N    | GND       | TCK          | GND       | DP8_C2M_N    | GND       |
| 30 | GND        | HB11_P     | GND         | LA29_P     | GND       | HB13_P    | TDI          | SCL       | GND          | DP3_C2M_P |
| 31 | HB10_P     | HB11_N     | LA28_P      | LA29_N     | HB12_P    | HB13_N    | TDO          | SDA       | GND          | DP3_C2M_N |
| 32 | HB10_N     | GND        | LA28_N      | GND        | HB12_N    | GND       | 3P3VAUX      | GND       | DP7_C2M_P    | GND       |
| 33 | GND        | HB15_P     | GND         | LA31_P     | GND       | HB19_P    | TMS          | GND       | DP7_C2M_N    | GND       |
| 34 | HB14_P     | HB15_N     | LA30_P      | LA31_N     | HB16_P    | HB19_N    | TRST_L       | GA0       | GND          | DP4_C2M_P |
| 35 | HB14_N     | GND        | LA30_N      | GND        | HB16_N    | GND       | GA1          | 12P0V     | GND          | DP4_C2M_N |
| 36 | GND        | HB18_P     | GND         | LA33_P     | GND       | HB21_P    | 3P3V         | GND       | DP6_C2M_P    | GND       |
| 37 | HB17_P_CC  | HB18_N     | LA32_P      | LA33_N     | HB20_P    | HB21_N    | GND          | 12P0V     | DP6_C2M_N    | GND       |
| 38 | HB17_N_CC  | GND        | LA32_N      | GND        | HB20_N    | GND       | 3P3V         | GND       | GND          | DP5_C2M_P |
| 39 | GND        | VIO_B_M2C  | GND         | VADJ       | GND       | VADJ      | GND          | 3P3V      | GND          | DP5_C2M_N |
| 40 | VIO_B_M2C  | GND        | VADJ        | GND        | VADJ      | GND       | 3P3V         | GND       | RES0         | GND       |

UG751\_aB\_01\_041310

Figure B-1: FMC HPC Connector Pinout



## SP623 Master UCF Listing

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The SP623 master user constraints file (UCF) template provides for designs targeting the SP623 Spartan-6 FPGA GTP transceiver characterization board. Net names in the constraints listed below correlate with net names on the SP623 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See the [Constraints Guide](#) for more information.

Users can refer to the UCF files generated by tools such as Memory Interface Generator (MIG) for memory interfaces and Base System Builder (BSB) for more detailed I/O standards information required for each particular interface. The FMC connectors J112 and J113 are connected to 2.5V  $V_{CC0}$  banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

### SP623 Master UCF Listing:

|                     |               |
|---------------------|---------------|
| NET "101_REFCLK0_N" | LOC = "A10";  |
| NET "101_REFCLK0_P" | LOC = "B10";  |
| NET "101_REFCLK1_N" | LOC = "C11";  |
| NET "101_REFCLK1_P" | LOC = "D11";  |
| NET "101_RX0_N"     | LOC = "C7";   |
| NET "101_RX0_P"     | LOC = "D7";   |
| NET "101_RX1_N"     | LOC = "C9";   |
| NET "101_RX1_P"     | LOC = "D9";   |
| NET "101_TX0_N"     | LOC = "A6";   |
| NET "101_TX0_P"     | LOC = "B6";   |
| NET "101_TX1_N"     | LOC = "A8";   |
| NET "101_TX1_P"     | LOC = "B8";   |
| NET "123_REFCLK0_N" | LOC = "C15";  |
| NET "123_REFCLK0_P" | LOC = "D15";  |
| NET "123_REFCLK1_N" | LOC = "A16";  |
| NET "123_REFCLK1_P" | LOC = "B16";  |
| NET "123_RX0_N"     | LOC = "C17";  |
| NET "123_RX0_P"     | LOC = "D17";  |
| NET "123_RX1_N"     | LOC = "C19";  |
| NET "123_RX1_P"     | LOC = "D19";  |
| NET "123_TX0_N"     | LOC = "A18";  |
| NET "123_TX0_P"     | LOC = "B18";  |
| NET "123_TX1_N"     | LOC = "A20";  |
| NET "123_TX1_P"     | LOC = "B20";  |
| NET "245_REFCLK0_N" | LOC = "AF11"; |
| NET "245_REFCLK0_P" | LOC = "AE11"; |
| NET "245_REFCLK1_N" | LOC = "AD12"; |
| NET "245_REFCLK1_P" | LOC = "AC12"; |
| NET "245_RX0_N"     | LOC = "AD8";  |
| NET "245_RX0_P"     | LOC = "AC8";  |
| NET "245_RX1_N"     | LOC = "AD10"; |

|                     |               |
|---------------------|---------------|
| NET "245_RX1_P"     | LOC = "AC10"; |
| NET "245_TX0_N"     | LOC = "AF7";  |
| NET "245_TX0_P"     | LOC = "AE7";  |
| NET "245_TX1_N"     | LOC = "AF9";  |
| NET "245_TX1_P"     | LOC = "AE9";  |
| NET "267_REFCLK0_N" | LOC = "AD16"; |
| NET "267_REFCLK0_P" | LOC = "AC16"; |
| NET "267_REFCLK1_N" | LOC = "AF17"; |
| NET "267_REFCLK1_P" | LOC = "AE17"; |
| NET "267_RX0_N"     | LOC = "AD18"; |
| NET "267_RX0_P"     | LOC = "AC18"; |
| NET "267_RX1_N"     | LOC = "AD20"; |
| NET "267_RX1_P"     | LOC = "AC20"; |
| NET "267_TX0_N"     | LOC = "AF19"; |
| NET "267_TX0_P"     | LOC = "AE19"; |
| NET "267_TX1_N"     | LOC = "AF21"; |
| NET "267_TX1_P"     | LOC = "AE21"; |
| NET "AWAKE_1"       | LOC = "AC23"; |
| NET "CCLK_2"        | LOC = "AE24"; |
| NET "CM_CTRL_0"     | LOC = "U20";  |
| NET "CM_CTRL_1"     | LOC = "U19";  |
| NET "CM_CTRL_10"    | LOC = "Y26";  |
| NET "CM_CTRL_11"    | LOC = "Y24";  |
| NET "CM_CTRL_12"    | LOC = "AC26"; |
| NET "CM_CTRL_13"    | LOC = "AC25"; |
| NET "CM_CTRL_14"    | LOC = "AB26"; |
| NET "CM_CTRL_15"    | LOC = "AB24"; |
| NET "CM_CTRL_16"    | LOC = "AD26"; |
| NET "CM_CTRL_17"    | LOC = "AD24"; |
| NET "CM_CTRL_18"    | LOC = "AA26"; |
| NET "CM_CTRL_19"    | LOC = "AA25"; |
| NET "CM_CTRL_2"     | LOC = "AA24"; |
| NET "CM_CTRL_20"    | LOC = "W26";  |
| NET "CM_CTRL_21"    | LOC = "W25";  |
| NET "CM_CTRL_22"    | LOC = "V24";  |
| NET "CM_CTRL_23"    | LOC = "T23";  |
| NET "CM_CTRL_3"     | LOC = "AA23"; |
| NET "CM_CTRL_4"     | LOC = "T20";  |
| NET "CM_CTRL_5"     | LOC = "T19";  |
| NET "CM_CTRL_6"     | LOC = "U22";  |
| NET "CM_CTRL_7"     | LOC = "U21";  |
| NET "CM_CTRL_8"     | LOC = "AE26"; |
| NET "CM_CTRL_9"     | LOC = "AE25"; |
| NET "CM_GCLK_N"     | LOC = "U26";  |
| NET "CM_GCLK_P"     | LOC = "U25";  |
| NET "CM_LVDS1_N"    | LOC = "E12";  |
| NET "CM_LVDS1_P"    | LOC = "F12";  |
| NET "CM_LVDS2_N"    | LOC = "W12";  |
| NET "CM_LVDS2_P"    | LOC = "V12";  |
| NET "CM_LVDS3_N"    | LOC = "F11";  |
| NET "CM_LVDS3_P"    | LOC = "G12";  |
| NET "CM_RST"        | LOC = "T22";  |
| NET "CMPCS_B_2"     | LOC = "Y19";  |
| NET "CSO_B_2"       | LOC = "AF3";  |
| NET "DOUT_BUSY_1"   | LOC = "AC24"; |
| NET "DUT_I2C_SCL"   | LOC = "J23";  |
| NET "DUT_I2C_SDA"   | LOC = "J24";  |
| NET "DUT_PMB_ALERT" | LOC = "E24";  |
| NET "DUT_PMB_CLK"   | LOC = "L19";  |

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NET "DUT_PMB_CTRL"          LOC = "E23";
NET "DUT_PMB_DATA"          LOC = "K20";
NET "DUT_SPI_CS"            LOC = "B26";
NET "DUT_SPI_D"             LOC = "C26";
NET "DUT_SPI_Q"             LOC = "B25";
NET "DUT_SPI_SCK"           LOC = "C25";
NET "FMC1_CLK0_M2C_N"       LOC = "T1";
NET "FMC1_CLK0_M2C_P"       LOC = "T3";
NET "FMC1_CLK1_M2C_N"       LOC = "A14";
NET "FMC1_CLK1_M2C_P"       LOC = "B14";
NET "FMC1_CLK2_M2C_N"       LOC = "W3";
NET "FMC1_CLK2_M2C_P"       LOC = "V4";
NET "FMC1_HA00_CC_N"        LOC = "R1";
NET "FMC1_HA00_CC_P"        LOC = "R2";
NET "FMC1_HA01_CC_N"        LOC = "N3";
NET "FMC1_HA01_CC_P"        LOC = "M4";
NET "FMC1_HA02_N"           LOC = "N1";
NET "FMC1_HA02_P"           LOC = "N2";
NET "FMC1_HA03_N"           LOC = "M1";
NET "FMC1_HA03_P"           LOC = "M3";
NET "FMC1_HA04_N"           LOC = "L1";
NET "FMC1_HA04_P"           LOC = "L2";
NET "FMC1_HA05_N"           LOC = "K1";
NET "FMC1_HA05_P"           LOC = "K3";
NET "FMC1_HA06_N"           LOC = "J1";
NET "FMC1_HA06_P"           LOC = "J2";
NET "FMC1_HA07_N"           LOC = "H1";
NET "FMC1_HA07_P"           LOC = "H3";
NET "FMC1_HA08_N"           LOC = "G1";
NET "FMC1_HA08_P"           LOC = "G2";
NET "FMC1_HA09_N"           LOC = "F1";
NET "FMC1_HA09_P"           LOC = "F3";
NET "FMC1_HA10_N"           LOC = "E1";
NET "FMC1_HA10_P"           LOC = "E2";
NET "FMC1_HA11_N"           LOC = "D1";
NET "FMC1_HA11_P"           LOC = "D3";
NET "FMC1_HA12_N"           LOC = "J3";
NET "FMC1_HA12_P"           LOC = "J4";
NET "FMC1_HA13_N"           LOC = "L8";
NET "FMC1_HA13_P"           LOC = "L9";
NET "FMC1_HA14_N"           LOC = "L3";
NET "FMC1_HA14_P"           LOC = "L4";
NET "FMC1_HA15_N"           LOC = "M6";
NET "FMC1_HA15_P"           LOC = "M8";
NET "FMC1_HA16_N"           LOC = "J5";
NET "FMC1_HA16_P"           LOC = "K5";
NET "FMC1_HA17_CC_N"        LOC = "L6";
NET "FMC1_HA17_CC_P"        LOC = "L7";
NET "FMC1_HA18_N"           LOC = "B1";
NET "FMC1_HA18_P"           LOC = "B2";
NET "FMC1_HA19_N"           LOC = "K10";
NET "FMC1_HA19_P"           LOC = "L10";
NET "FMC1_HA20_N"           LOC = "G3";
NET "FMC1_HA20_P"           LOC = "G4";
NET "FMC1_HA21_N"           LOC = "J7";
NET "FMC1_HA21_P"           LOC = "J9";
NET "FMC1_HA22_N"           LOC = "C1";
NET "FMC1_HA22_P"           LOC = "C2";
NET "FMC1_HA23_N"           LOC = "K8";

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|                      |              |
|----------------------|--------------|
| NET "FMC1_HA23_P"    | LOC = "K9";  |
| NET "FMC1_LA00_CC_N" | LOC = "D13"; |
| NET "FMC1_LA00_CC_P" | LOC = "E13"; |
| NET "FMC1_LA01_CC_N" | LOC = "A13"; |
| NET "FMC1_LA01_CC_P" | LOC = "C13"; |
| NET "FMC1_LA02_N"    | LOC = "G9";  |
| NET "FMC1_LA02_P"    | LOC = "H9";  |
| NET "FMC1_LA03_N"    | LOC = "A2";  |
| NET "FMC1_LA03_P"    | LOC = "A3";  |
| NET "FMC1_LA04_N"    | LOC = "E8";  |
| NET "FMC1_LA04_P"    | LOC = "F9";  |
| NET "FMC1_LA05_N"    | LOC = "C5";  |
| NET "FMC1_LA05_P"    | LOC = "D5";  |
| NET "FMC1_LA06_N"    | LOC = "G7";  |
| NET "FMC1_LA06_P"    | LOC = "H7";  |
| NET "FMC1_LA07_N"    | LOC = "G10"; |
| NET "FMC1_LA07_P"    | LOC = "H10"; |
| NET "FMC1_LA08_N"    | LOC = "A4";  |
| NET "FMC1_LA08_P"    | LOC = "B4";  |
| NET "FMC1_LA09_N"    | LOC = "E10"; |
| NET "FMC1_LA09_P"    | LOC = "F10"; |
| NET "FMC1_LA10_N"    | LOC = "A5";  |
| NET "FMC1_LA10_P"    | LOC = "B5";  |
| NET "FMC1_LA11_N"    | LOC = "G8";  |
| NET "FMC1_LA11_P"    | LOC = "H8";  |
| NET "FMC1_LA12_N"    | LOC = "G11"; |
| NET "FMC1_LA12_P"    | LOC = "J11"; |
| NET "FMC1_LA13_N"    | LOC = "G13"; |
| NET "FMC1_LA13_P"    | LOC = "H12"; |
| NET "FMC1_LA14_N"    | LOC = "J12"; |
| NET "FMC1_LA14_P"    | LOC = "K12"; |
| NET "FMC1_LA15_N"    | LOC = "F6";  |
| NET "FMC1_LA15_P"    | LOC = "F7";  |
| NET "FMC1_LA16_N"    | LOC = "H15"; |
| NET "FMC1_LA16_P"    | LOC = "J15"; |
| NET "FMC1_LA17_CC_N" | LOC = "A12"; |
| NET "FMC1_LA17_CC_P" | LOC = "B12"; |
| NET "FMC1_LA18_CC_N" | LOC = "J17"; |
| NET "FMC1_LA18_CC_P" | LOC = "J16"; |
| NET "FMC1_LA19_N"    | LOC = "E16"; |
| NET "FMC1_LA19_P"    | LOC = "F16"; |
| NET "FMC1_LA20_N"    | LOC = "B3";  |
| NET "FMC1_LA20_P"    | LOC = "C3";  |
| NET "FMC1_LA21_N"    | LOC = "F15"; |
| NET "FMC1_LA21_P"    | LOC = "G15"; |
| NET "FMC1_LA22_N"    | LOC = "E18"; |
| NET "FMC1_LA22_P"    | LOC = "F18"; |
| NET "FMC1_LA23_N"    | LOC = "F17"; |
| NET "FMC1_LA23_P"    | LOC = "G16"; |
| NET "FMC1_LA24_N"    | LOC = "E20"; |
| NET "FMC1_LA24_P"    | LOC = "F20"; |
| NET "FMC1_LA25_N"    | LOC = "G17"; |
| NET "FMC1_LA25_P"    | LOC = "H17"; |
| NET "FMC1_LA26_N"    | LOC = "B21"; |
| NET "FMC1_LA26_P"    | LOC = "C21"; |
| NET "FMC1_LA27_N"    | LOC = "F5";  |
| NET "FMC1_LA27_P"    | LOC = "G6";  |
| NET "FMC1_LA28_N"    | LOC = "H19"; |
| NET "FMC1_LA28_P"    | LOC = "H18"; |

|                       |               |
|-----------------------|---------------|
| NET "FMC1_LA29_N"     | LOC = "A22";  |
| NET "FMC1_LA29_P"     | LOC = "B22";  |
| NET "FMC1_LA30_N"     | LOC = "F19";  |
| NET "FMC1_LA30_P"     | LOC = "G19";  |
| NET "FMC1_LA31_N"     | LOC = "A23";  |
| NET "FMC1_LA31_P"     | LOC = "B23";  |
| NET "FMC1_LA32_N"     | LOC = "D22";  |
| NET "FMC1_LA32_P"     | LOC = "D21";  |
| NET "FMC1_LA33_N"     | LOC = "E5";   |
| NET "FMC1_LA33_P"     | LOC = "E6";   |
| NET "FMC1_PRSNT_M2C"  | LOC = "E3";   |
| NET "FMC2_CLK0_M2C_N" | LOC = "U24";  |
| NET "FMC2_CLK0_M2C_P" | LOC = "U23";  |
| NET "FMC2_CLK1_M2C_N" | LOC = "AF14"; |
| NET "FMC2_CLK1_M2C_P" | LOC = "AD14"; |
| NET "FMC2_HA00_CC_N"  | LOC = "R6";   |
| NET "FMC2_HA00_CC_P"  | LOC = "R7";   |
| NET "FMC2_HA02_N"     | LOC = "U3";   |
| NET "FMC2_HA02_P"     | LOC = "U4";   |
| NET "FMC2_HA03_N"     | LOC = "W5";   |
| NET "FMC2_HA03_P"     | LOC = "V5";   |
| NET "FMC2_HA04_N"     | LOC = "U8";   |
| NET "FMC2_HA04_P"     | LOC = "U9";   |
| NET "FMC2_HA05_N"     | LOC = "T6";   |
| NET "FMC2_HA05_P"     | LOC = "U7";   |
| NET "FMC2_HA06_N"     | LOC = "AB1";  |
| NET "FMC2_HA06_P"     | LOC = "AB3";  |
| NET "FMC2_HA07_N"     | LOC = "AD1";  |
| NET "FMC2_HA07_P"     | LOC = "AD3";  |
| NET "FMC2_HA08_N"     | LOC = "AC1";  |
| NET "FMC2_HA08_P"     | LOC = "AC2";  |
| NET "FMC2_HA09_N"     | LOC = "AE1";  |
| NET "FMC2_HA09_P"     | LOC = "AE2";  |
| NET "FMC2_HA10_N"     | LOC = "AA1";  |
| NET "FMC2_HA10_P"     | LOC = "AA2";  |
| NET "FMC2_HA11_N"     | LOC = "Y1";   |
| NET "FMC2_HA11_P"     | LOC = "Y3";   |
| NET "FMC2_HA12_N"     | LOC = "W1";   |
| NET "FMC2_HA12_P"     | LOC = "W2";   |
| NET "FMC2_HA13_N"     | LOC = "T9";   |
| NET "FMC2_HA13_P"     | LOC = "R10";  |
| NET "FMC2_HA14_N"     | LOC = "P1";   |
| NET "FMC2_HA14_P"     | LOC = "P3";   |
| NET "FMC2_HA15_N"     | LOC = "P6";   |
| NET "FMC2_HA15_P"     | LOC = "N6";   |
| NET "FMC2_HA16_N"     | LOC = "R5";   |
| NET "FMC2_HA16_P"     | LOC = "P5";   |
| NET "FMC2_HA17_CC_N"  | LOC = "N7";   |
| NET "FMC2_HA17_CC_P"  | LOC = "N8";   |
| NET "FMC2_HA18_N"     | LOC = "R3";   |
| NET "FMC2_HA18_P"     | LOC = "R4";   |
| NET "FMC2_HA19_N"     | LOC = "P8";   |
| NET "FMC2_HA19_P"     | LOC = "R9";   |
| NET "FMC2_HA20_N"     | LOC = "N4";   |
| NET "FMC2_HA20_P"     | LOC = "N5";   |
| NET "FMC2_HA21_N"     | LOC = "N9";   |
| NET "FMC2_HA21_P"     | LOC = "P10";  |
| NET "FMC2_HA22_N"     | LOC = "M9";   |
| NET "FMC2_HA22_P"     | LOC = "M10";  |

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|----------------------|---------------|
| NET "FMC2_HA23_N"    | LOC = "Y5";   |
| NET "FMC2_HA23_P"    | LOC = "Y6";   |
| NET "FMC2_LA00_CC_N" | LOC = "AC14"; |
| NET "FMC2_LA00_CC_P" | LOC = "AB14"; |
| NET "FMC2_LA01_CC_N" | LOC = "AF13"; |
| NET "FMC2_LA01_CC_P" | LOC = "AE13"; |
| NET "FMC2_LA02_N"    | LOC = "W19";  |
| NET "FMC2_LA02_P"    | LOC = "V18";  |
| NET "FMC2_LA03_N"    | LOC = "W18";  |
| NET "FMC2_LA03_P"    | LOC = "W17";  |
| NET "FMC2_LA04_N"    | LOC = "AB21"; |
| NET "FMC2_LA04_P"    | LOC = "AA21"; |
| NET "FMC2_LA05_N"    | LOC = "AA17"; |
| NET "FMC2_LA05_P"    | LOC = "Y17";  |
| NET "FMC2_LA06_N"    | LOC = "V16";  |
| NET "FMC2_LA06_P"    | LOC = "U15";  |
| NET "FMC2_LA07_N"    | LOC = "AB19"; |
| NET "FMC2_LA07_P"    | LOC = "AA19"; |
| NET "FMC2_LA08_N"    | LOC = "Y16";  |
| NET "FMC2_LA08_P"    | LOC = "W16";  |
| NET "FMC2_LA09_N"    | LOC = "AB17"; |
| NET "FMC2_LA09_P"    | LOC = "AA18"; |
| NET "FMC2_LA10_N"    | LOC = "AA16"; |
| NET "FMC2_LA10_P"    | LOC = "Y15";  |
| NET "FMC2_LA11_N"    | LOC = "V15";  |
| NET "FMC2_LA11_P"    | LOC = "V14";  |
| NET "FMC2_LA12_N"    | LOC = "V13";  |
| NET "FMC2_LA12_P"    | LOC = "U13";  |
| NET "FMC2_LA13_N"    | LOC = "AB15"; |
| NET "FMC2_LA13_P"    | LOC = "AA15"; |
| NET "FMC2_LA14_N"    | LOC = "AA22"; |
| NET "FMC2_LA14_P"    | LOC = "Y21";  |
| NET "FMC2_LA15_N"    | LOC = "AA12"; |
| NET "FMC2_LA15_P"    | LOC = "Y12";  |
| NET "FMC2_LA16_N"    | LOC = "Y13";  |
| NET "FMC2_LA16_P"    | LOC = "W14";  |
| NET "FMC2_LA17_CC_N" | LOC = "AF15"; |
| NET "FMC2_LA17_CC_P" | LOC = "AE15"; |
| NET "FMC2_LA18_CC_N" | LOC = "AF23"; |
| NET "FMC2_LA18_CC_P" | LOC = "AD23"; |
| NET "FMC2_LA19_N"    | LOC = "AA11"; |
| NET "FMC2_LA19_P"    | LOC = "Y11";  |
| NET "FMC2_LA20_N"    | LOC = "V10";  |
| NET "FMC2_LA20_P"    | LOC = "V11";  |
| NET "FMC2_LA21_N"    | LOC = "AB9";  |
| NET "FMC2_LA21_P"    | LOC = "AA9";  |
| NET "FMC2_LA22_N"    | LOC = "AB11"; |
| NET "FMC2_LA22_P"    | LOC = "AA10"; |
| NET "FMC2_LA23_N"    | LOC = "AF6";  |
| NET "FMC2_LA23_P"    | LOC = "AD6";  |
| NET "FMC2_LA24_N"    | LOC = "Y20";  |
| NET "FMC2_LA24_P"    | LOC = "W20";  |
| NET "FMC2_LA25_N"    | LOC = "W9";   |
| NET "FMC2_LA25_P"    | LOC = "W10";  |
| NET "FMC2_LA26_N"    | LOC = "AF5";  |
| NET "FMC2_LA26_P"    | LOC = "AE5";  |
| NET "FMC2_LA27_N"    | LOC = "AA8";  |
| NET "FMC2_LA27_P"    | LOC = "Y9";   |
| NET "FMC2_LA28_N"    | LOC = "AC6";  |

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NET "FMC2_LA28_P"          LOC = "AB7";
NET "FMC2_LA29_N"          LOC = "AC22";
NET "FMC2_LA29_P"          LOC = "AB22";
NET "FMC2_LA30_N"          LOC = "AD5";
NET "FMC2_LA30_P"          LOC = "AC5";
NET "FMC2_LA31_N"          LOC = "W7";
NET "FMC2_LA31_P"          LOC = "W8";
NET "FMC2_LA32_N"          LOC = "AF4";
NET "FMC2_LA32_P"          LOC = "AD4";
NET "FMC2_LA33_N"          LOC = "AA6";
NET "FMC2_LA33_P"          LOC = "AA7";
NET "FMC2_PRSENT_M2C"      LOC = "AC3";
NET "HSWAPEN_0"            LOC = "A1";
NET "INIT_B_2"             LOC = "AE3";
NET "IO_L36N_2_AA13"        LOC = "AA13";
NET "IO_L36P_2_AB13"        LOC = "AB13";
NET "IO_L39N_M3LDQSN_3_V1" LOC = "V1";
NET "IO_L39P_M3LDQS_3_V3"  LOC = "V3";
NET "IO_L40N_M3DQ7_3_U1"   LOC = "U1";
NET "IO_L40P_M3DQ6_3_U2"   LOC = "U2";
NET "IO_LVDS_CLK_N"         LOC = "W24";
NET "IO_LVDS_CLK_P"         LOC = "V23";
NET "LED1"                  LOC = "L21";
NET "LED2"                  LOC = "L20";
NET "LED3"                  LOC = "M23";
NET "LED4"                  LOC = "M21";
NET "LED5"                  LOC = "N26";
NET "LED6"                  LOC = "N25";
NET "LED7"                  LOC = "L26";
NET "LED8"                  LOC = "L25";
NET "M0_CMPMISO_2"          LOC = "AF24";
NET "M1_2"                  LOC = "AD22";
NET "PB_SW1"                LOC = "M26";
NET "PB_SW2"                LOC = "M24";
NET "RFUSE"                 LOC = "V19";
NET "SMA_CLK_N"             LOC = "R26";
NET "SMA_CLK_P"             LOC = "R25";
NET "SW1"                   LOC = "J26";
NET "SW2"                   LOC = "J25";
NET "SW3"                   LOC = "K26";
NET "SW4"                   LOC = "K24";
NET "SW5"                   LOC = "G26";
NET "SW6"                   LOC = "G25";
NET "SW7"                   LOC = "H26";
NET "SW8"                   LOC = "H24";
NET "USB_CTS"               LOC = "L23";
NET "USB_GPIO0"             LOC = "P22";
NET "USB_GPIO1"             LOC = "P21";
NET "USB_GPIO2"             LOC = "N22";
NET "USB_GPIO3"             LOC = "N21";
NET "USB_RTS"               LOC = "L24";
NET "USB_RX"                LOC = "N20";
NET "USB_TX"                LOC = "N19";
NET "VFS"                   LOC = "W22";

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# *References*

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Additional information relevant to Spartan®-6 devices, the SP623 Spartan-6 FPGA GTP transceiver characterization board, and intellectual property is available in the documents listed here:

- [DS162](#), Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
- [UG380](#), Spartan-6 FPGA Configuration User Guide
- [UG385](#), Spartan-6 FPGA Packaging and Pinout Specifications
- [UG381](#), Spartan-6 FPGA SelectIO Resources User Guide
- [UG388](#), Spartan-6 FPGA Memory Controller User Guide
- [DS080](#), System ACE CompactFlash Solution Data Sheet
- [UG386](#), Spartan-6 FPGA GTP Transceivers User Guide
- [DS606](#), XPS IIC Bus Interface Data Sheet
- [DS614](#), Clock Generator (v3.01a) Data Sheet
- HW-CLK-101-SCLK2 SuperClock-2 Module User Guide

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>.

