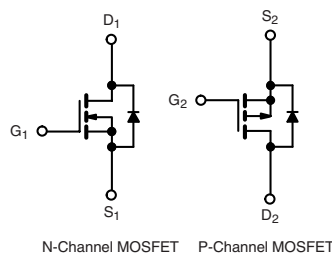
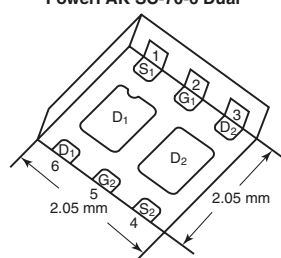


N- and P-Channel 12 V (D-S) MOSFET

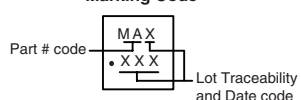
PRODUCT SUMMARY

	N-CHANNEL	P-CHANNEL
V_{DS} (V)	12	- 12
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.040	0.070
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 2.5$ V	0.048	0.100
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 1.8$ V	0.063	0.140
I_D (A) ^a	4.5	- 4.5
Configuration	N- and P-Pair	

PowerPAK SC-70-6 Dual



Marking Code



FEATURES

- High Quality Manufacturing Process Using SMM Process Flow
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- Compliant to RoHS Directive 2002/95/EC
- Find out more about Vishay's Medical Products at: www.vishay.com/medical-mosfets



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATION EXAMPLES

- Medical Implantable Applications Including
 - Drug Delivery Systems
 - Defibrillators
 - Pacemakers
 - Hearing Aids
 - Other Implantable Devices
- Load Switch for Portable Devices

ORDERING INFORMATION

Package	PowerPAK SC-70
Lead (Pb)-free and Halogen-free	SMMA511DJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-Source Voltage		V _{DS}	12	- 12	V
Gate-Source Voltage		V _{GS}	± 8	± 8	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C ^a	I _D	4.5	- 4.5	A
	T _C = 70 °C ^a		4.5	- 4.5	
	T _A = 25 °C ^{a, b, c}		4.5	- 4.3	
	T _A = 70 °C ^{a, b, c}		4.5	- 3.4	
Pulsed Drain Current		I _{DM}	20	- 10	
Continuous Source-Drain Diode Current	T _C = 25 °C ^a	I _S	4.5	- 4.5	
	T _A = 25 °C ^{b, c}		1.6	- 1.6	
Maximum Power Dissipation	T _C = 25 °C	P _D	6.5	6.5	W
	T _C = 70 °C		5	5	
	T _A = 25 °C ^{a, c}		1.9	1.9	
	T _A = 70 °C ^{a, c}		1.2	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	12.5	16	12.5	16	

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. Package limit is $\pm 4.5 \text{ A}$.c. $t = 5 \text{ s}$.d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 110 °C/W .SPECIFICATIONS $T_J = 25 \text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		N-Ch	12	-	V	
		V _{GS} = 0 V, I _D = - 250 μA		P-Ch	- 12	-		
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		N-Ch	-	12	mV/°C	
		I _D = - 250 μA		P-Ch	-	- 7		
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA		N-Ch	-	- 2.8	mV/°C	
		I _D = - 250 μA		P-Ch	-	2.1		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	0.4	-	V	
		V _{DS} = V _{GS} , I _D = - 250 μA		P-Ch	- 0.4	-		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 12 V	N-Ch	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = - 12 V	P-Ch	-	-	- 1	
		V _{GS} = 0 V	V _{DS} = 12 V, T _J = 55 °C	N-Ch	-	-	10	
		V _{GS} = 0 V	V _{DS} = - 12 V, T _J = 55 °C	P-Ch	-	-	- 10	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	N-Ch	15	-	-	A
		V _{GS} = - 4.5 V	V _{DS} ≤ - 5 V	P-Ch	- 8	-	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 4.2 A	N-Ch	-	0.033	0.040	Ω
		V _{GS} = - 4.5 V	I _D = - 3.3 A	P-Ch	-	0.058	0.070	
		V _{GS} = 2.5 V	I _D = 3.8 A	N-Ch	-	0.039	0.048	
		V _{GS} = - 2.5 V	I _D = - 2.8 A	P-Ch	-	0.082	0.100	
		V _{GS} = 1.8 V	I _D = 1.6 A	N-Ch	-	0.051	0.063	
		V _{GS} = - 1.8 V	I _D = - 0.7 A	P-Ch	-	0.111	0.140	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.2 A		N-Ch	-	13	-	S
		V _{DS} = - 10 V, I _D = - 3.3 A		P-Ch	-	9	-	
Dynamic ^b								
Input Capacitance	C _{iss}	V _{GS} = 0 V	N-Channel V _{DS} = 6 V, f = 1 MHz	N-Ch	-	400	-	pF
Output Capacitance	C _{oss}			P-Ch	-	400	-	
			N-Ch	-	120	-		
			P-Ch	-	140	-		
			Reverse Transfer Capacitance	C _{rss}	N-Ch	-	70	
P-Ch	-				100	-		

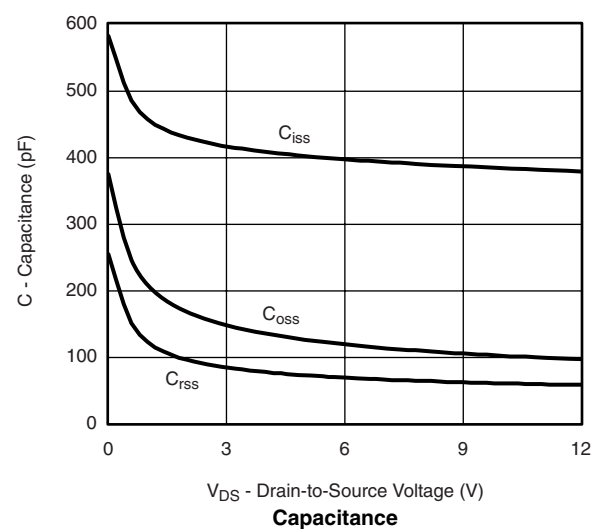
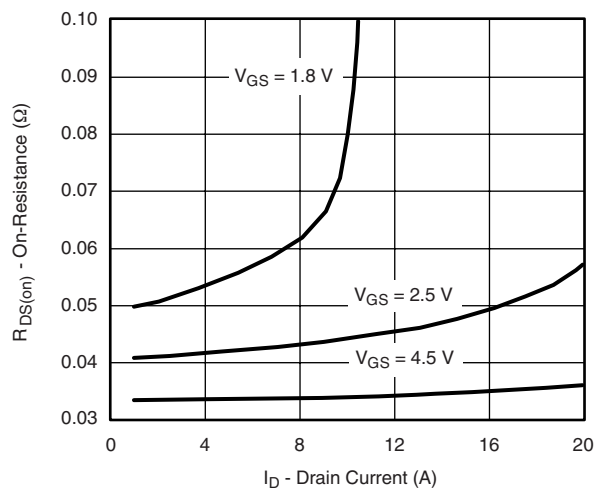
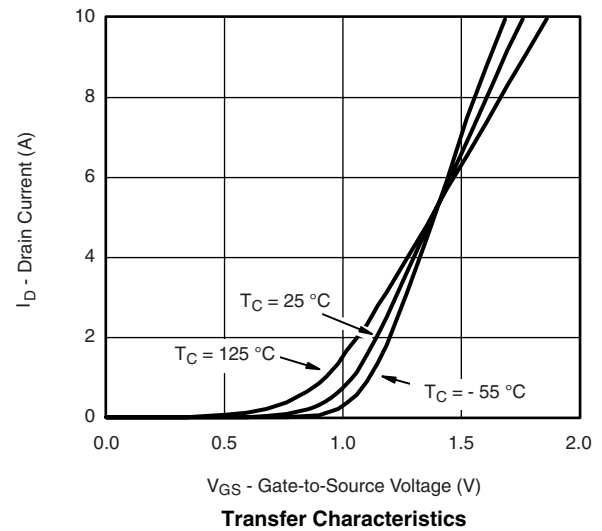
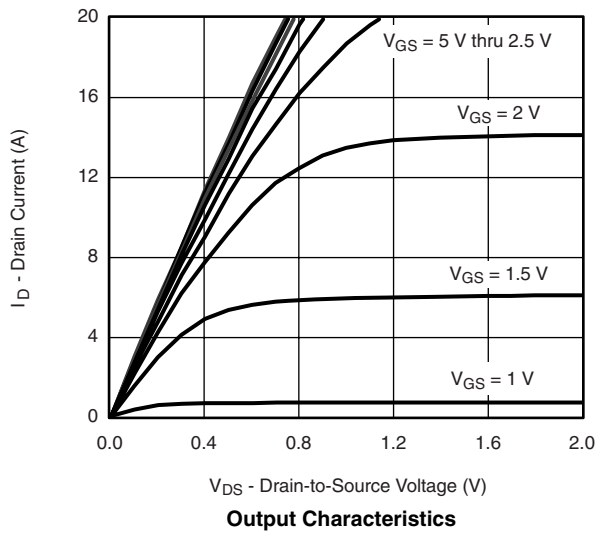
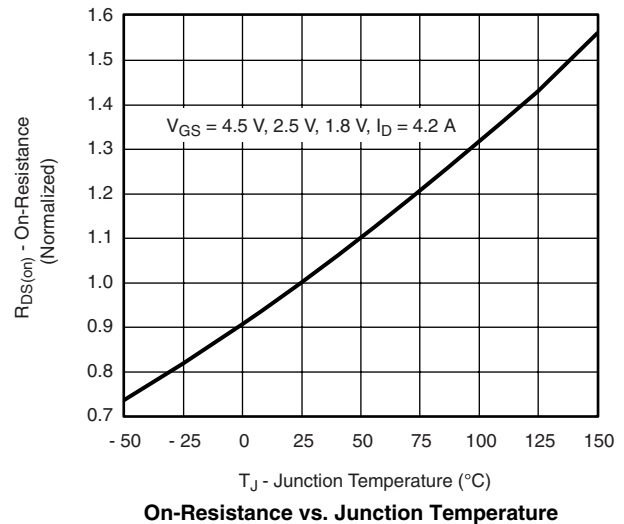
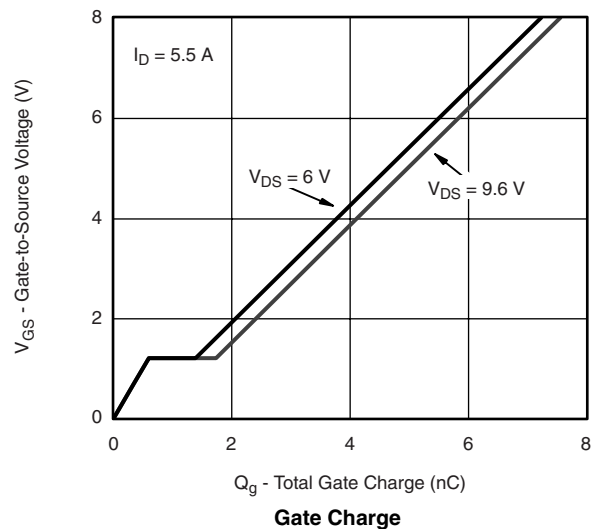


SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT	
Dynamic ^b									
Total Gate Charge	Q _g	V _{GS} = 8 V	V _{DS} = 6 V, I _D = 5.5 A	N-Ch	-	7.5	12	nC	
		V _{GS} = - 8 V	V _{DS} = - 6 V, I _D = - 4.3 A	P-Ch	-	8	12		
		V _{GS} = 4.5 V	N-Channel V _{DS} = 6 V, I _D = 5.5 A	N-Ch	-	4.5	6.8		
		V _{GS} = - 4.5 V		P-Ch	-	5	7.5		
Gate-Source Charge	Q _{gs}	V _{GS} = 4.5 V	P-Channel V _{DS} = - 6 V, I _D = - 4.3 A	N-Ch	-	0.6	-		
		V _{GS} = - 4.5 V		P-Ch	-	0.8	-		
Gate-Drain Charge	Q _{gd}	V _{GS} = 4.5 V		N-Ch	-	0.8	-		
		V _{GS} = - 4.5 V		P-Ch	-	1.4	-		
Gate Resistance	R _g	f = 1 MHz			N-Ch	-	2.5	-	Ω
					P-Ch	-	7	-	
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 1.4 Ω I _D ≅ 4.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω P-Channel V _{DD} = - 6 V, R _L = 1.8 Ω I _D ≅ - 3.4 A, V _{GEN} = - 4.5 V, R _g = 1 Ω			N-Ch	-	5	10	ns
Rise Time	t _r				P-Ch	-	15	25	
					N-Ch	-	15	25	
Turn-Off Delay Time	t _{d(off)}				P-Ch	-	25	40	
					N-Ch	-	35	55	
Fall Time	t _f				P-Ch	-	20	30	
					N-Ch	-	15	25	
Turn-On Delay Time	t _{d(on)}				P-Ch	-	10	15	
		N-Ch	-	5	10				
Rise Time	t _r	P-Ch	-	5	10				
		N-Ch	-	10	15				
Turn-Off Delay Time	t _{d(off)}	P-Ch	-	12	20				
		N-Ch	-	15	25				
Fall Time	t _f	P-Ch	-	20	30				
		N-Ch	-	10	15				
Source-Drain Body Diode Characteristics									
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			N-Ch	-	-	4.5	A
					P-Ch	-	-	- 4.5	
Pulse Diode Forward Current	I _{SM}				N-Ch	-	-	20	
					P-Ch	-	-	- 10	
Body Diode Voltage	V _{SD}	V _{GS} = 0 V	I _S = 4.4 A	N-Ch	-	0.8	1.2	V	
			I _S = - 3.4 A	P-Ch	-	- 0.8	- 1.2		
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 4.4 A, di/dt = 100 A/μs, T _J = 25 °C P-Channel I _F = - 3.4 A, di/dt = - 100 A/μs, T _J = 25 °C			N-Ch	-	15	30	ns
					P-Ch	-	30	60	
Body Diode Reverse Recovery Charge	Q _{rr}				N-Ch	-	8	20	nC
					P-Ch	-	12	24	
Reverse Recovery Fall Time	t _a				N-Ch	-	8.5	-	ns
					P-Ch	-	14	-	
Reverse Recovery Rise Time	t _b				N-Ch	-	8.5	-	
					P-Ch	-	16	-	

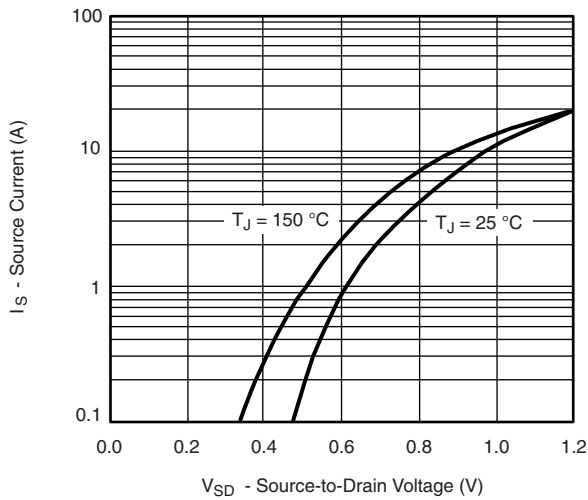
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

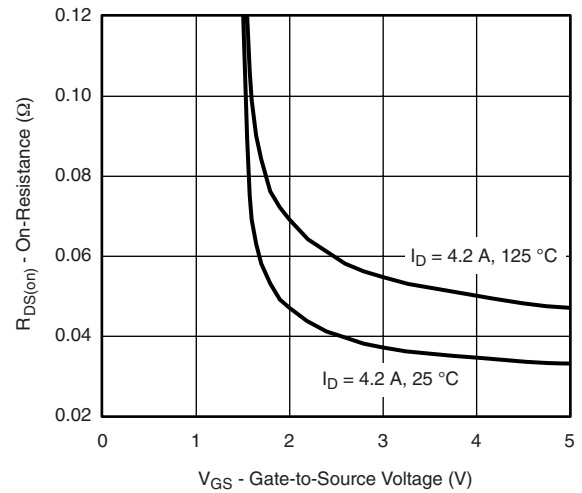
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted**On-Resistance vs. Drain Current and Gate Voltage**

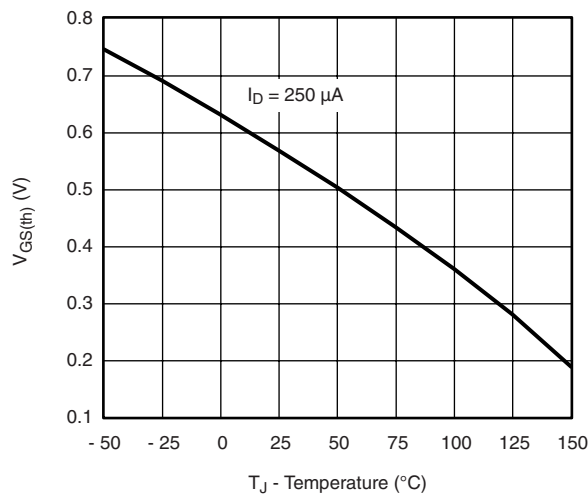
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



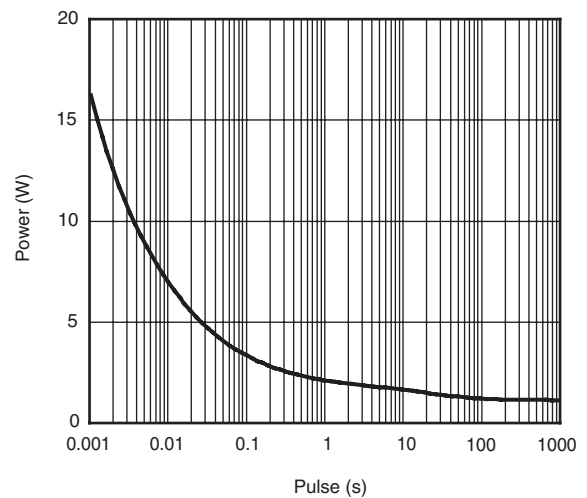
Source-Drain Diode Forward Voltage



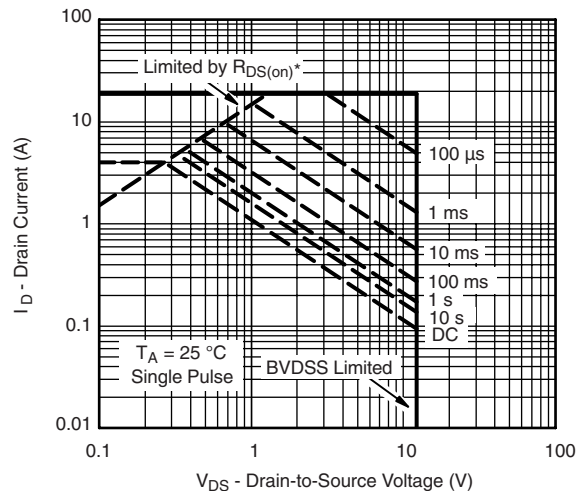
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

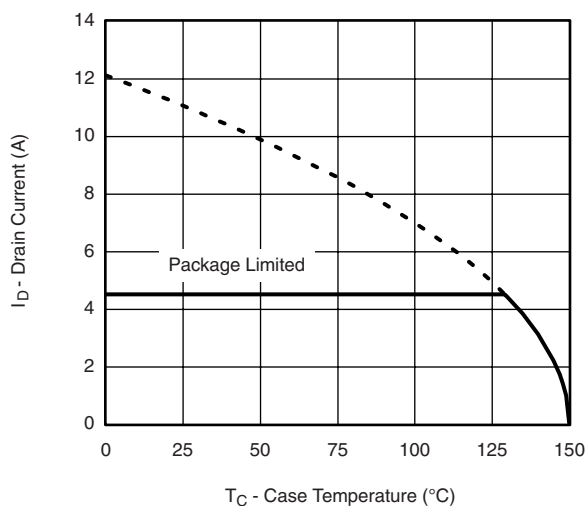
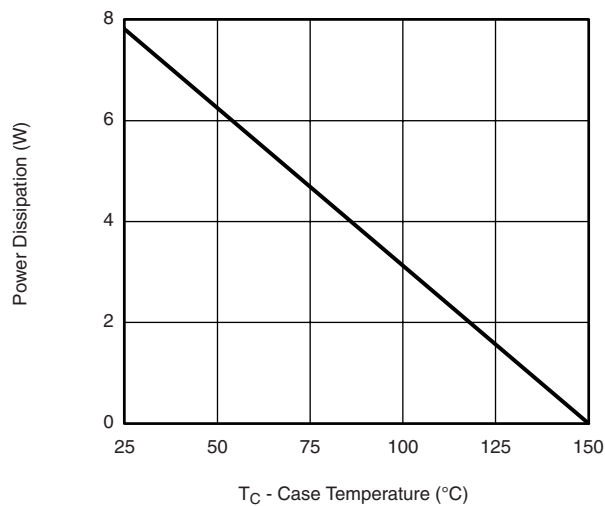


Single Pulse Power, Junction-to-Ambient



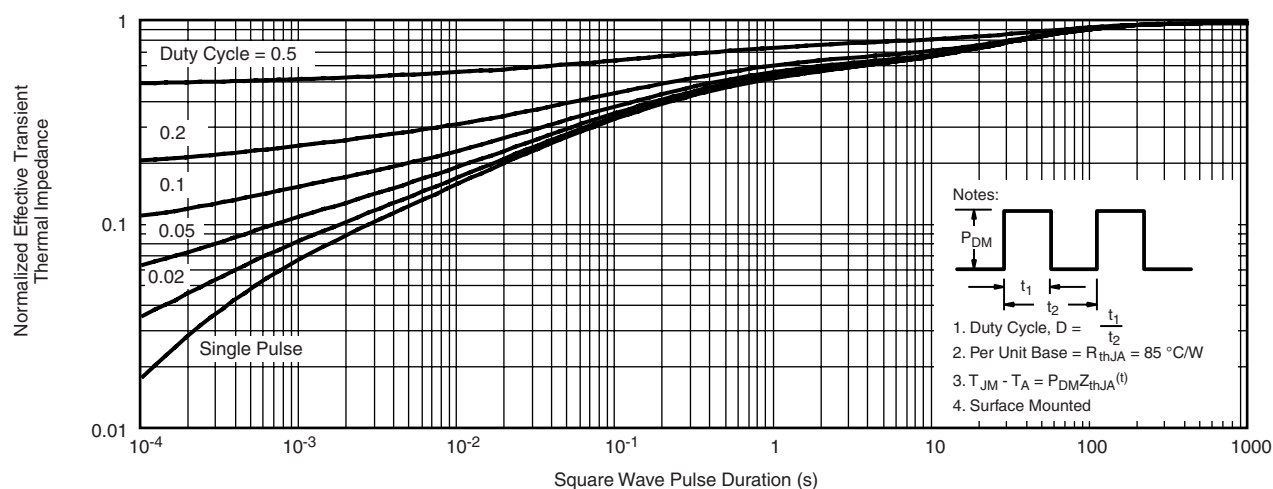
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

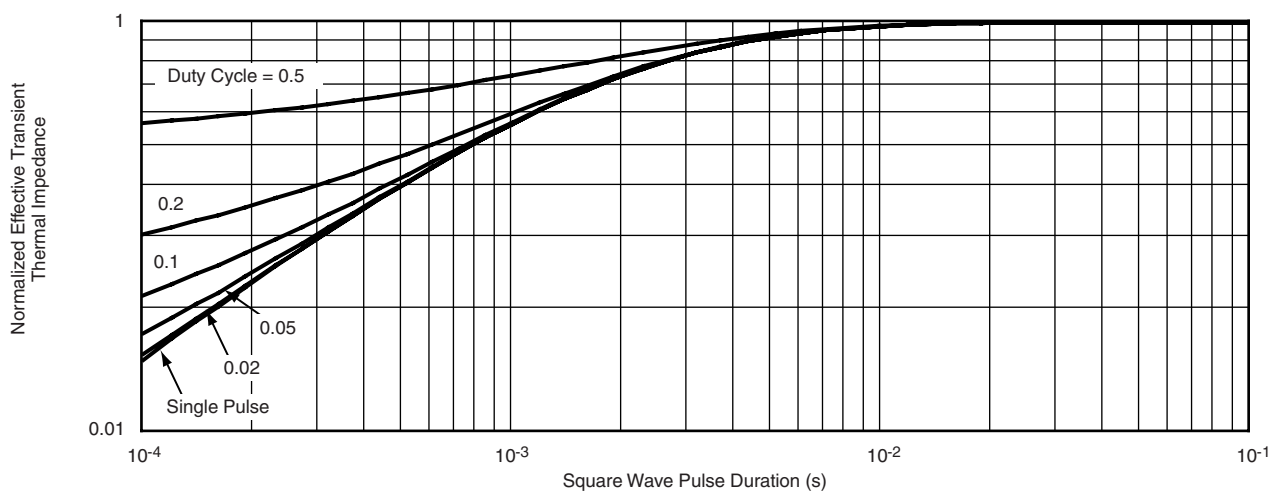
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Current Derating*

Power Derating

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

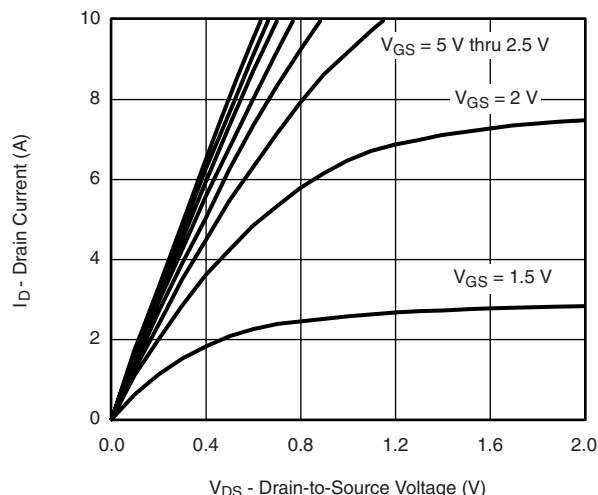
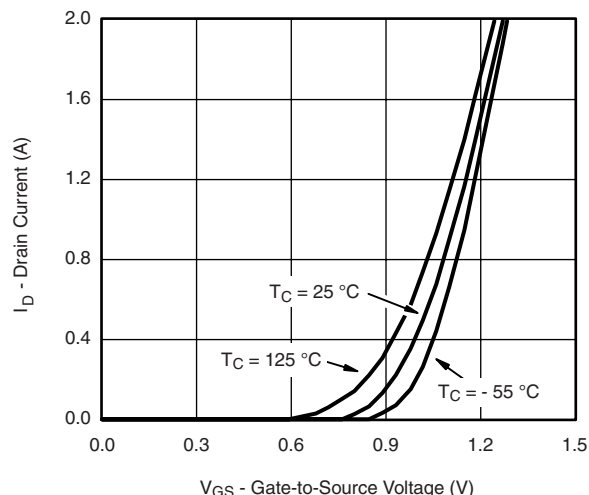
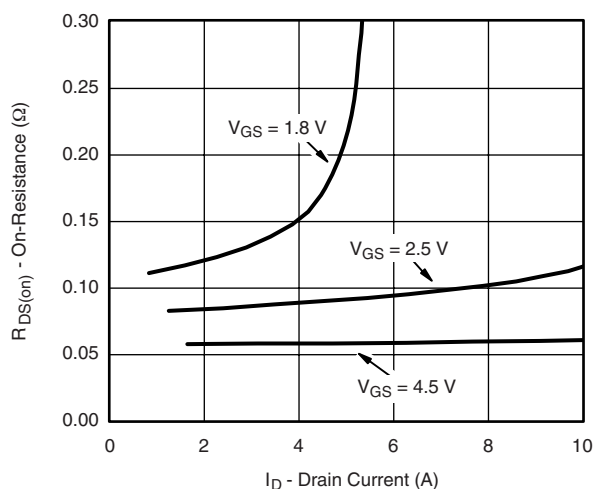
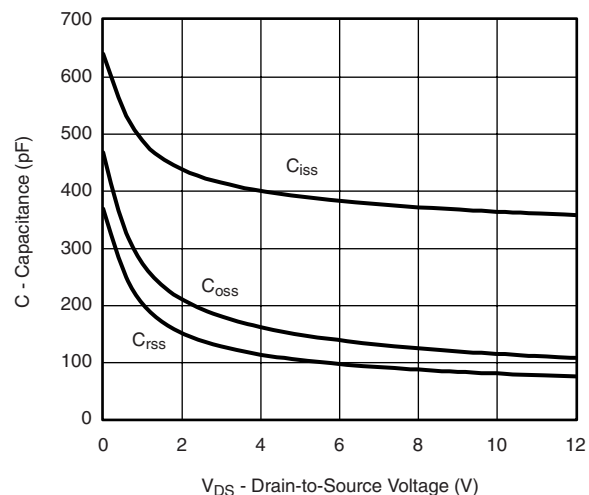
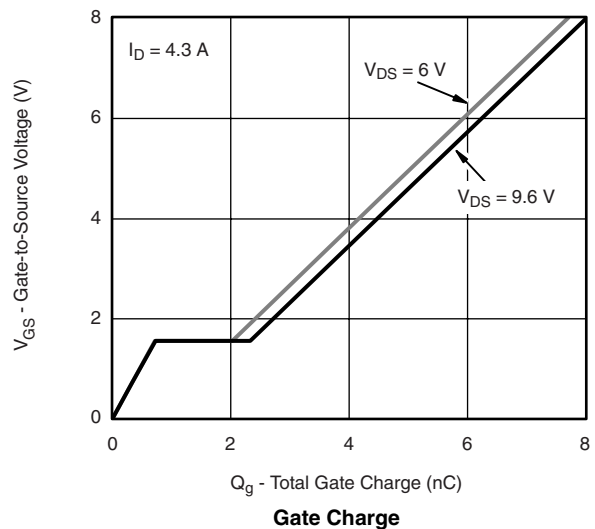
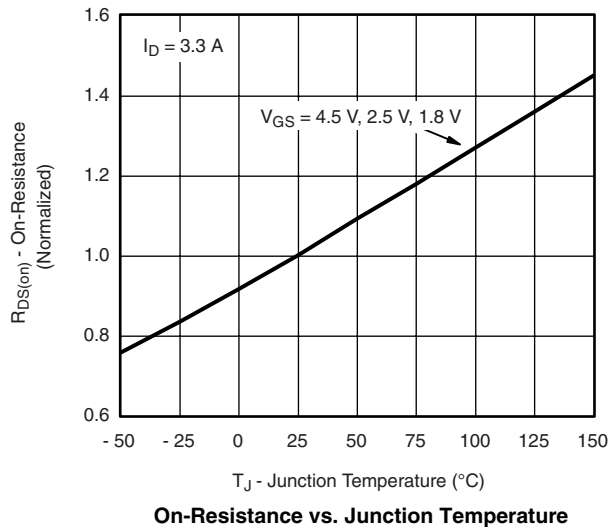
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



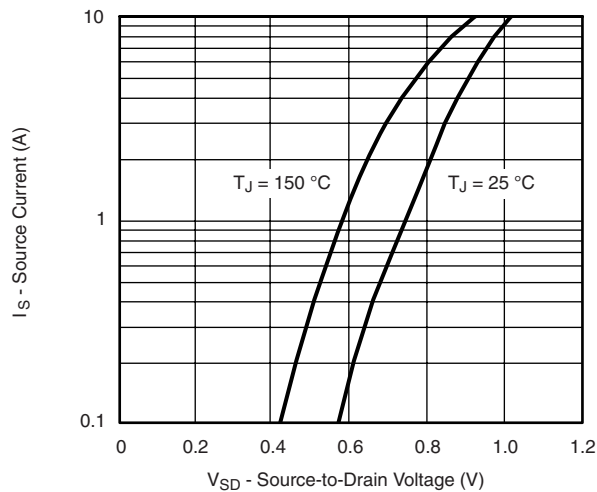
Normalized Thermal Transient Impedance, Junction-to-Ambient



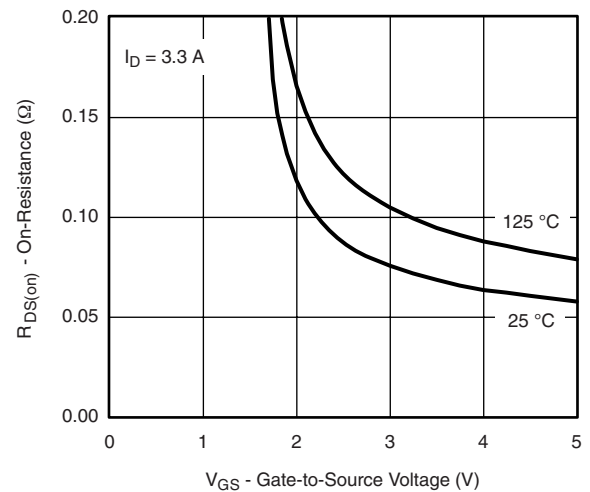
Normalized Thermal Transient Impedance, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

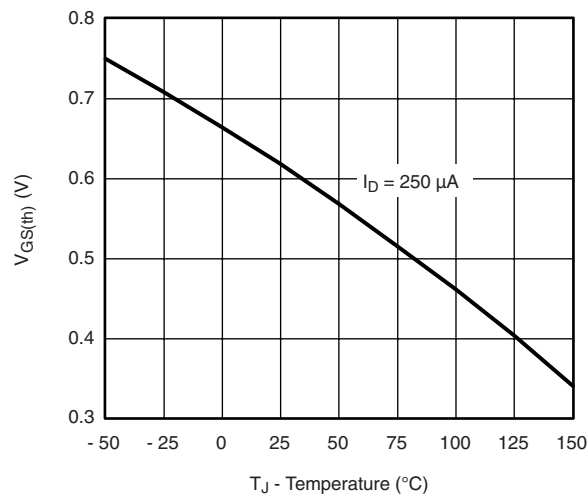
P-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



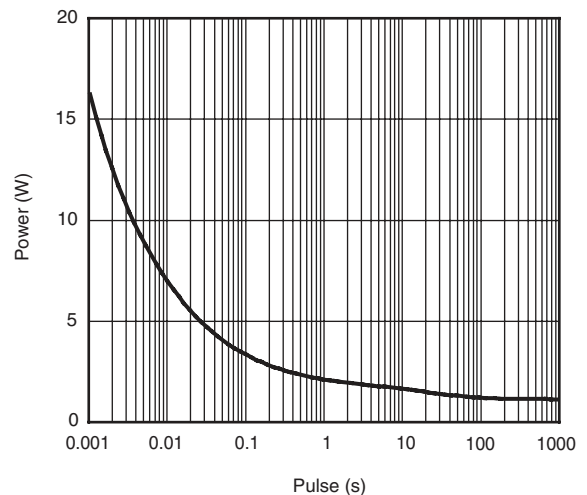
Source-Drain Diode Forward Voltage



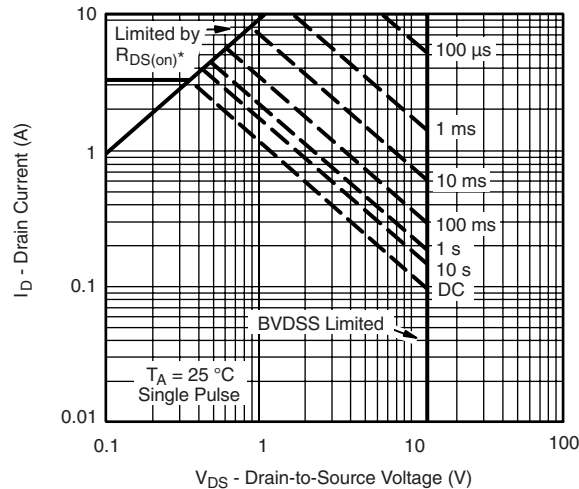
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

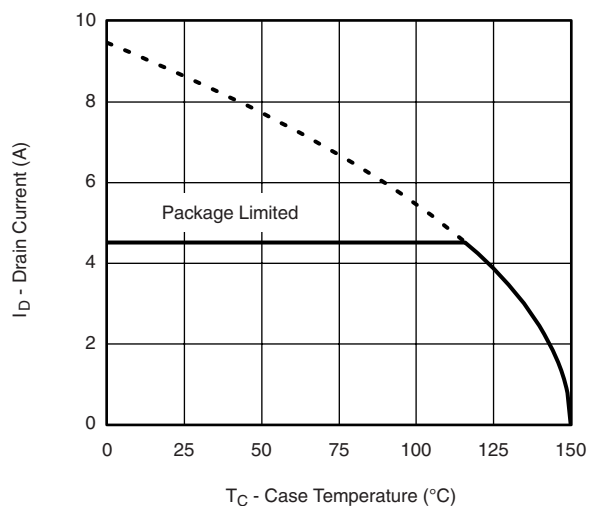
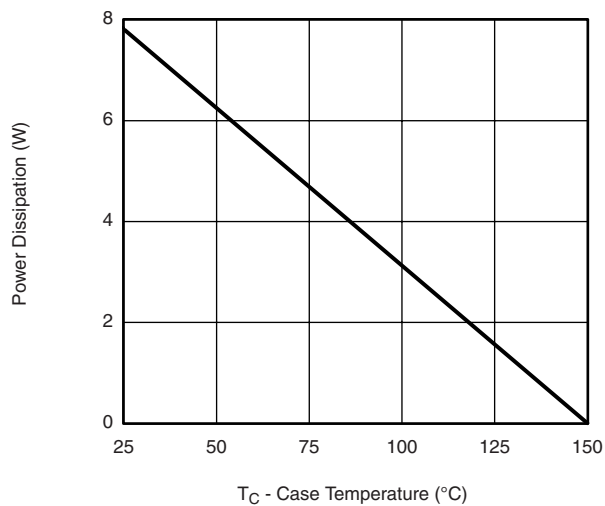


Single Pulse Power, Junction-to-Ambient



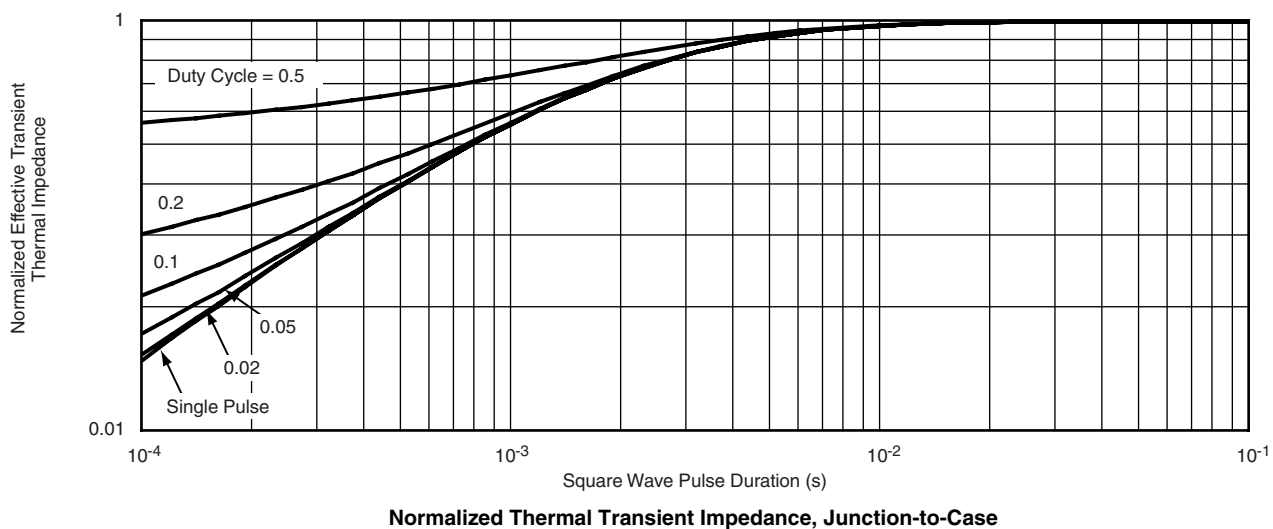
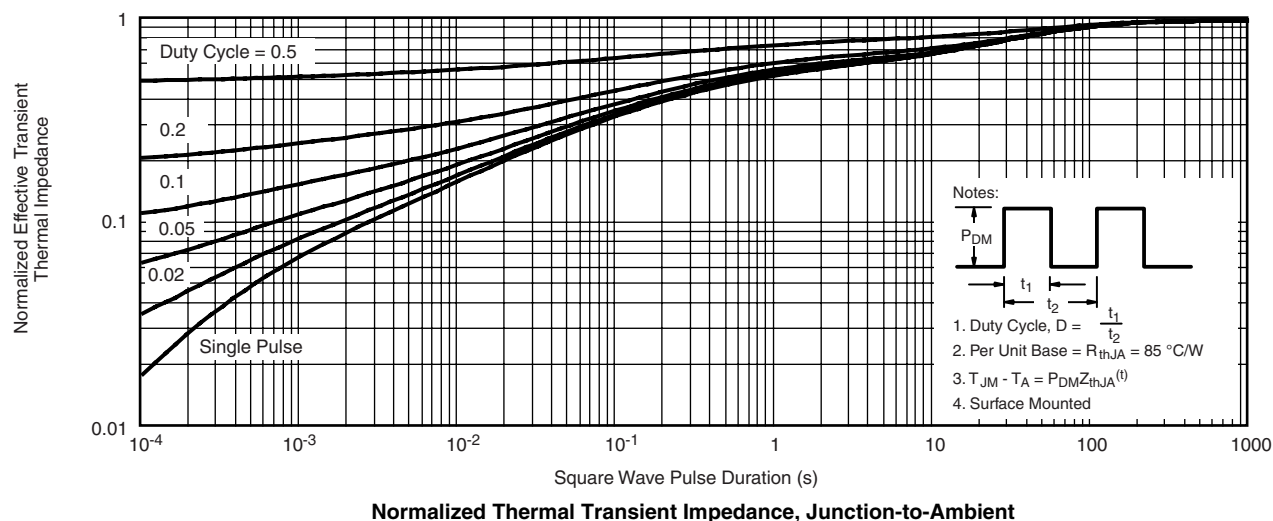
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Current Derating*

Power Derating

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

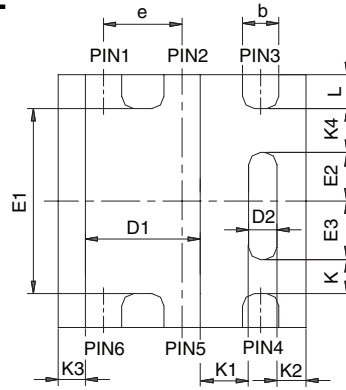
P-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



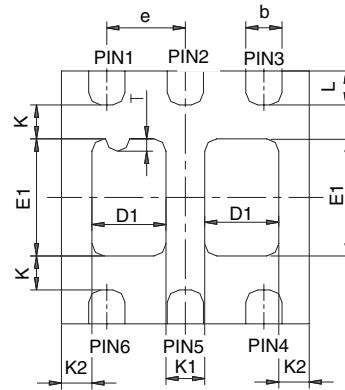
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65281.



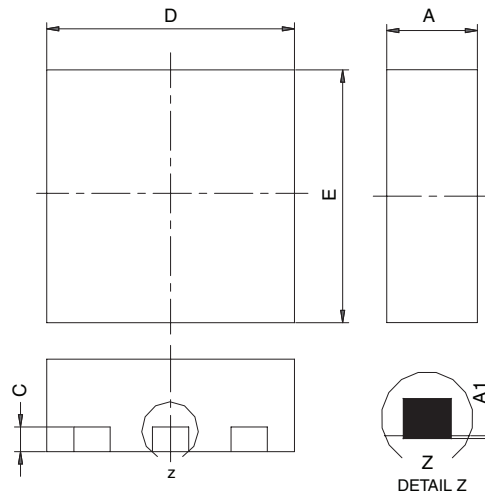
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

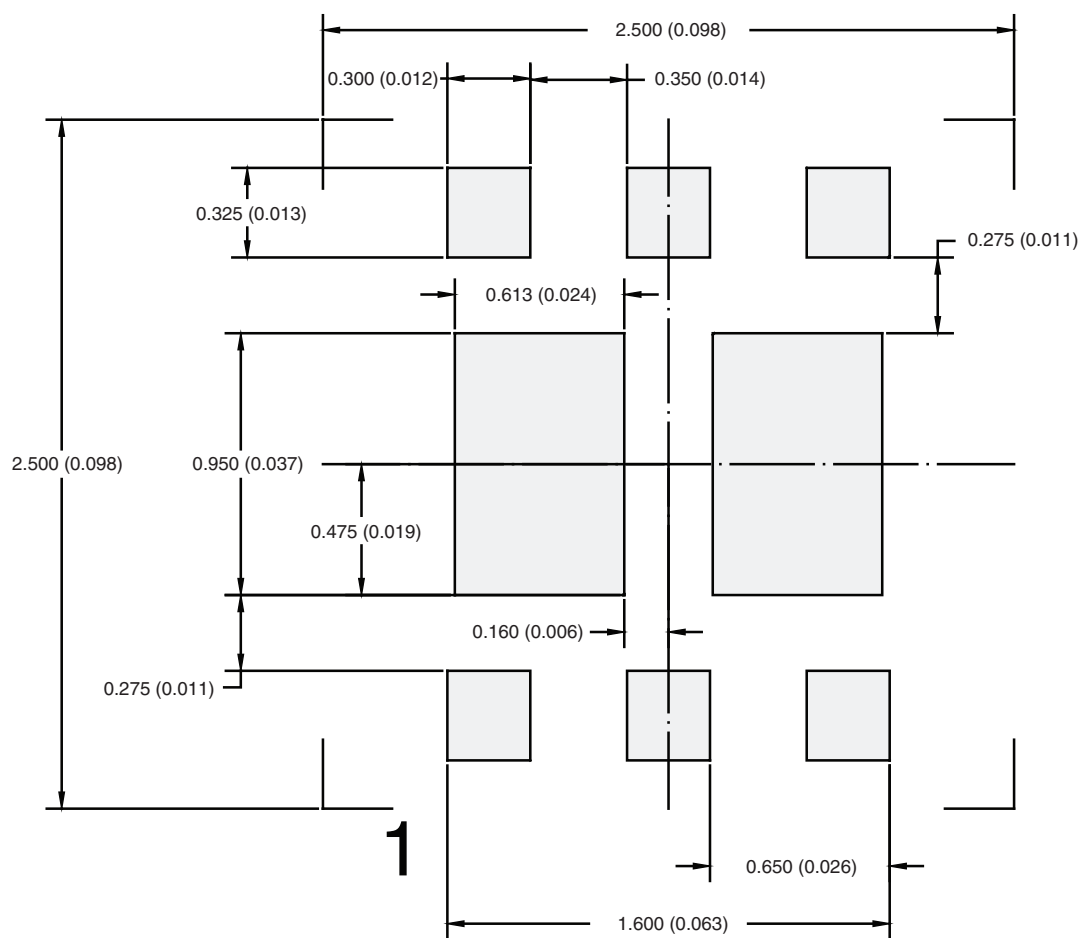


Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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