

FEATURES

- 9-bit ideal for byte-parity applications
- 3-state TTL outputs
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 6.0ns max. delay into 50pF, 12ns into 200pF (all outputs switching)
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with MC10H/100H603
- Available in 28-pin PLCC package

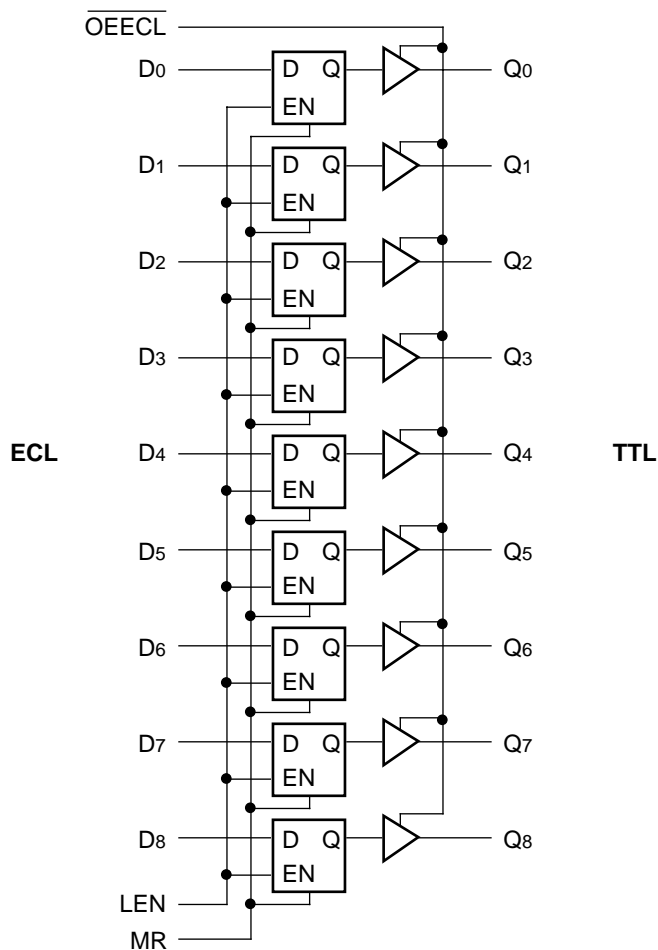
DESCRIPTION

The SY10/100H603 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Micrel 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. Latching is controlled by Latch Enable (LEN) and Master Reset (MR) resets the latches. A HIGH on \overline{OEECL} sends the outputs into the high impedance state. All control inputs are ECL level.

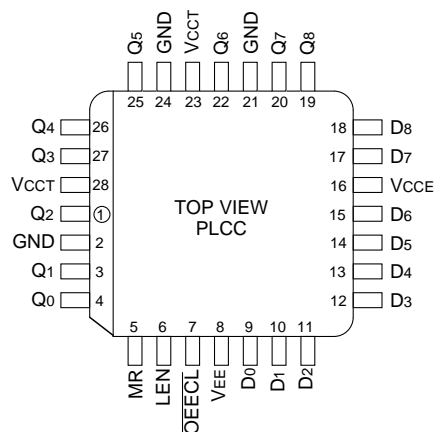
The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCCE	ECL Vcc (0V)
VCCT	TTL Supply (+5.0V)
VEE	ECL Supply (-5.2/-4.5V)
D0-D8	Data Inputs (ECL)
Q0-Q8	Data Outputs (TTL)
\overline{OEECL}	3-state Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

PACKAGE/ORDERING INFORMATION**28-Pin PLCC (J28-1)****Ordering Information⁽¹⁾**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10H603JC	J28-1	Commercial	SY10H603JC	Sn-Pb
SY10H603JCTR ⁽²⁾	J28-1	Commercial	SY10H603JC	Sn-Pb
SY100H603JC	J28-1	Commercial	SY100H603JC	Sn-Pb
SY100H603JCTR ⁽²⁾	J28-1	Commercial	SY100H603JC	Sn-Pb
SY10H603JZ ⁽³⁾	J28-1	Commercial	SY10H603JZ with Pb-Free bar-line indicator	Matte-Sn
SY10H603JZTR ^(2, 3)	J28-1	Commercial	SY10H603JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H603JZ ⁽³⁾	J28-1	Commercial	SY100H603JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H603JZTR ^(2, 3)	J28-1	Commercial	SY100H603JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

D	LEN	MR	\overline{OECL}	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q ₀
X	X	H	L	L
X	X	X	H	Z

DC ELECTRICAL CHARACTERISTICS

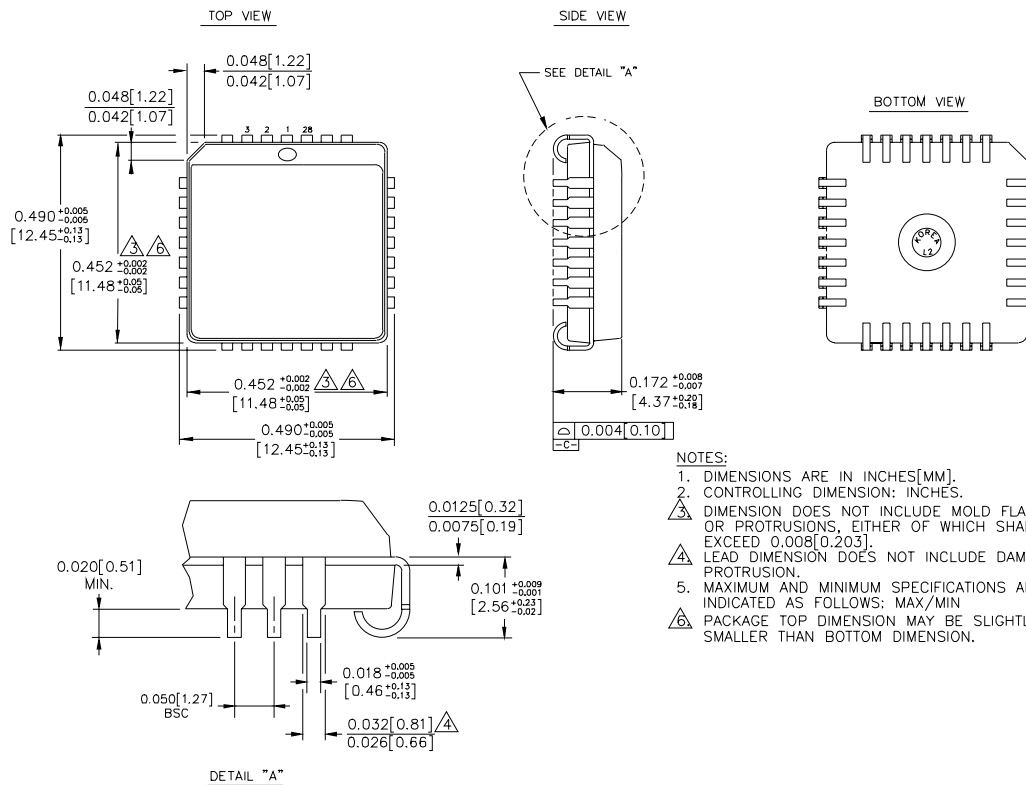
V_{CC}T = 5.0V ± 10%; V_{EE} = -4.75V to -5.5V (10H Version); V_{EE} = -4.2V to -5.5V (100H Version)

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{EE}	Power Supply Current, ECL	45	63	45	64	45	68	mA	—
I _{CC}	Power Supply Current, TTL	80	110	80	110	80	110	mA	—
I _{OS}	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	V _{OUT} = 0V
I _{OZH}	Output Disable Current, HIGH	—	50	—	50	—	50	μA	V _{OUT} = 2.7V
I _{OZL}	Output Disable Current, LOW	—	-50	—	-50	—	-50	μA	V _{OUT} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CC}T = 5.0V ± 10%; V_{EE} = -4.75V to -5.5V (10H Version); V_{EE} = -4.2V to -5.5V (100H Version)

Symbol	Parameter		T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t _{PD}	Propagation Delay to Output	D	3.2 6.4	6.0 12	3.2 6.4	6.0 12	3.2 6.4	6.0 12	ns	C _L = 50pF C _L = 200pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns	C _L = 50pF C _L = 200pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns	C _L = 50pF C _L = 200pF
t _S	Set-up Time, D to LEN		1.5	—	1.5	—	1.5	—	ns	—
t _H	Hold Time, D to LEN		0.8	—	0.8	—	0.8	—	ns	—
t _w ^(L)	LEN Pulse Width, LOW		2.0	—	2.0	—	2.0	—	ns	—
t _{PLZ} t _{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns	C _L = 50pF C _L = 200pF
t _{PZL} t _{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns	C _L = 50pF C _L = 200pF
t _r t _f	Output Rise/Fall Time 1.0V – 2.0V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns	C _L = 50pF C _L = 200pF

28-PIN PLCC (J28-1)

Rev. 03

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