



STL22NF10

N-CHANNEL 100V - 0.065Ω - 22A PowerFLAT™ LOW GATE CHARGE STripFET™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL22NF10	100 V	< 0.070 Ω	22 A

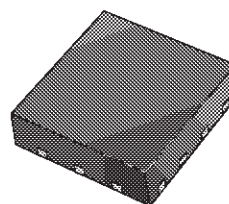
- TYPICAL R_{DS(on)} = 0.065Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

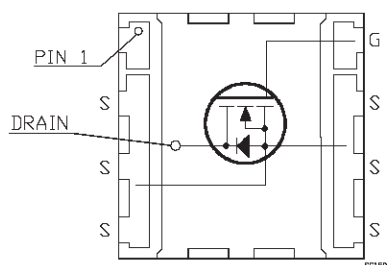
APPLICATIONS

- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT



**PowerFLAT™ (5x5)
(Chip Scale Package)**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C Drain Current (continuous) at T _C = 100°C	22 14	A A
I _{DM} (●)	Drain Current (pulsed)	88	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
	Derating Factor	0.56	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	9	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	240	mJ
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 22A, di/dt ≤ 300A/μs, V_{DD} ≤ V(BR)DSS, T_j ≤ T_{JMAX}.
(2) Starting T_j = 25°C, I_D = 11A, V_{DD} = 30V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.8	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Condition s	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Condition s	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 11 A		0.065	0.070	Ω

DYNAMIC

Symbol	Parameter	Test Condition s	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 11 A		10		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		870		pF
C _{oss}	Output Capacitance			125		pF
C _{rss}	Reverse Transfer Capacitance			52		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 11\text{ A}$		58		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		45		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$, $I_D = 22\text{ A}$,		30	40	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		6		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 11\text{ A}$,		49		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		17		ns
$t_{d(off)}$	Off-Voltage Rise Time	$V_{clamp} = 80\text{ V}$, $I_D = 22\text{ A}$,		43		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$		21		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		39		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				22	A
$I_{SDM} (1)$	Source-drain Current (pulsed)				88	A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 22\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 22\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		100		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 30\text{ V}$, $T_j = 150^\circ\text{C}$		375		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		7.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

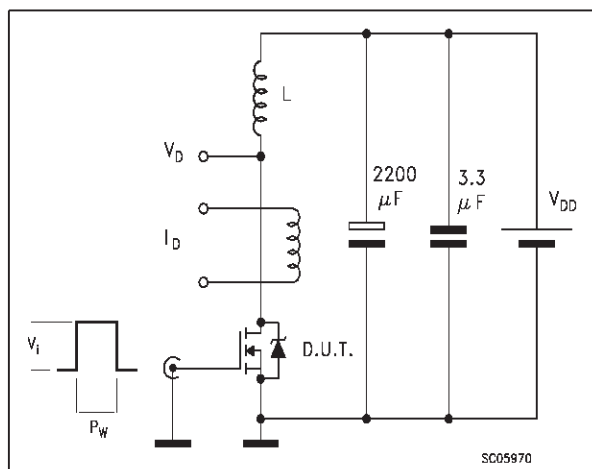


Fig. 2: Unclamped Inductive Waveform

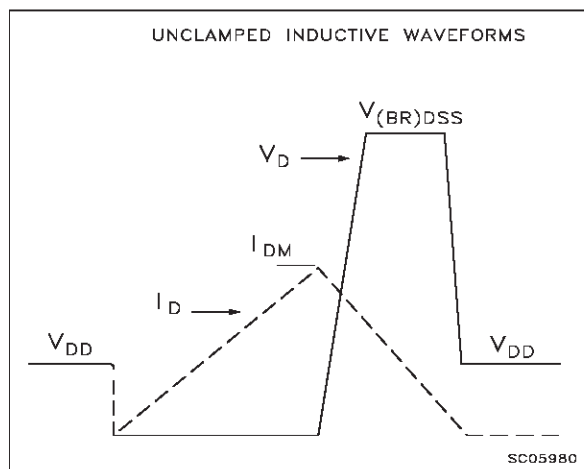


Fig. 3: Switching Times Test Circuit For Resistive Load

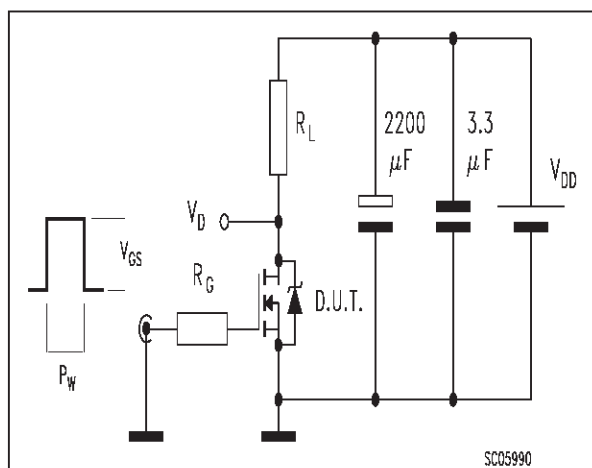


Fig. 4: Gate Charge test Circuit

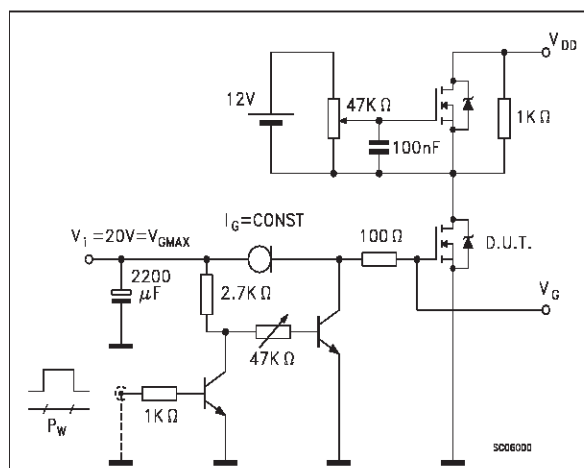
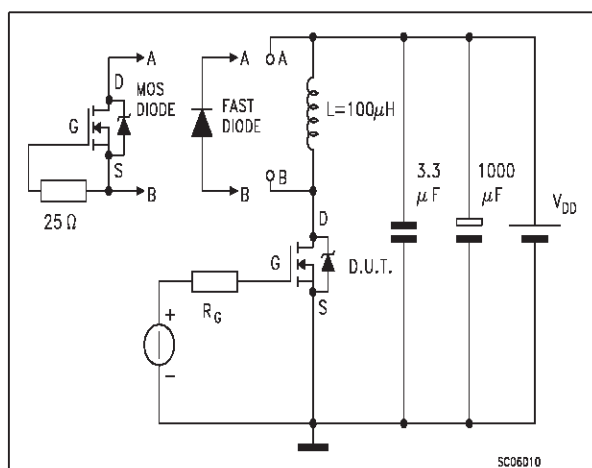
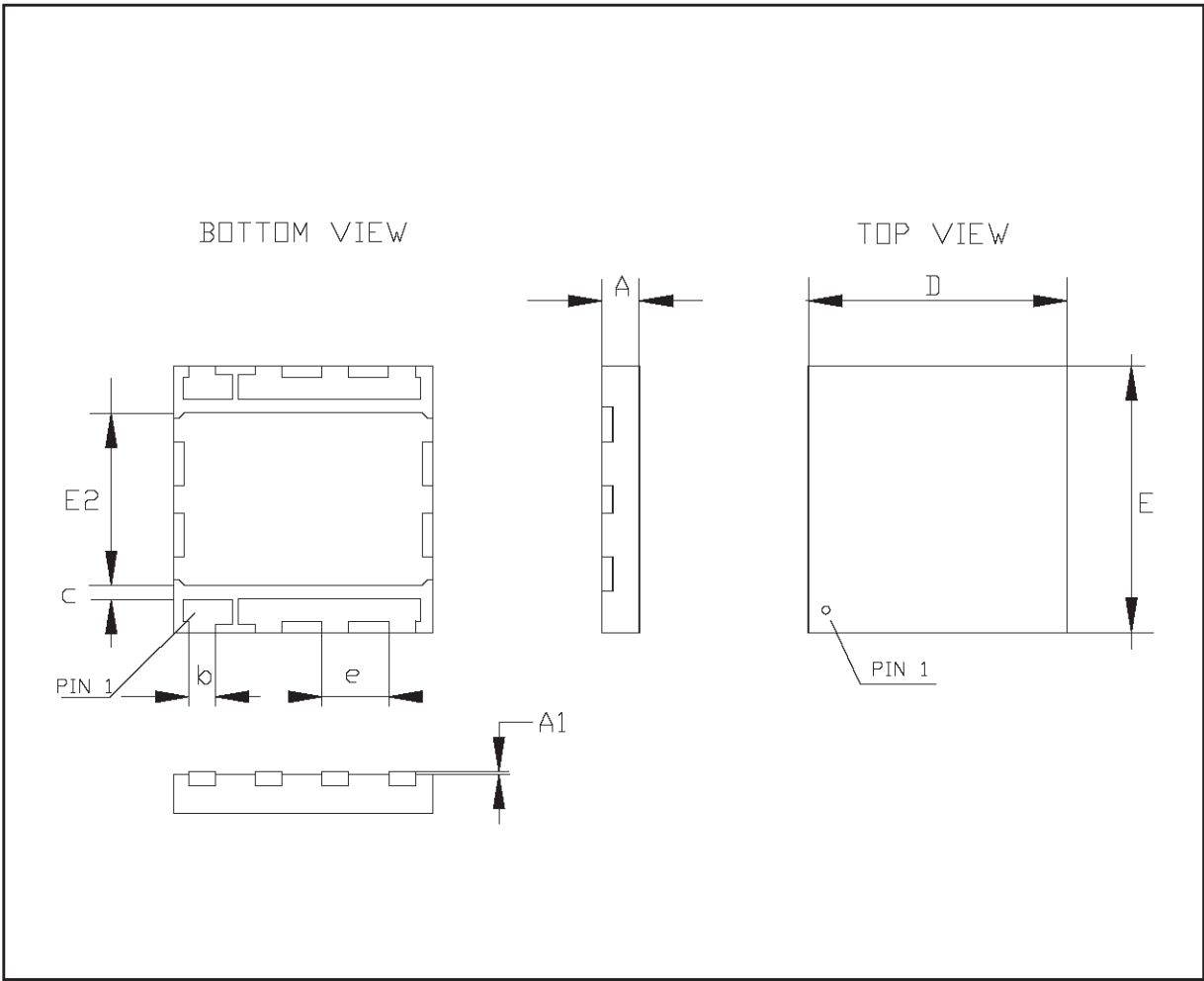


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerFLAT™(5x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
e		1.27			0.050	



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