



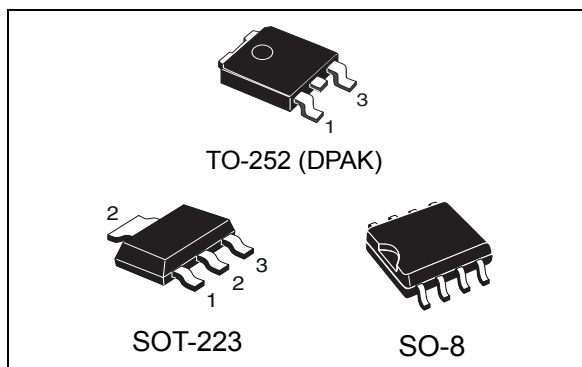
VND1NV04 VNN1NV04 - VNS1NV04

OMNIFET II
fully autoprotected Power MOSFET

Features

Parameter	Symbol	Value
Max on-state resistance (per ch.)	R_{ON}	250 m Ω
Current limitation (typ)	I_{LIMH}	1.7 A
Drain-source clamp voltage	V_{CLAMP}	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



Description

The VND1NV04, VNN1NV04, VNS1NV04 are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes			
	Tube	Tube (lead free)	Tape and reel	Tape and reel (lead free)
TO-252 (DPAK)	VND1NV04	VND1NV04-E	VND1NV04TR	VND1NV04TR-E
SOT-223	VNN1NV04	-	VNN1NV04TR	-
SO-8	VNS1NV04	-	VNS1NV04TR	-

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1 Block diagram and pin description

Figure 1. Block diagram

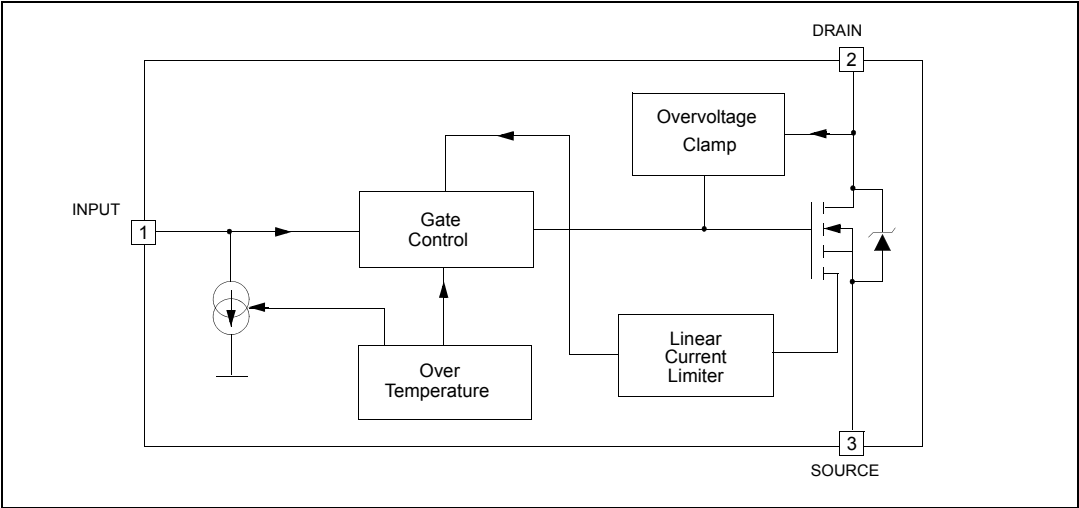
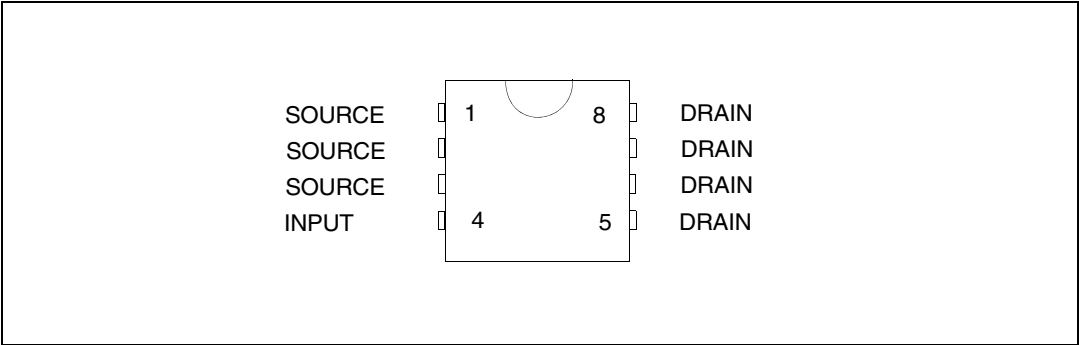


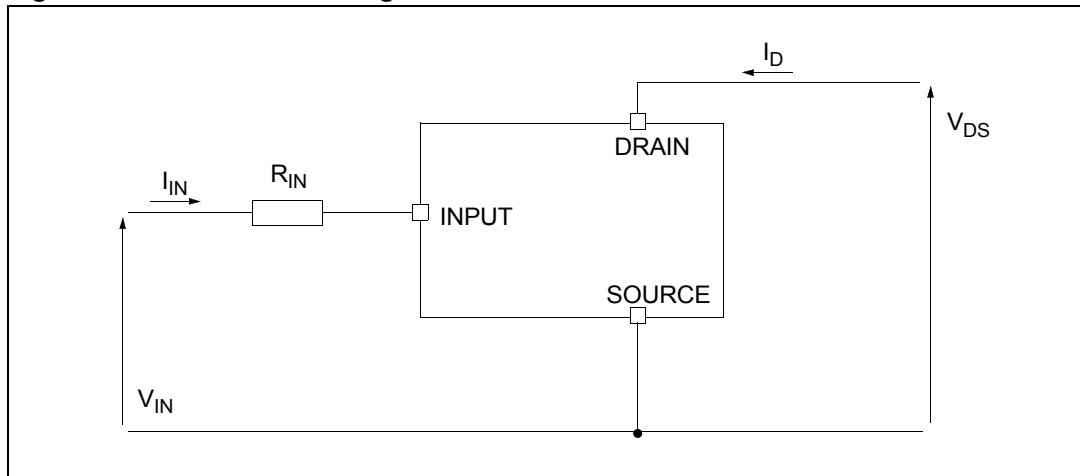
Figure 2. Configuration diagram (top view) (a)



a. For the pins configuration related to SOT-223 and DPAK see outline at page 1.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		SOT-223	SO-8	DPAK	
V_{DSn}	Drain-source voltage ($V_{INn}=0$ V)	Internally clamped			V
V_{INn}	Input voltage	Internally clamped			V
I_{INn}	Input current	+/-20			mA
$R_{IN\ MINn}$	Minimum input series impedance	330			Ω
I_{Dn}	Drain current	Internally limited			A
I_{Rn}	Reverse DC output current	-3			A
V_{ESD1}	Electrostatic discharge ($R=1.5$ K Ω , $C=100$ pF)	4000			V
V_{ESD2}	Electrostatic discharge on output pins only ($R=330$ Ω , $C=150$ pF)	16500			V
P_{tot}	Total dissipation at $T_c=25$ °C	7	8.3	35	W
T_j	Operating junction temperature	Internally limited			°C
T_c	Case operating temperature	Internally limited			°C
T_{stg}	Storage temperature	-55 to 150			°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max value			Unit
		SOT-223	SO-8	DPAK	
$R_{thj-case}$	Thermal resistance junction-case	18		3.5	°C/W
$R_{thj-lead}$	Thermal resistance junction-lead		15		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	70 ⁽¹⁾	65 ⁽¹⁾	54 ⁽¹⁾	°C/W

1. When mounted on a standard single-sided FR4 board with 50 mm² of Cu (at least 35 µm thick) connected to all DRAIN pins

2.3 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off (-40 °C<T_j<150 °C, unless otherwise specified)						
V_{CLAMP}	Drain-source clamp voltage	$V_{IN}=0\text{ V}; I_D=0.5\text{ A}$	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{IN}=0\text{ V}; I_D=2\text{ mA}$	36			V
V_{INTH}	Input threshold voltage	$V_{DS}=V_{IN}; I_D=1\text{ mA}$	0.5		2.5	V
I_{ISS}	Supply current from input pin	$V_{DS}=0\text{ V}; V_{IN}=5\text{ V}$		100	150	µA
V_{INCL}	Input-source clamp voltage	$I_{IN}=1\text{ mA}$ $I_{IN}=-1\text{ mA}$	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero input voltage drain current ($V_{IN}=0\text{ V}$)	$V_{DS}=13\text{ V}; V_{IN}=0\text{ V}; T_j=25\text{ °C}$ $V_{DS}=25\text{ V}; V_{IN}=0\text{ V}$			30 75	µA
On (-40 °C<T_j<150 °C, unless otherwise specified)						
$R_{DS(on)}$	Static drain-source on resistance	$V_{IN}=5\text{ V}; I_D=0.5\text{ A}; T_j=25\text{ °C}$ $V_{IN}=5\text{ V}; I_D=0.5\text{ A}$			250 500	mΩ
Dynamic (T_j=25 °C, unless otherwise specified)						
$g_{fs}^{(1)}$	Forward transconductance	$V_{DD}=13\text{ V}; I_D=0.5\text{ A}$		2		S
C_{OSS}	Output capacitance	$V_{DS}=13\text{ V}; f=1\text{ MHz}; V_{IN}=0\text{ V}$		90		pF
Switching (T_j=25 °C, unless otherwise specified)						

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} =15 V; I _D =0.5 A V _{gen} =5 V; R _{gen} =R _{IN MIN} =330 Ω (see Figure 4)		70	200	ns
t _r	Rise time			170	500	ns
t _{d(off)}	Turn-off delay time			350	1000	ns
t _f	Fall time			200	600	ns
t _{d(on)}	Turn-on delay time	V _{DD} =15 V; I _D =0.5 A V _{gen} =5 V; R _{gen} =2.2 KΩ (see Figure 4)		0.25	1.0	μs
t _r	Rise time			1.3	4.0	μs
t _{d(off)}	Turn-off delay time			1.8	5.5	μs
t _f	Fall time			1.2	4.0	μs
(dl/dt) _{on}	Turn-on current slope	V _{DD} =15 V; I _D =1.5 A V _{gen} =5 V; R _{gen} =R _{IN MIN} =330 Ω		5		A/μs
Q _i	Total input charge	V _{DD} =12 V; I _D =0.5 A; V _{IN} =5 V I _{gen} =2.13 mA (see Figure 7)		5		nC
Source drain diode (T _J =25 °C, unless otherwise specified)						
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} =0.5 A; V _{IN} =0 V		0.8		V
t _{rr}	Reverse recovery time	I _{SD} =0.5 A; dl/dt=6 A/μs V _{DD} =30 V; L=200 μH (see Figure 5)		205		ns
Q _{rr}	Reverse recovery charge			100		nC
I _{RRM}	Reverse recovery current			0.7		A
Protections (-40 °C<T _J <150 °C, unless otherwise specified)						
I _{lim}	Drain current limit	V _{IN} =5 V; V _{DS} =13 V	1.7		3.5	A
t _{dlim}	Step response current limit	V _{IN} =5 V; V _{DS} =13 V		2.0		μs
T _{jsh}	Over temperature shutdown		150	175	200	°C
T _{jrs}	Over temperature reset		135			°C
I _{gf}	Fault sink current	V _{IN} =5 V; V _{DS} =13 V; T _J =T _{jsh}	10	15	20	mA
E _{as}	Single pulse avalanche energy	Starting T _J =25 °C; V _{DD} =24 V V _{IN} =5 V R _{gen} =R _{IN MIN} =330 Ω; L=50 mH (see Figure 6 and Figure 8)	55			mJ

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

Figure 4. Switching time test circuit for resistive load

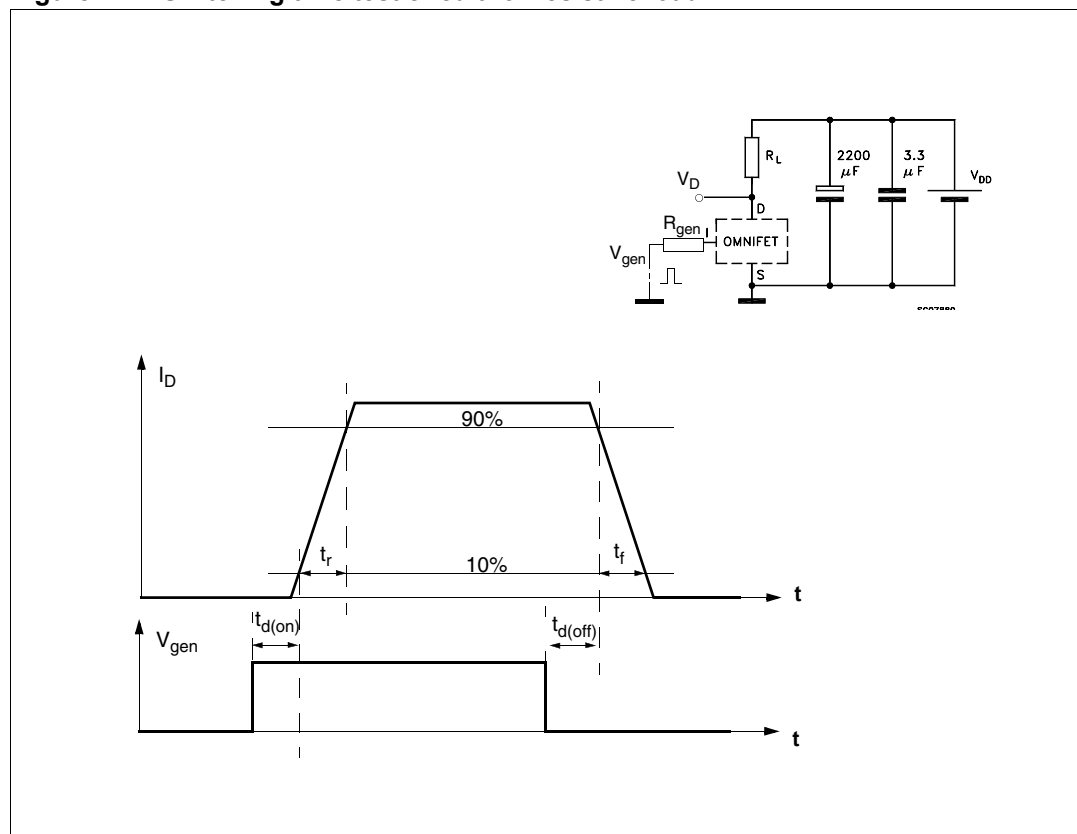


Figure 5. Test circuit for diode recovery times

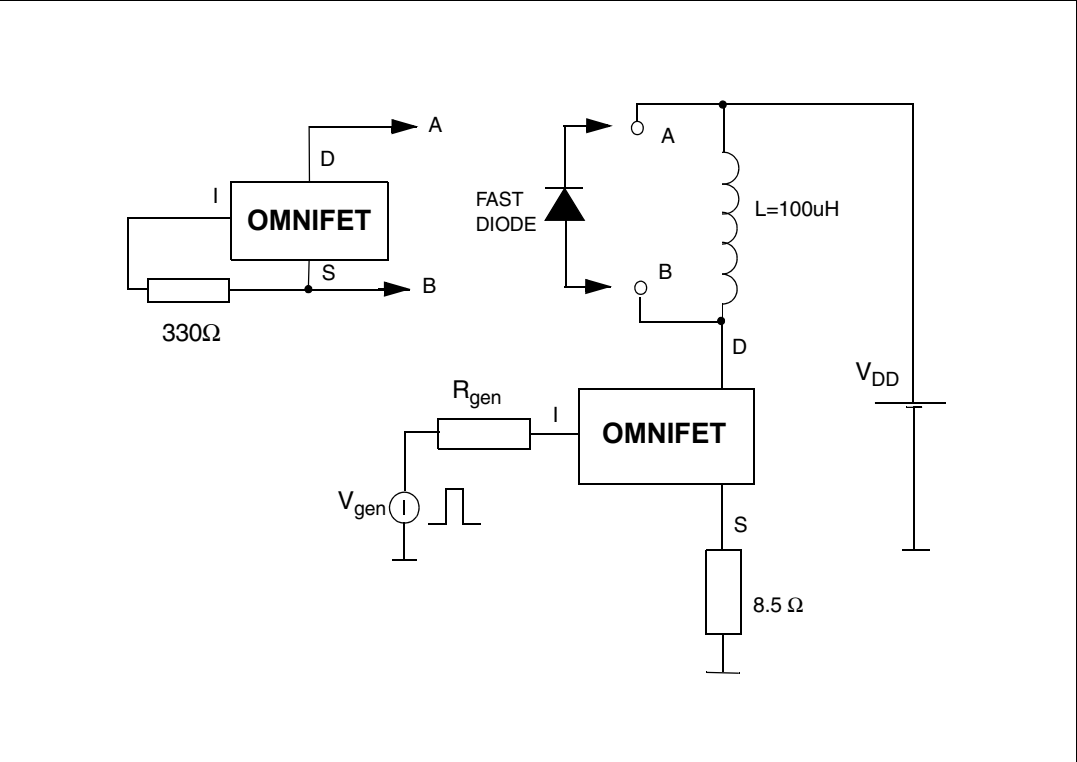


Figure 6. Unclamped inductive load test circuits

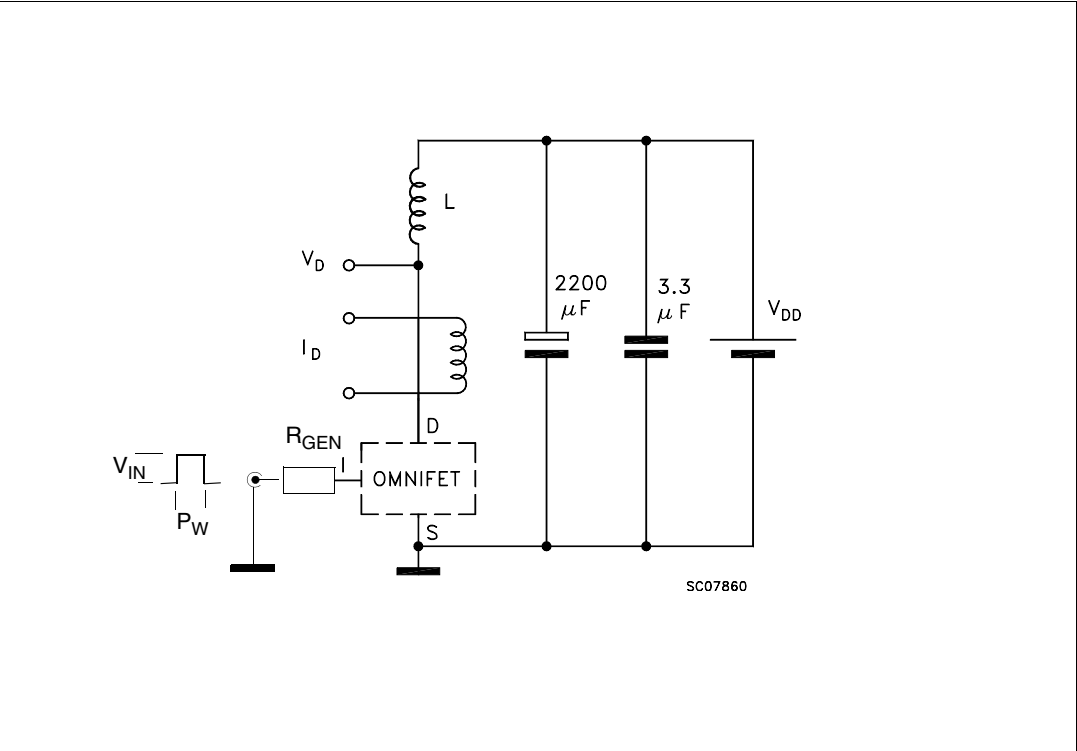


Figure 7. Input charge test circuit

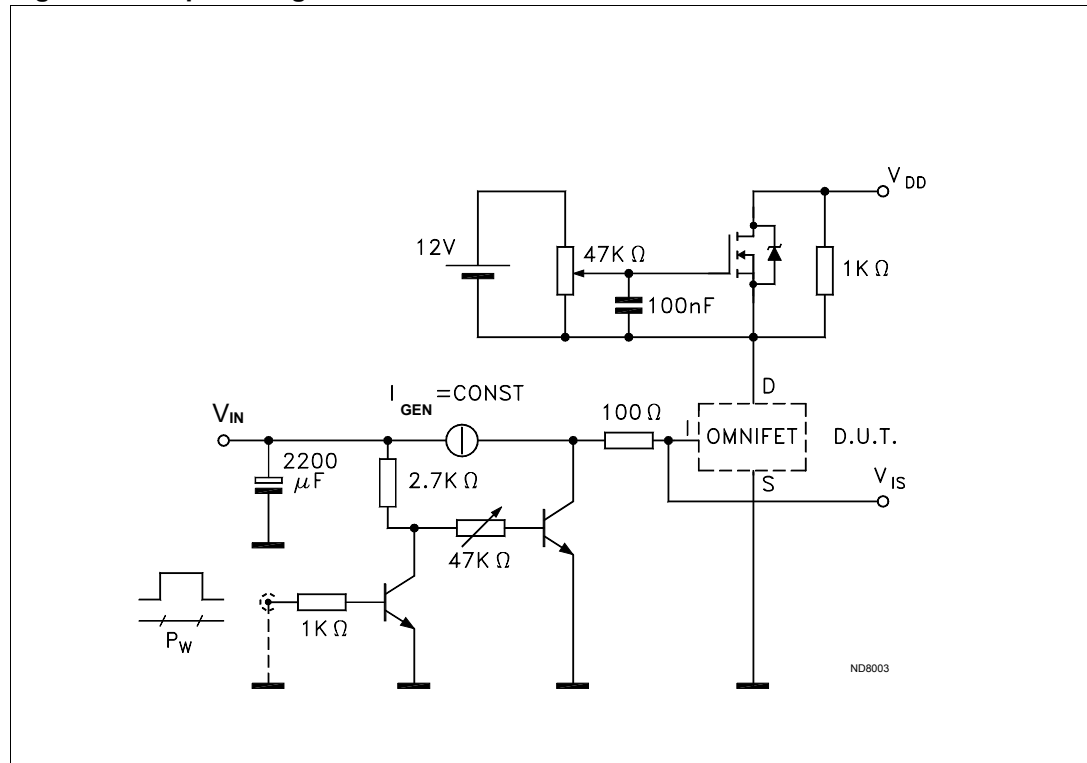
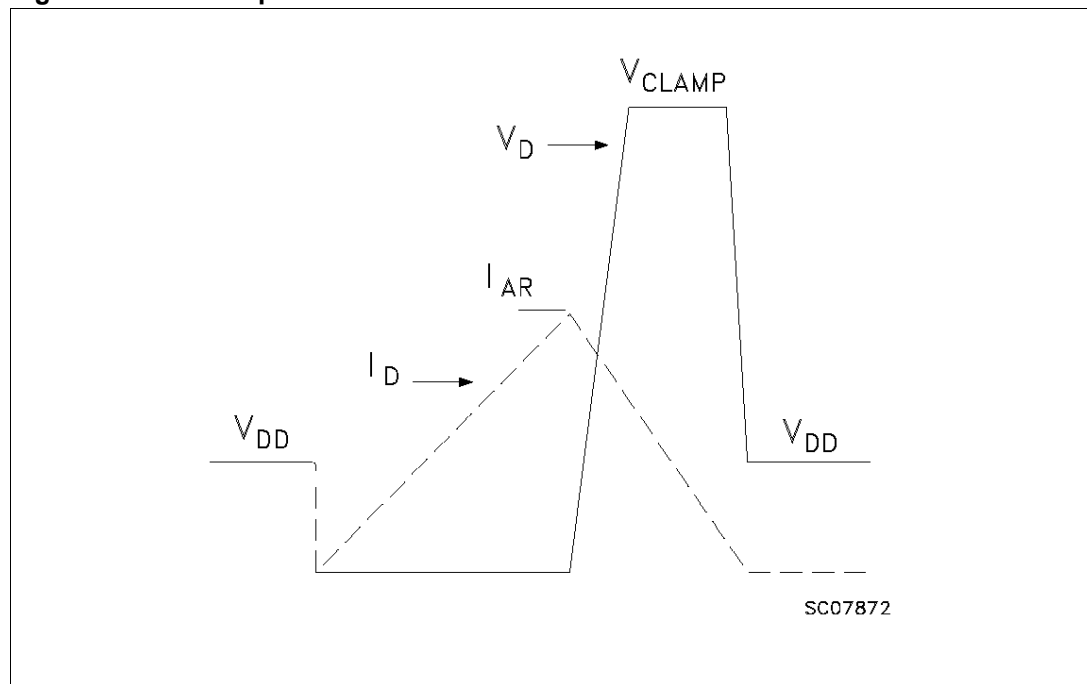


Figure 8. Unclamped inductive waveforms



2.4 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

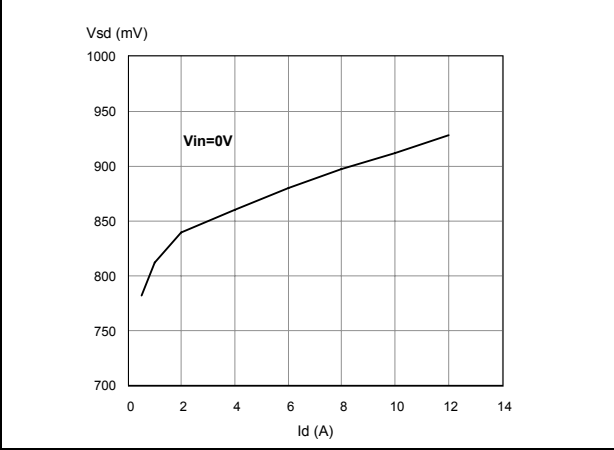


Figure 10. Static drain-source on resistance

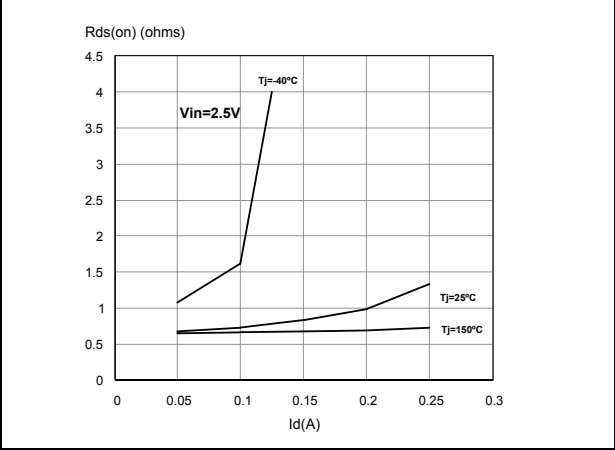


Figure 11. Derating curve

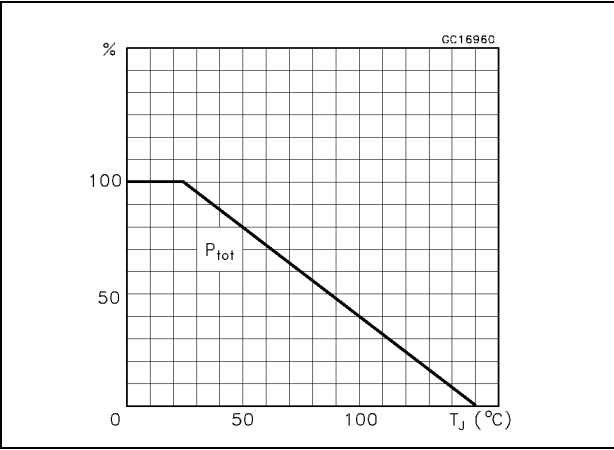


Figure 12. Static drain-source on resistance vs. input voltage (part 1/2)

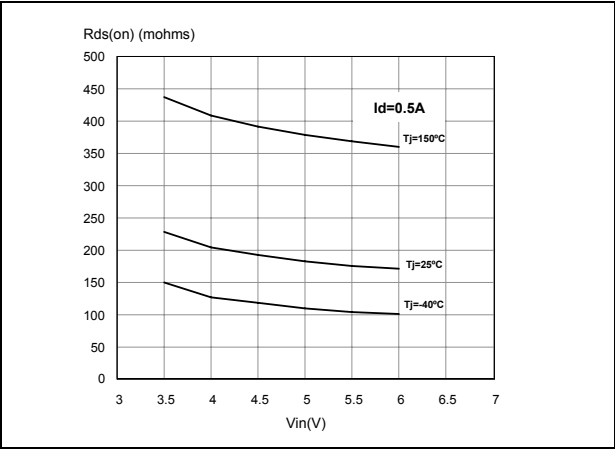


Figure 13. Static drain-source on resistance vs. input voltage (part 2/2)

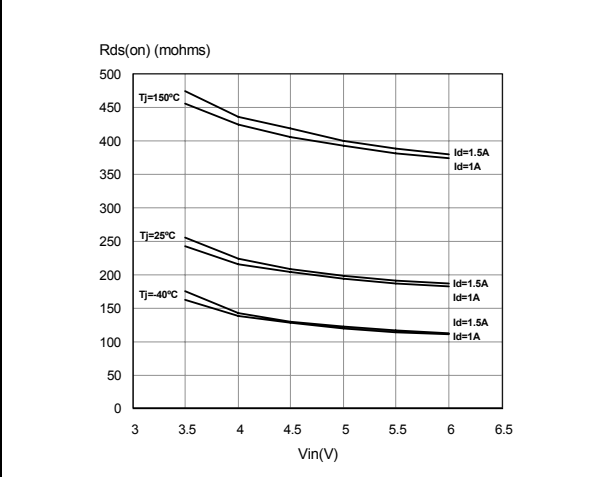


Figure 14. Transconductance

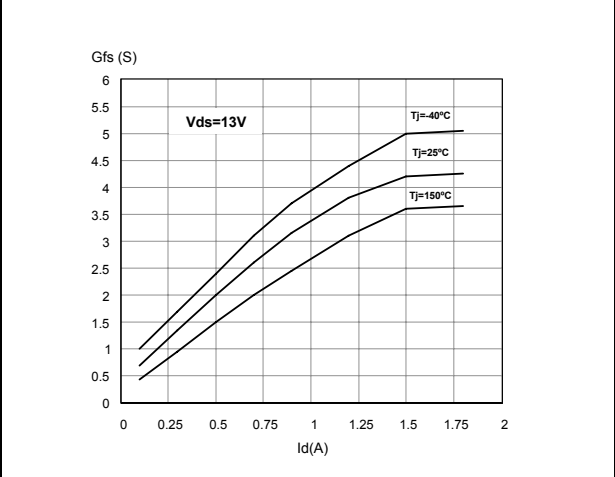


Figure 15. Static drain-source on resistance vs. Id

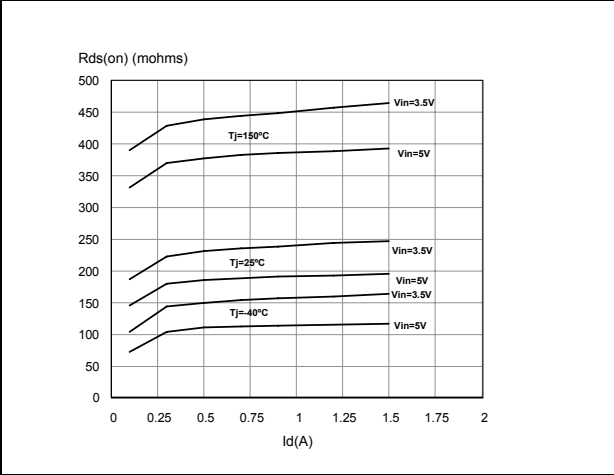


Figure 16. Transfer characteristics

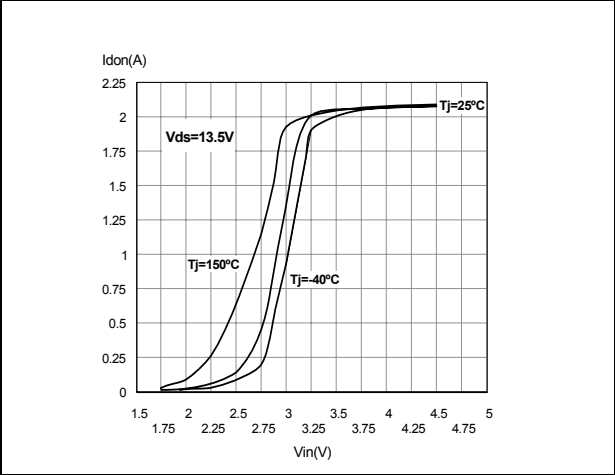


Figure 17. Turn-on current slope (part 1/2)

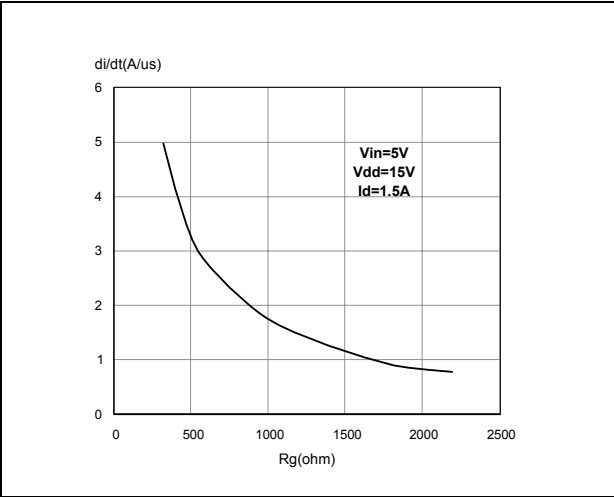


Figure 18. Turn-on current slope (part 2/2)

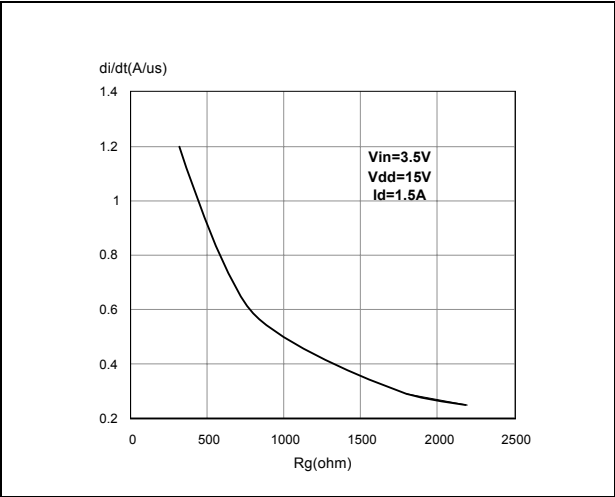


Figure 19. Input voltage vs. input charge

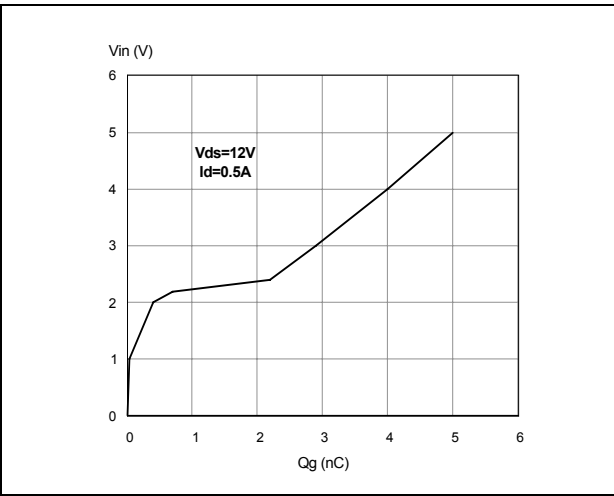


Figure 20. Turn-off drain source voltage slope (part 1/2)

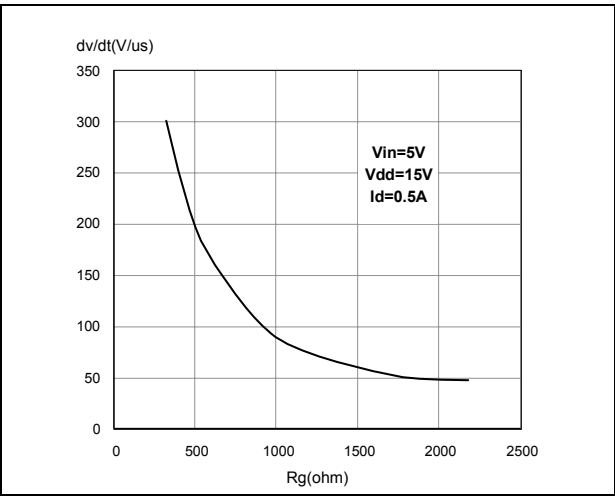


Figure 21. Turn-off drain-source voltage slope Figure 22. Capacitance variations
(part 2/2)

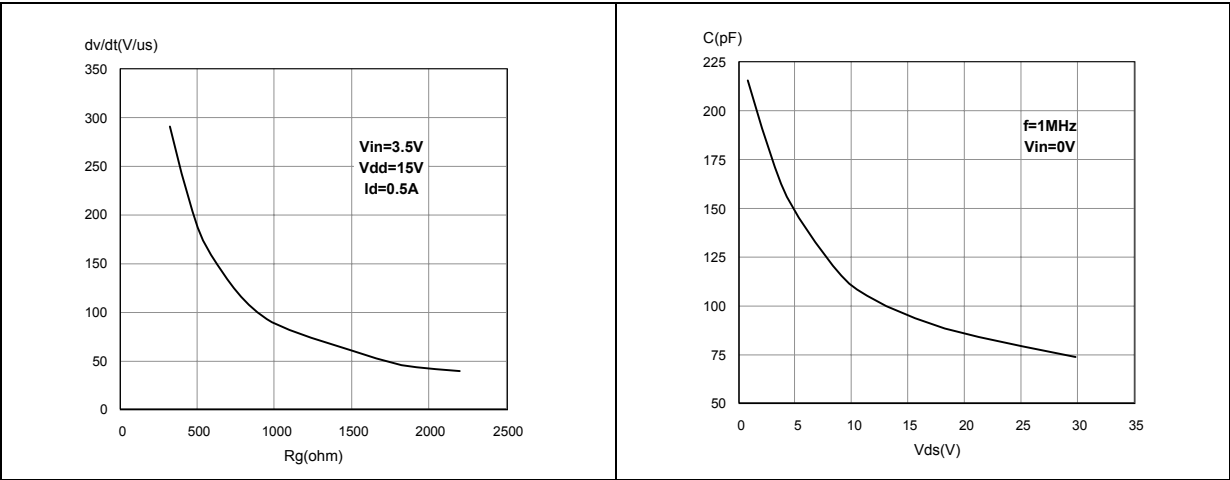


Figure 23. Switching time resistive load (part 1/2) Figure 24. Switching time resistive load (part 2/2)

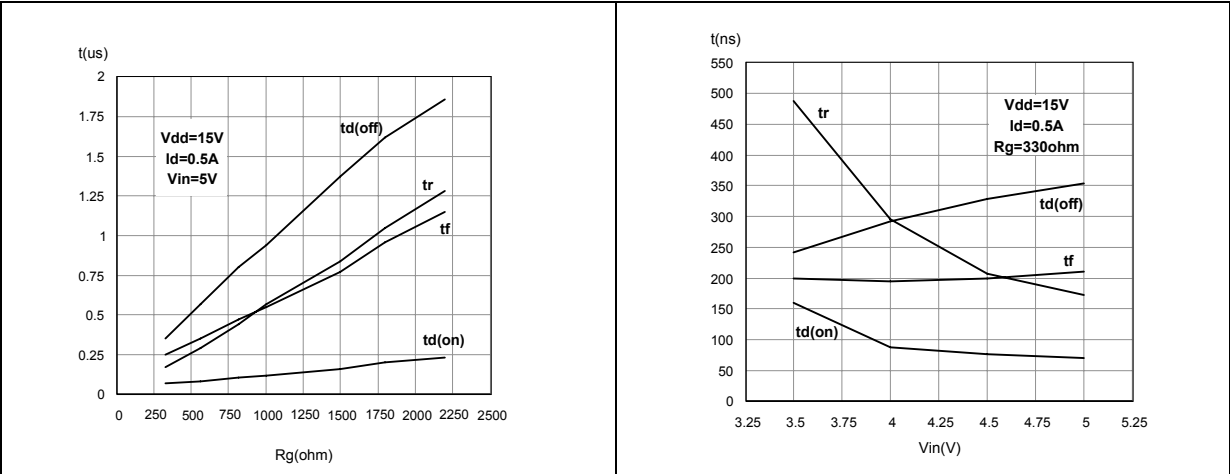


Figure 25. Output characteristics Figure 26. Normalized on resistance vs. temperature

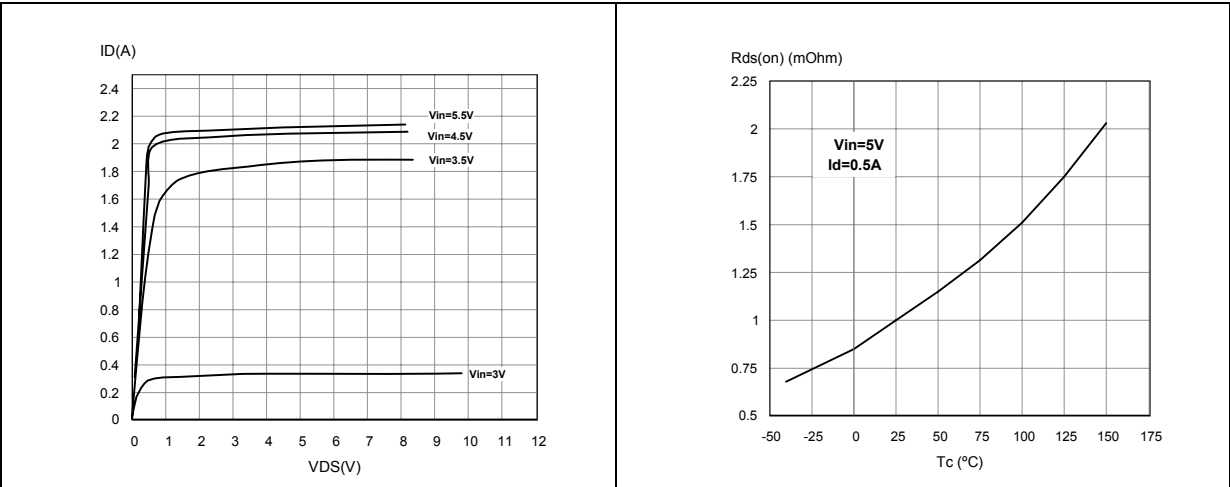


Figure 27. Normalized input threshold voltage vs. temperature

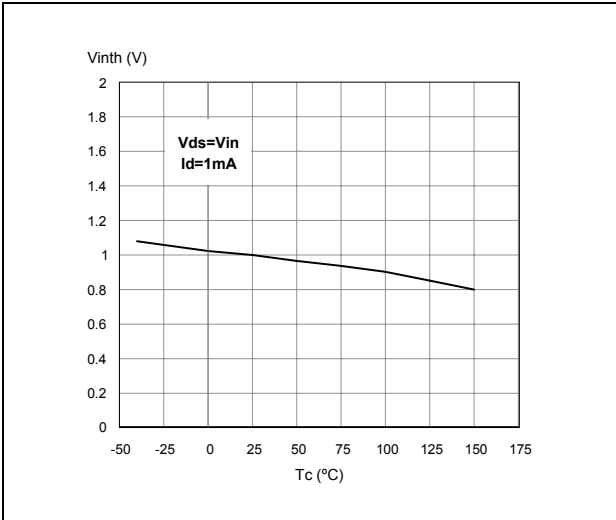


Figure 28. Normalized current limit vs. junction temperature

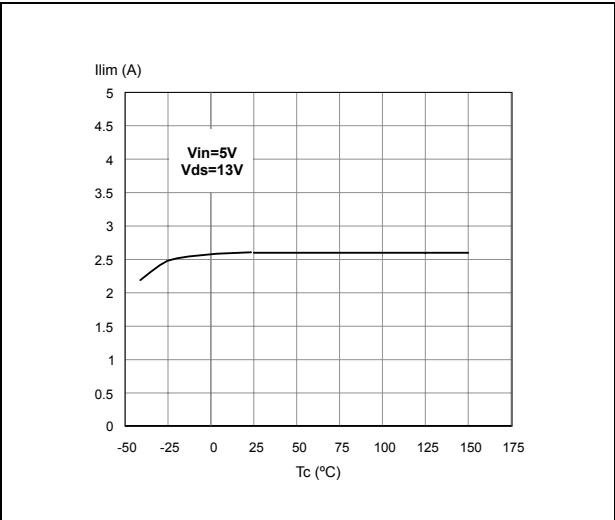
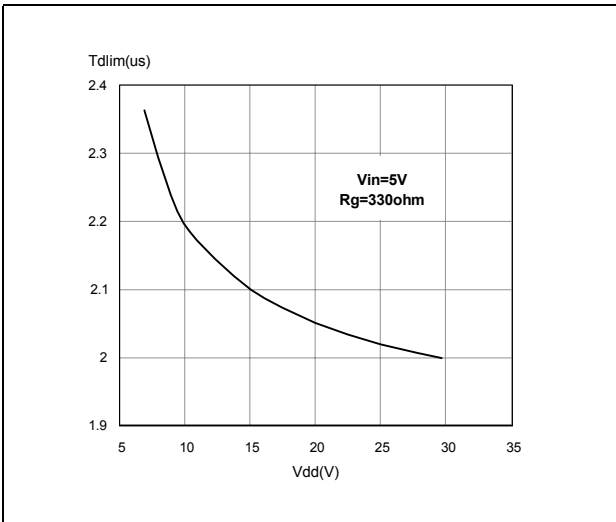


Figure 29. Step response current limit



3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

3.1 Overvoltage clamp protection

Internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

3.2 Linear current limiter circuit

Limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh} .

3.3 Over temperature and short circuit protection

These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.

3.4 Status feedback

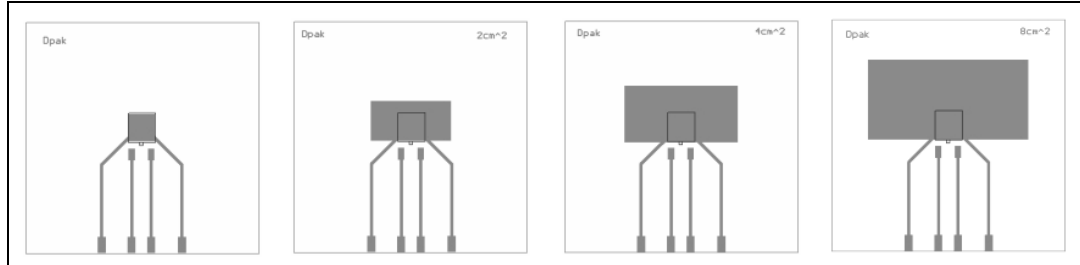
In the case of an over temperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf} , the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{SS} .

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

4 Package and PCB thermal data

4.1 DPAK thermal data

Figure 30. DPAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad layout to 16 cm²).

Figure 31. DPAK $R_{thi-amb}$ vs. PCB copper area in open box free air condition

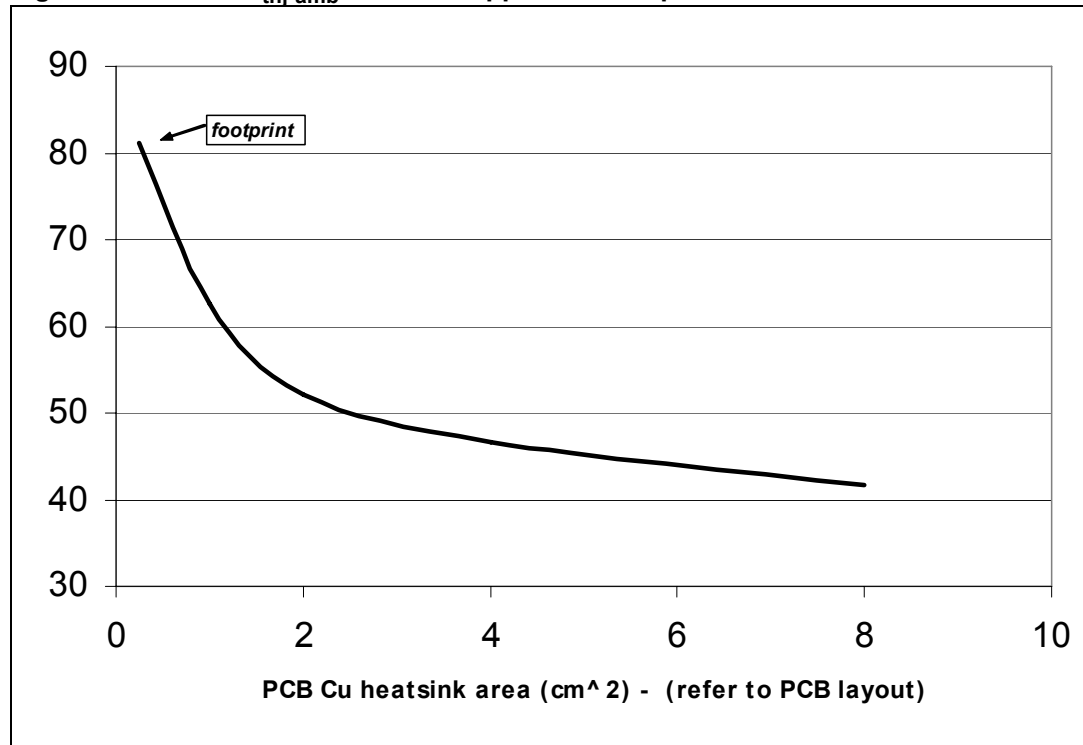
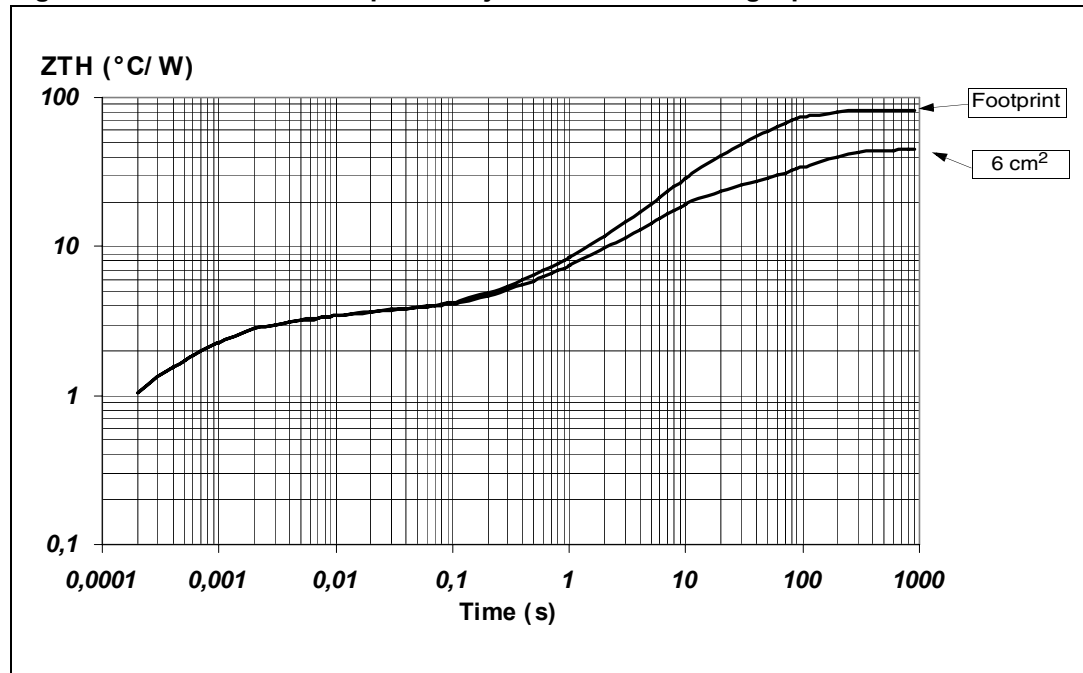


Figure 32. DPAK thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 33. DPAK thermal fitting model of a single channel

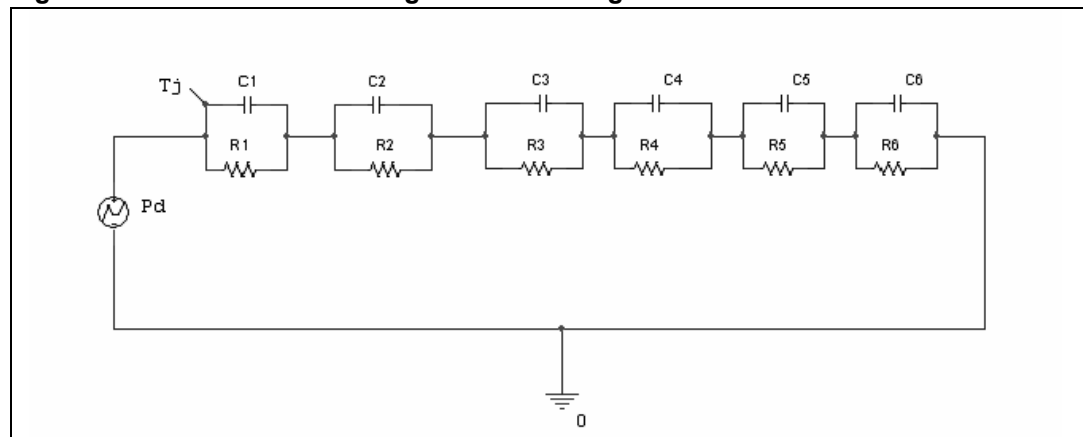
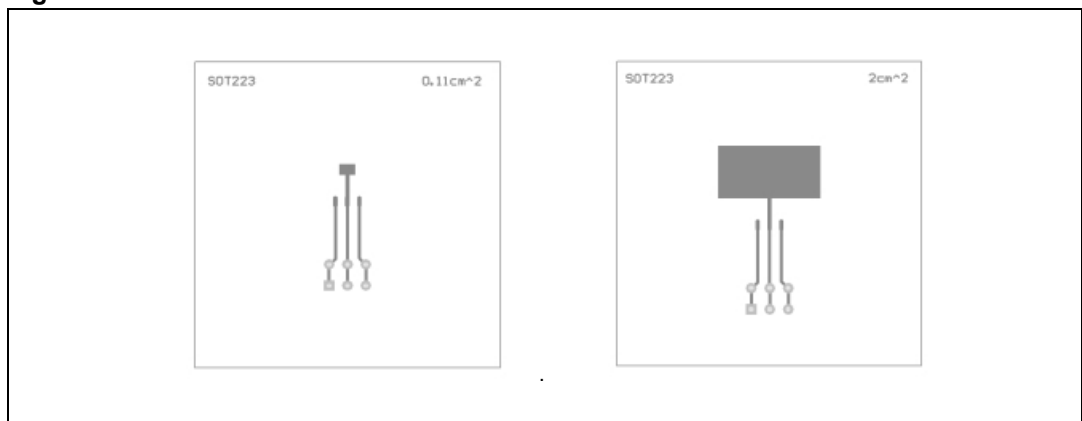


Table 5. DPAK thermal parameter

Area/island (cm ²)	0.25	6
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	0.8	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.01	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4.2 SOT-223 thermal data

Figure 34. SOT-223 PC board

1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness=35 μ m , Copper areas: from minimum pad layout to 0.8 cm²).

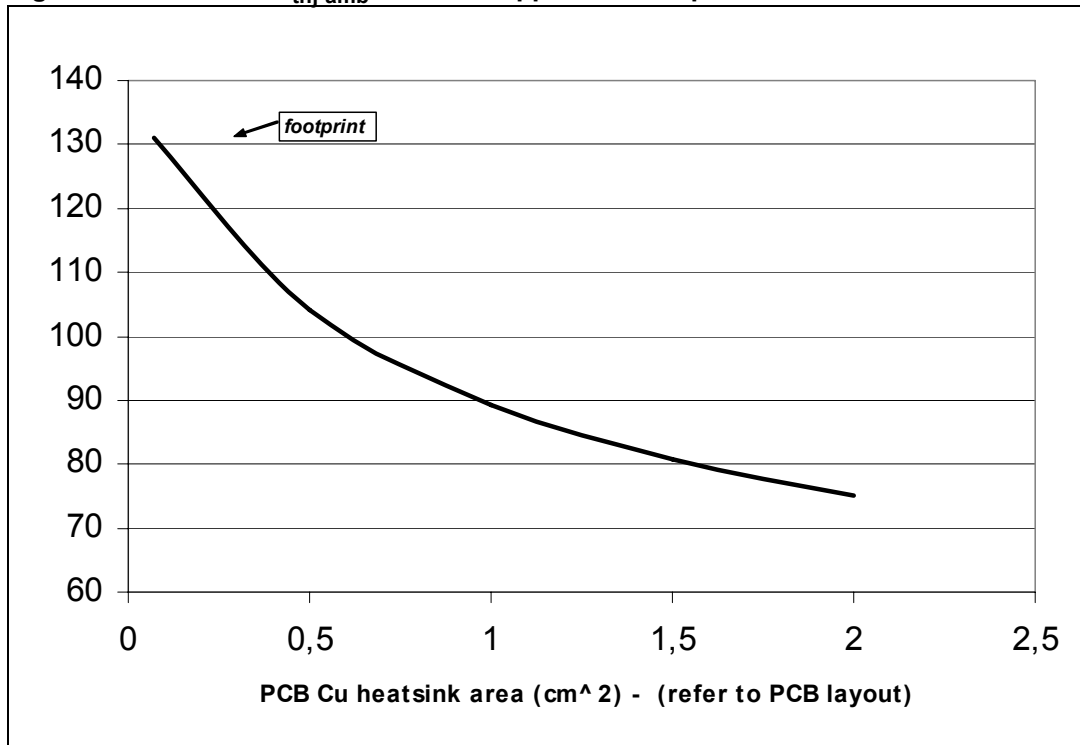
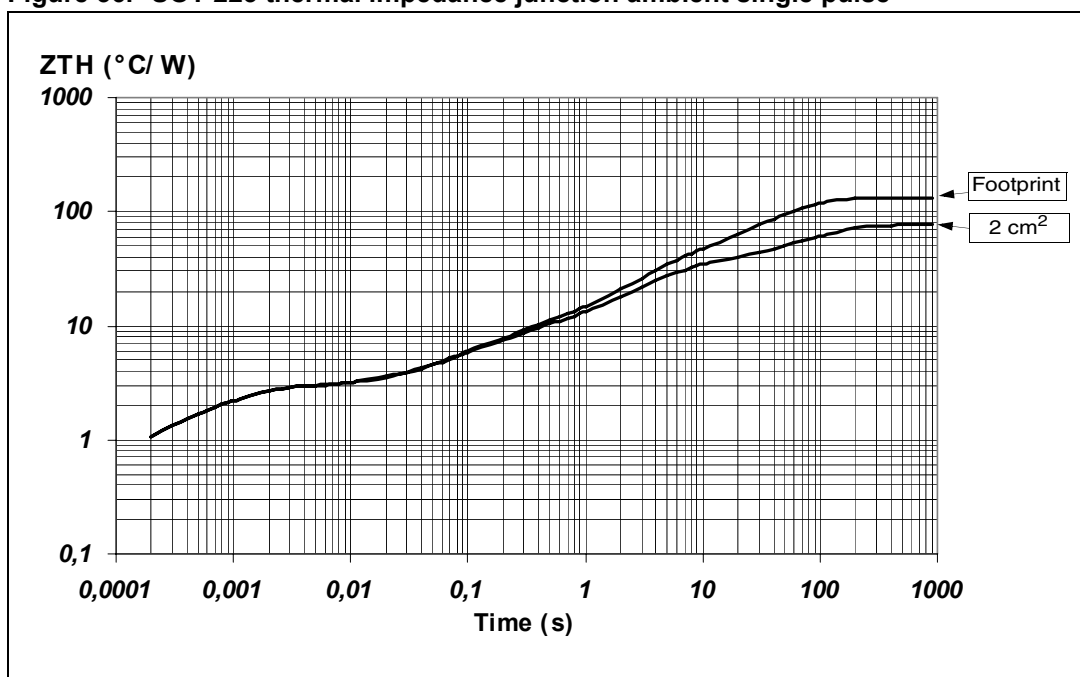
Figure 35. SOT-223 $R_{thj-amb}$ vs. PCB copper area in open box free air condition

Figure 36. SOT-223 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 37. SOT-223 thermal fitting model of a single channel

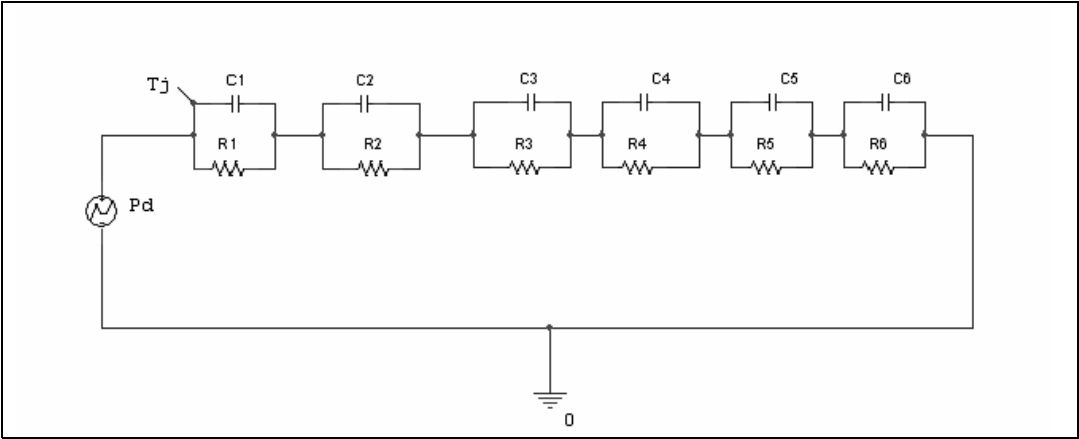
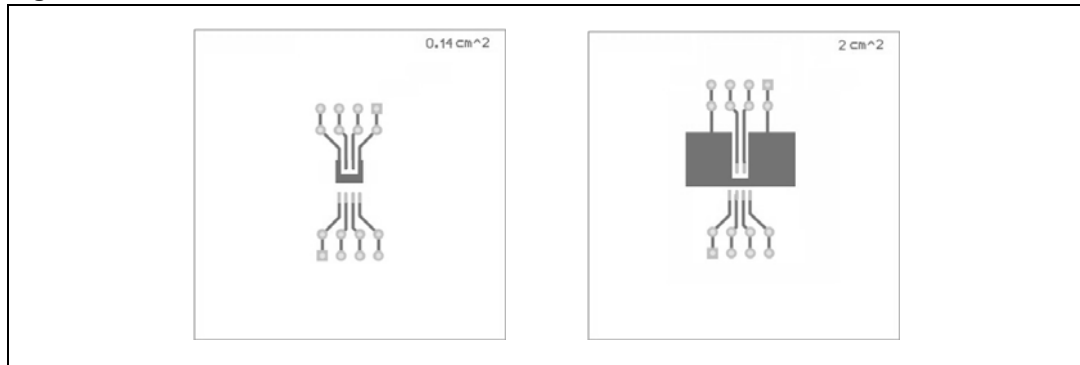


Table 6. SOT-223 thermal parameter

Area/island (cm ²)	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.5	2

4.3 SO-8 thermal data

Figure 38. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad layout to 2 cm²).

Figure 39. SO-8 $R_{thj-amb}$ vs. PCB copper area in open box free air condition

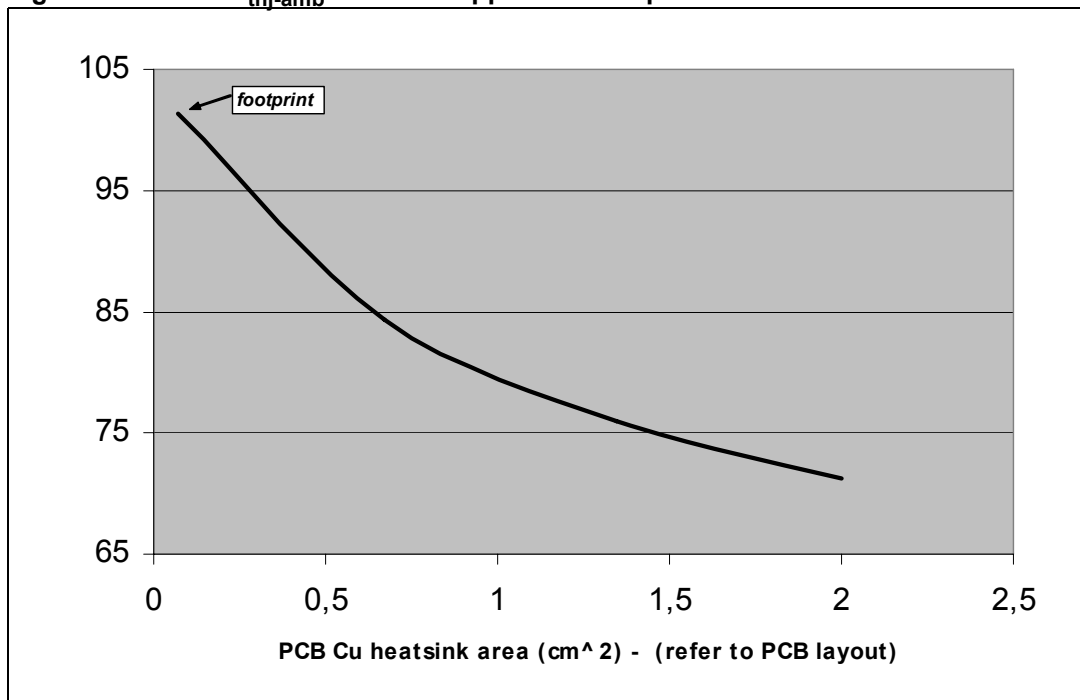
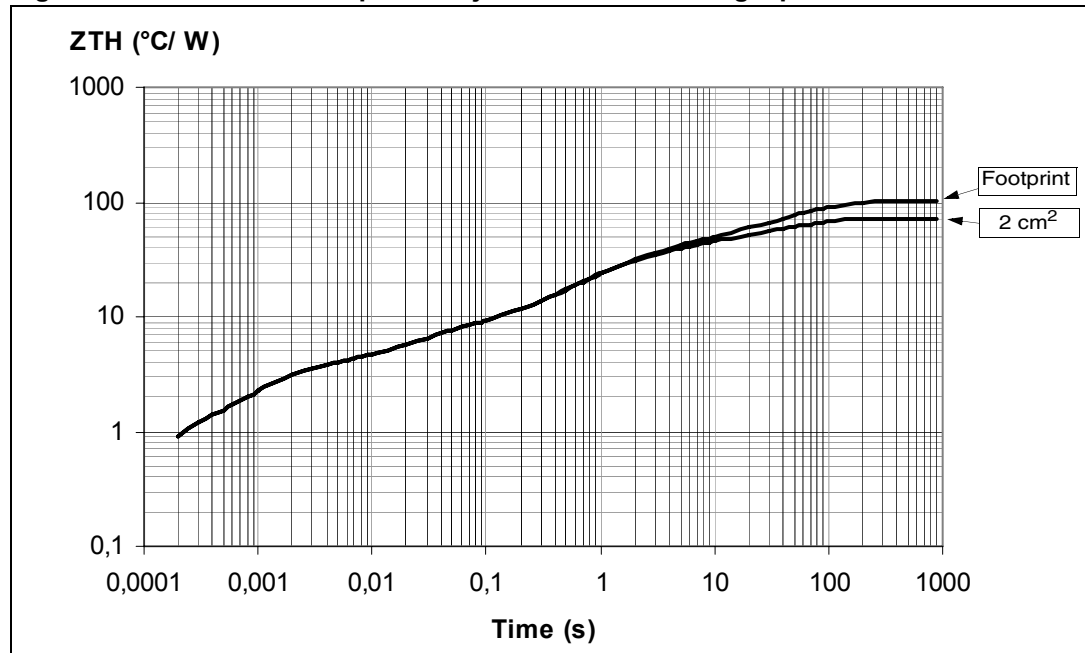


Figure 40. SO-8 thermal impedance junction ambient single pulse**Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

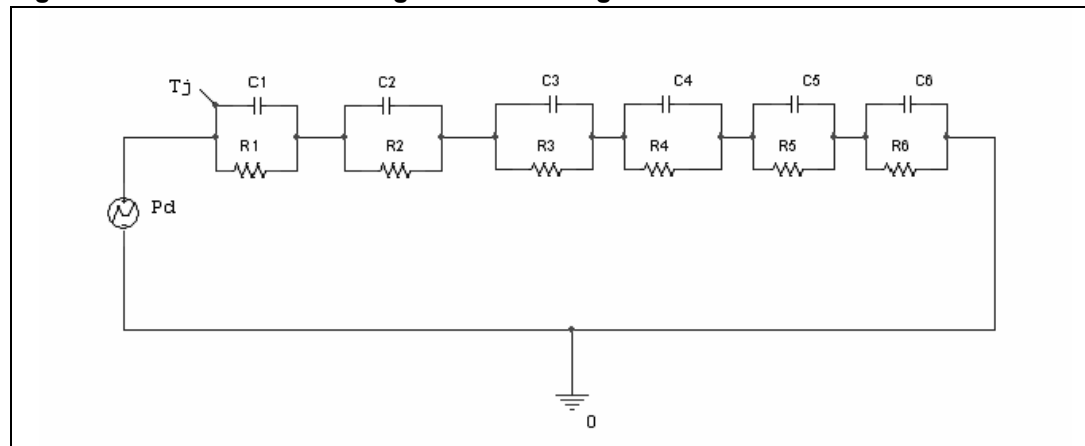
Figure 41. SO-8 thermal fitting model of a single channel

Table 7. SO-8 thermal parameter

Area/island (cm ²)	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.1 DPAK mechanical data

Figure 42. DPAK package dimensions

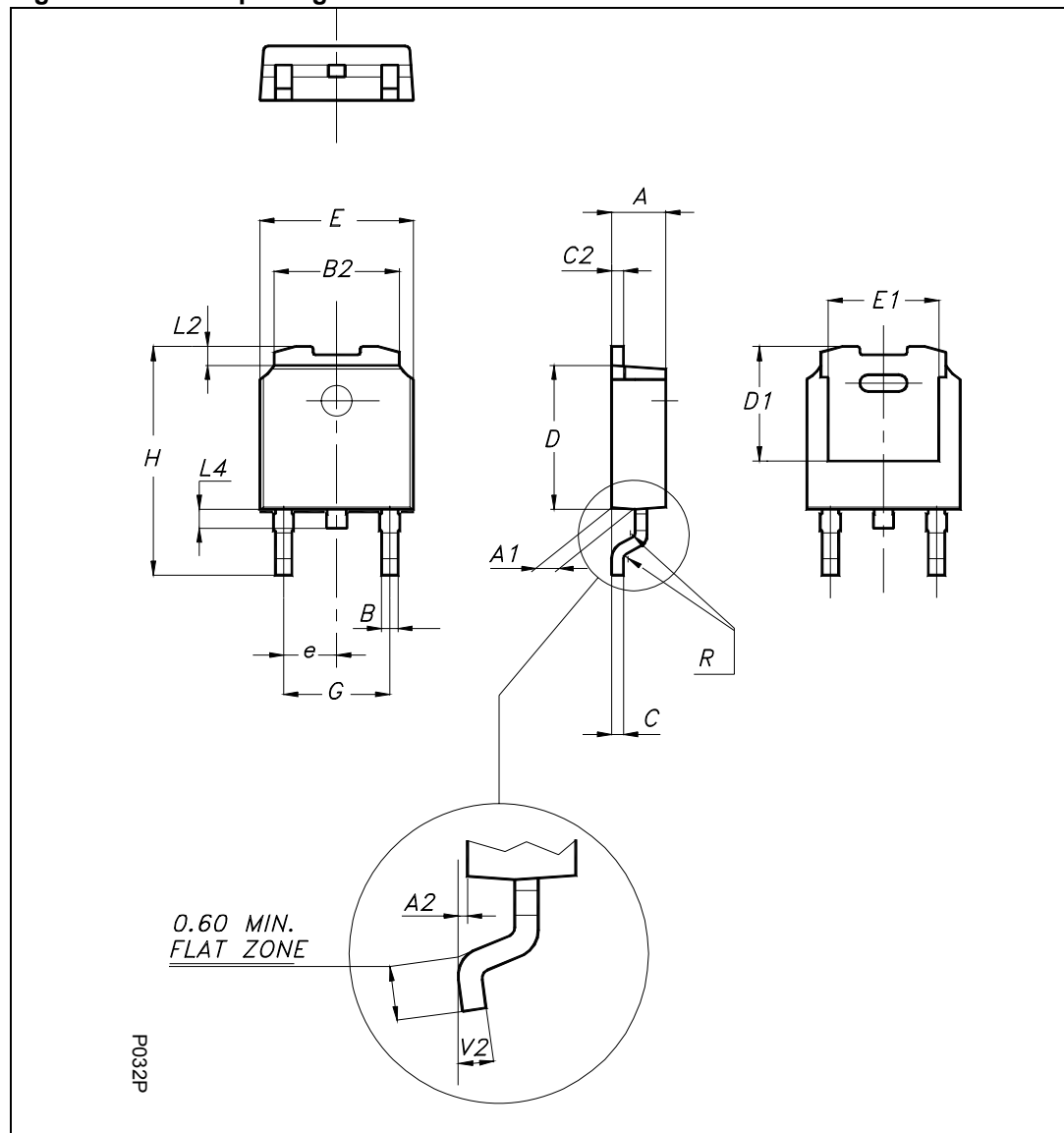
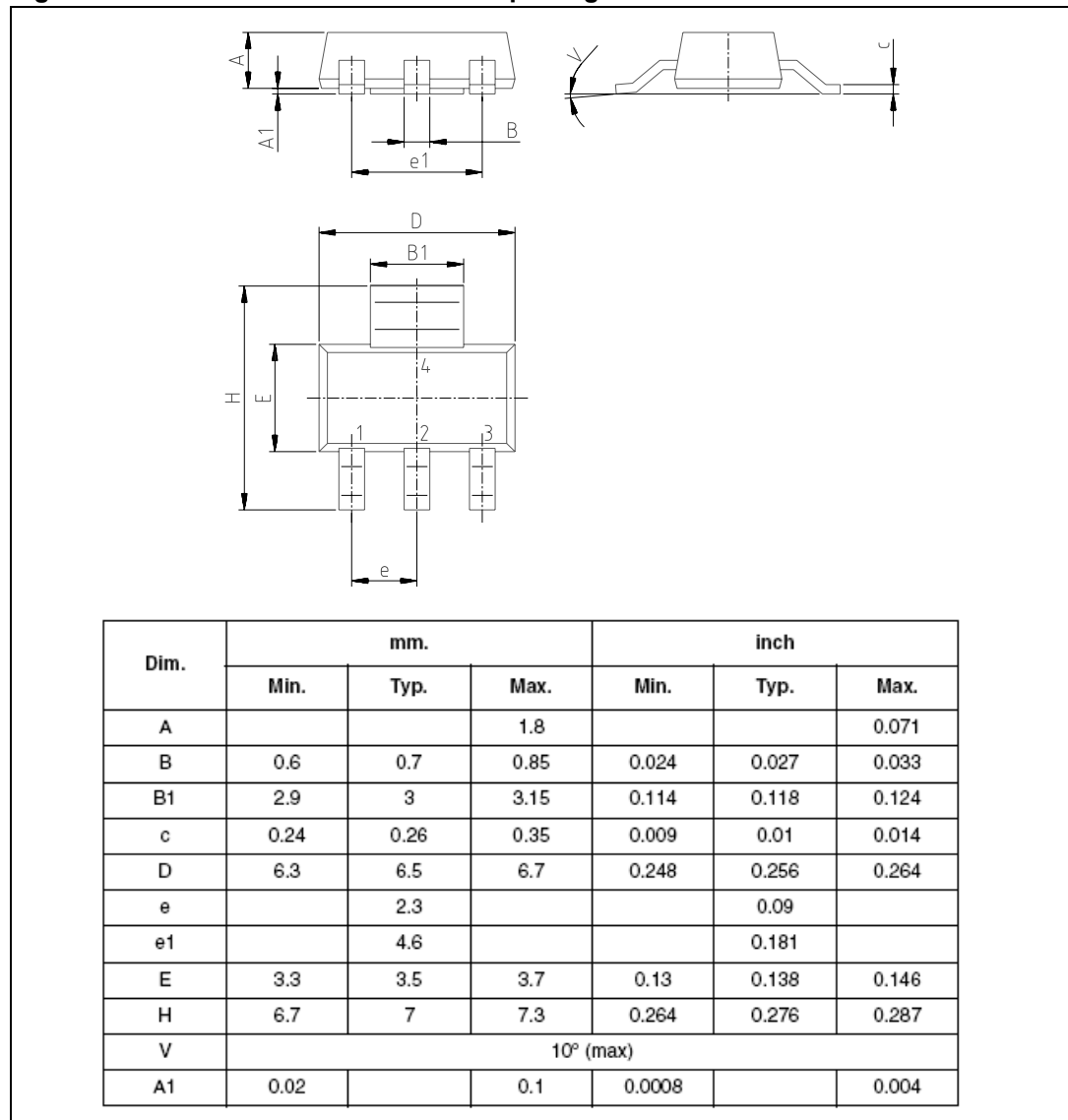


Table 8. DPAK mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

5.2 SOT-223 mechanical data

Figure 43. SOT-223 mechanical data & package outline



5.3 SO8 mechanical data

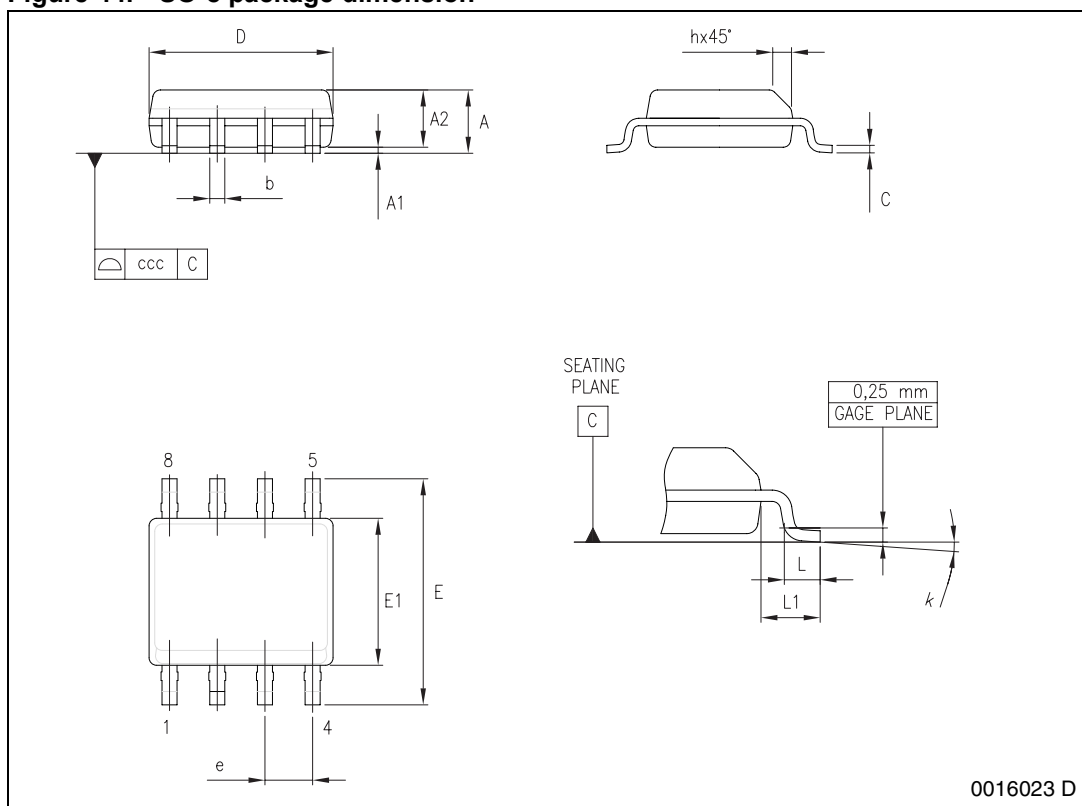
Table 9. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		

Table 9. SO-8 mechanical data (continued)

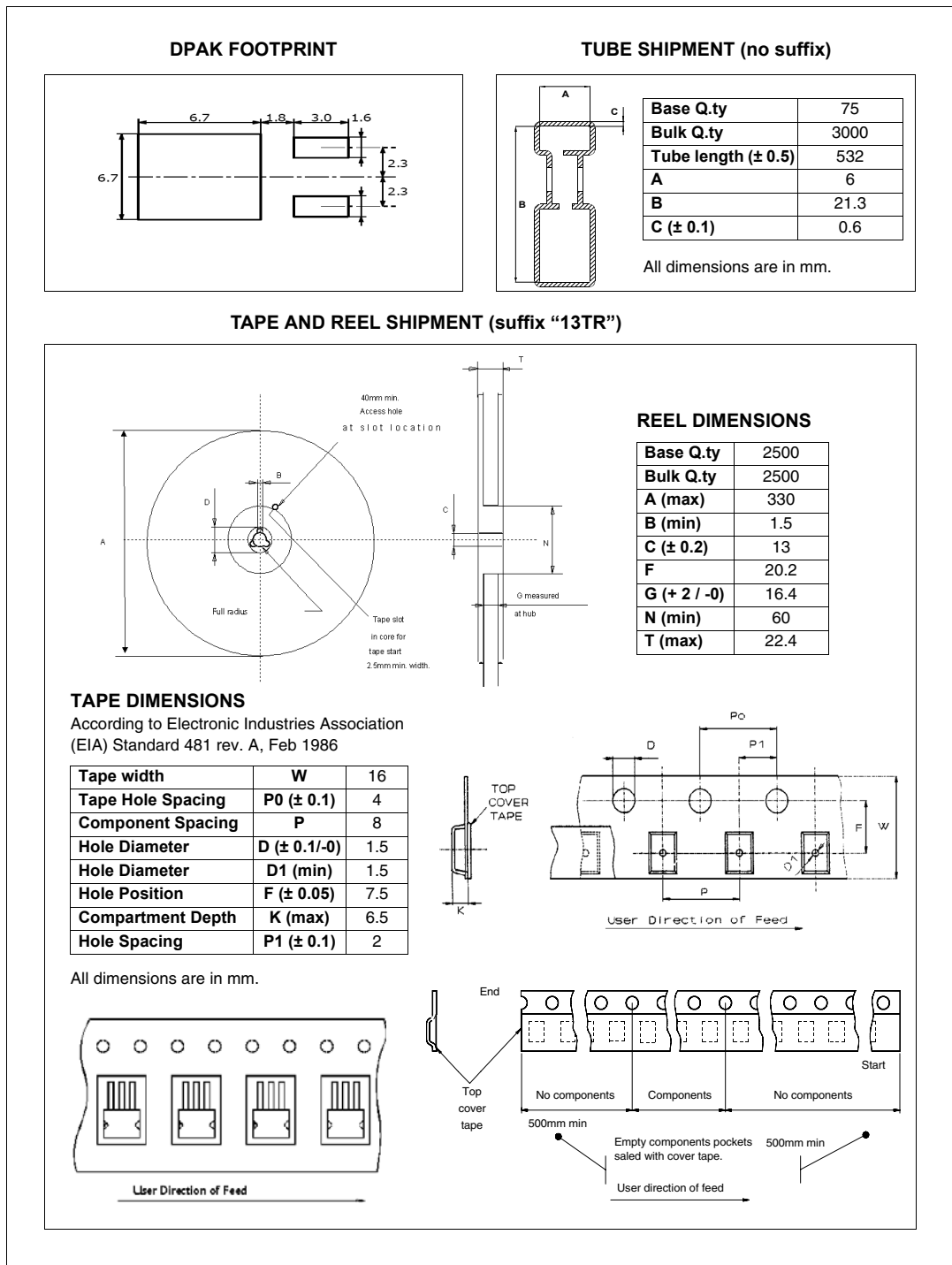
Dim.	mm		
	Min.	Typ.	Max.
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 44. SO-8 package dimension

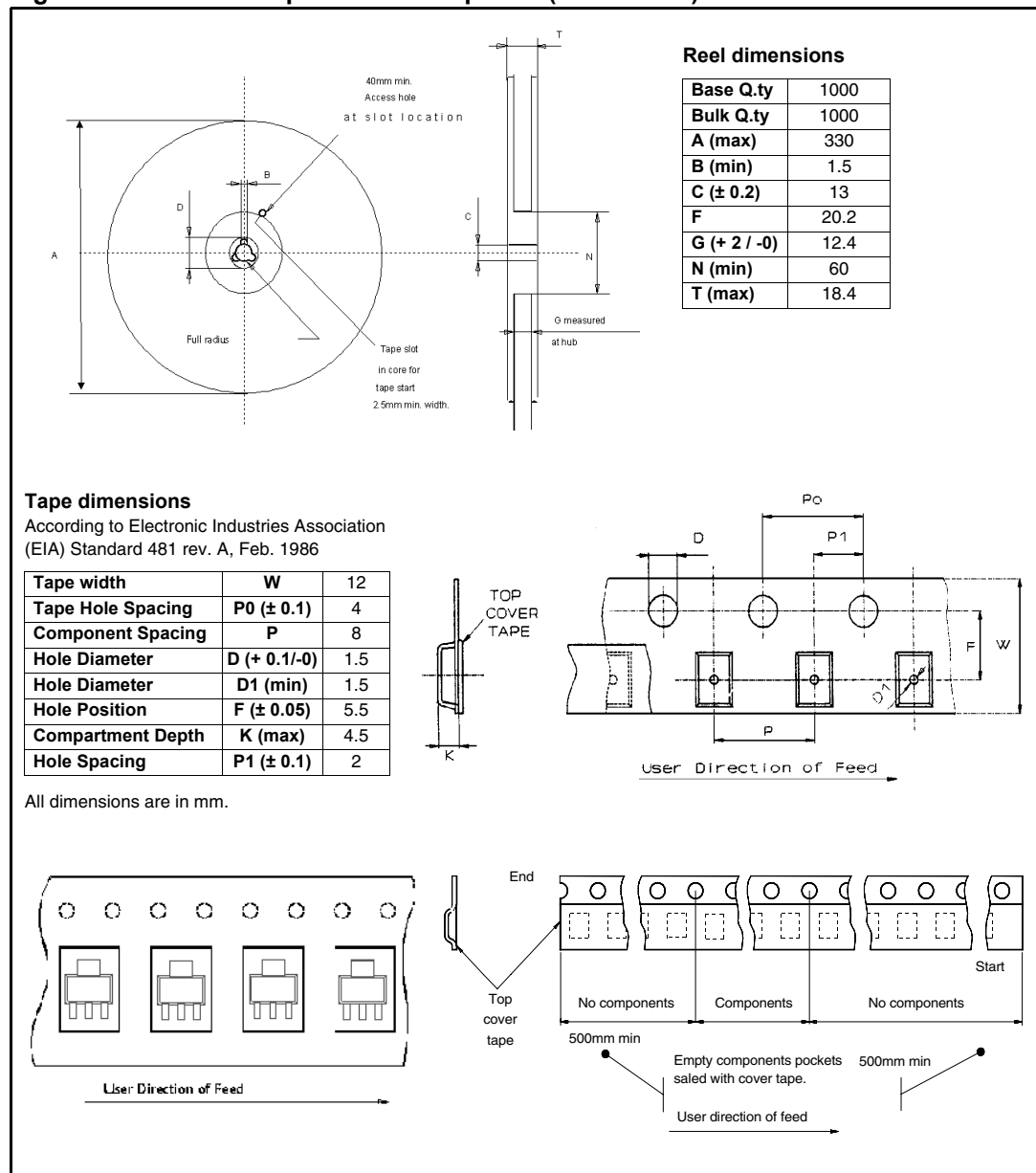
5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).



5.5 SOT-223 packing information

Figure 45. SOT-223 tape and reel shipment (suffix "TR")



5.6 SO8 packing information

Figure 46. SO-8 tube shipment (no suffix)

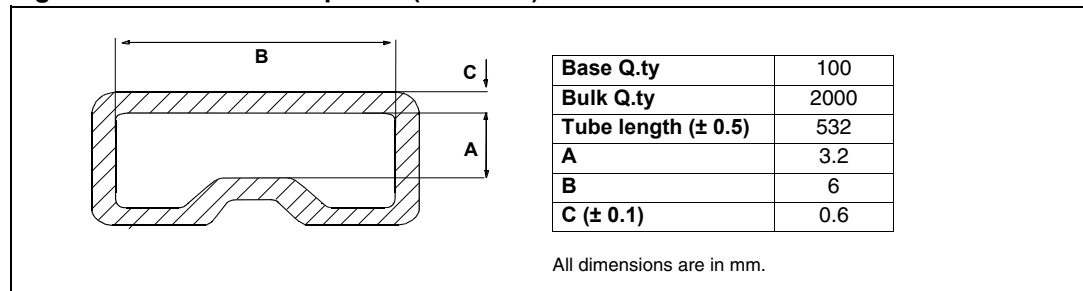
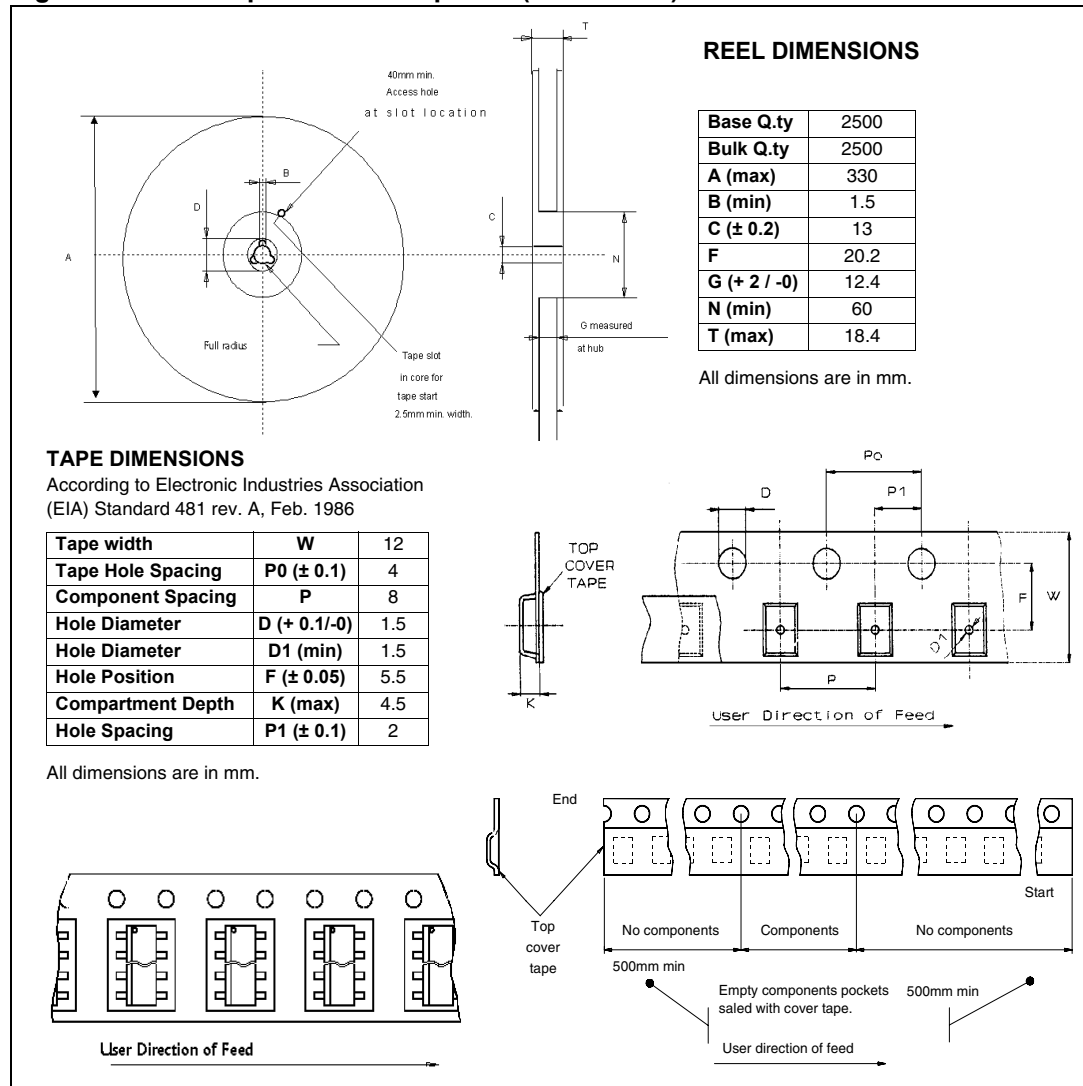


Figure 47. SO-8 tape and reel shipment (suffix "TR")



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
Feb-2003	1	Initial release.
16-Apr-2009	2	Added Table 1: Device summary on page 1 and Section 4: Package and PCB thermal data Updated Section 5: Package and packing information on page 25

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