HM628128D Series

1 M SRAM (128-kword × 8-bit)

HITACHI

ADE-203-996B (Z)
Rev. 1.0
Aug. 23, 1999

Description

The Hitachi HM628128D Series is 1-Mbit static RAM organized 131,072-kword × 8-bit. HM628128D Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. The HM628128D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has package variations of standard 32-pin plastic DIP, standard 32-pin plastic SOP and standard 32-pin plastic TSOPI.

Features

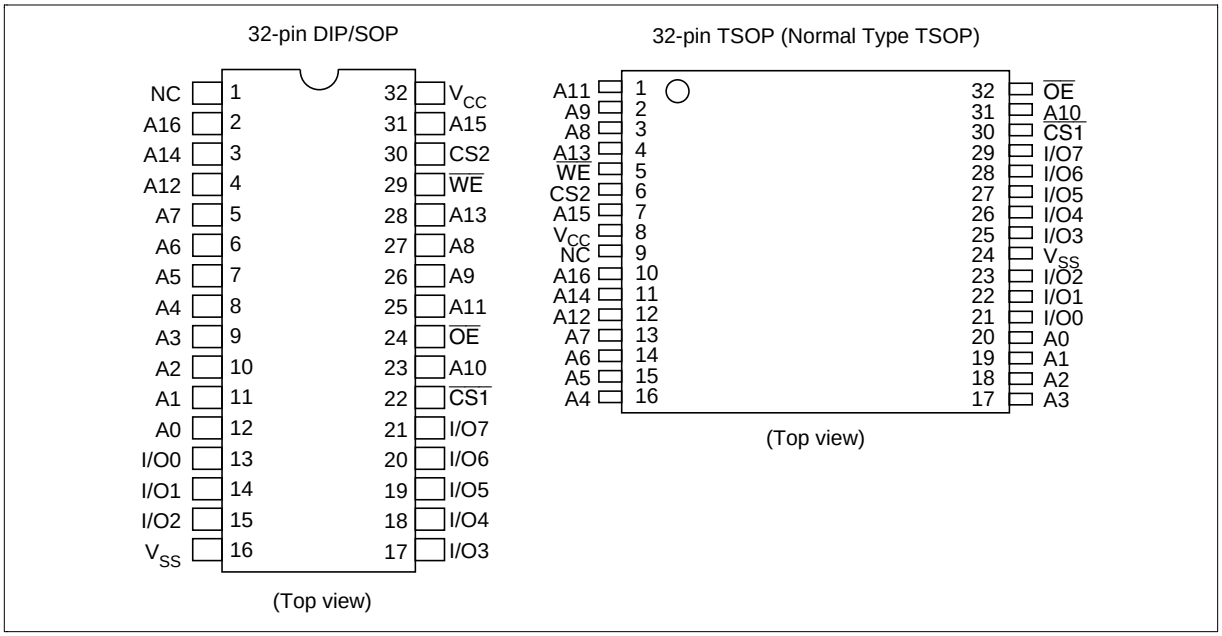
- Single 5 V supply: 5 V ± 10%
- Access time: 55 ns (max)
- Power dissipation
  - — Active: 30 mW/MHz (typ)
  - — Standby: 10 µW (typ)
- Completely static memory.
  - — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - — Three state output
- Directly TTL compatible all inputs
- Battery backup operation
  - — 2 chip selection for battery backup

Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HM628128DLP-5SL	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628128DLFP-5SL	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628128DLT-5SL	55 ns	Normal-bend type 8 × 20 mm 32-pin plastic TSOP I (TFP-32D)

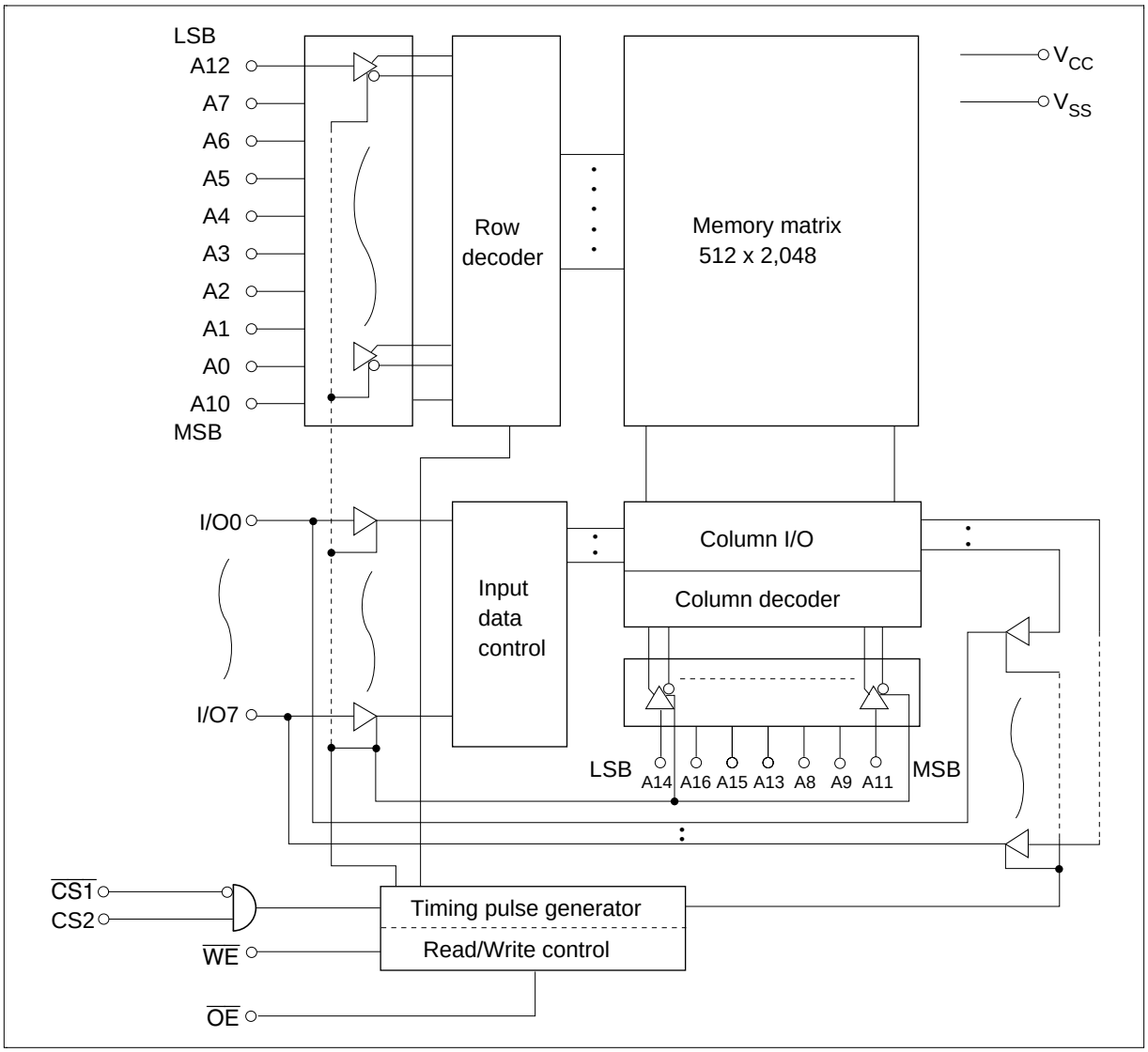
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O	Operation
H	×	×	×	High-Z	Standby
×	L	×	×	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	H	Din	Write
L	H	L	L	Din	Write
L	H	H	H	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–20 to +85	°C

Notes: 1. V_T min: –1.5 V for pulse half-width ≤ 30 ns
2. Maximum voltage is +7.0 V

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	–20	—	70	°C	

Note: 1. V_{IL} min: –1.5 V for pulse half-width ≤ 30 ns

DC Characteristics

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	60	mA	Min cycle, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	6	20	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current	I_{SB}	—	—	2	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH}, or (2) CS2 = V_{IL}
	I_{SB1}*[2]	—	2	50	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –20 to +70°C, V_{CC} = 5.0 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.8 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.5 V
- Output timing reference level: 1.5 V
- Output load: 1 TTL Gate+ CL (30pF) (Including scope and jig)

Read Cycle

		HM628128D			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time					
1 TTL Gate + CL (30pF)	t_{RC}	55	—	ns	
1 TTL Gate + CL (100pF)	t_{RC}	70	—	ns	
Address access time					
1 TTL Gate + CL (30pF)	t_{AA}	—	55	ns	
1 TTL Gate + CL (100pF)	t_{AA}	—	70	ns	
Chip select access time					
1 TTL Gate + CL (30pF)	t_{ACS1}	—	55	ns	
1 TTL Gate + CL (100pF)	t_{ACS1}	—	70	ns	
1 TTL Gate + CL (30pF)	t_{ACS2}	—	55	ns	
1 TTL Gate + CL (100pF)	t_{ACS2}	—	70	ns	
Output enable to output valid					
1 TTL Gate + CL (30pF)	t_{OE}	—	30	ns	
1 TTL Gate + CL (100pF)	t_{OE}	—	35	ns	
Output hold from address change	t_{OH}	10	—	ns	
Chip selection to output in low-Z	t_{CLZ1}	10	—	ns	2, 3
	t_{CLZ2}	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{CHZ1}	0	20	ns	1, 2, 3
	t_{CHZ2}	0	20	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2, 3

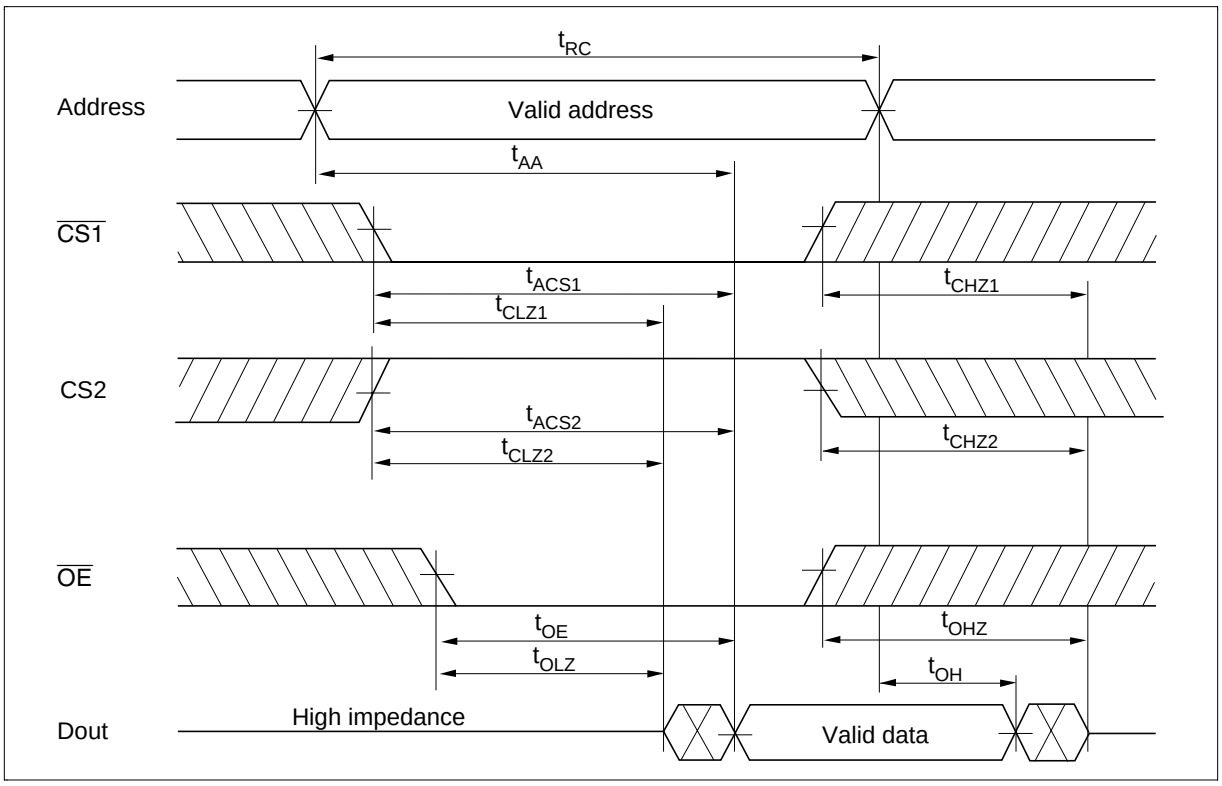
Write Cycle

		HM628128D			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	55	—	ns	
Address valid to end of write	t_{AW}	50	—	ns	
Chip selection to end of write	t_{CW}	50	—	ns	5
Write pulse width	t_{WP}	40	—	ns	4, 13
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2, 8
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	20	ns	1, 2, 8

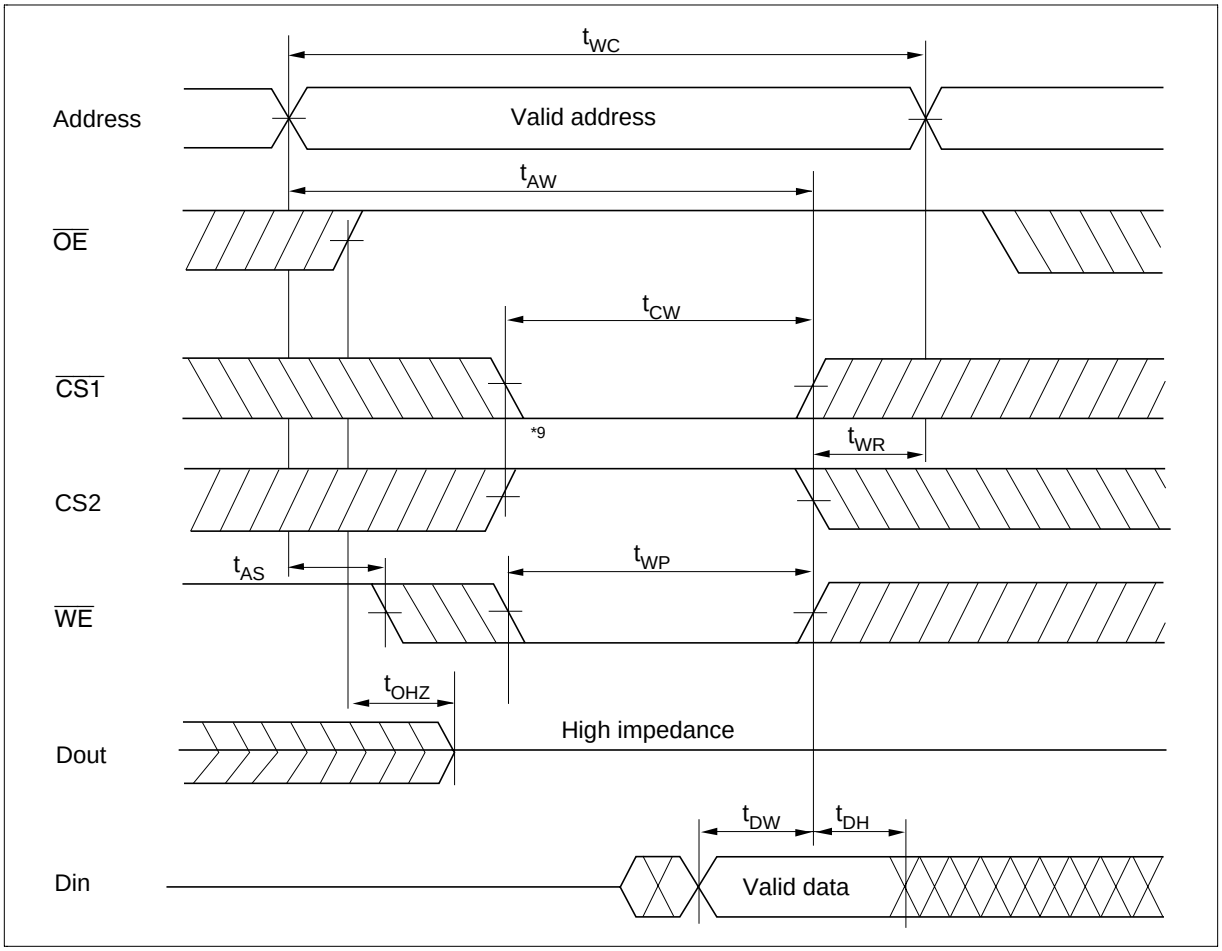
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS1}$ going high or CS2 going low to the end of write cycle.
8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
9. If the $\overline{CS1}$ goes low or CS2 going high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the output remain in a high impedance state.
10. Dout is the same phase of the write data of this write cycle.
11. Dout is the read data of next address.
12. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
13. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveforms

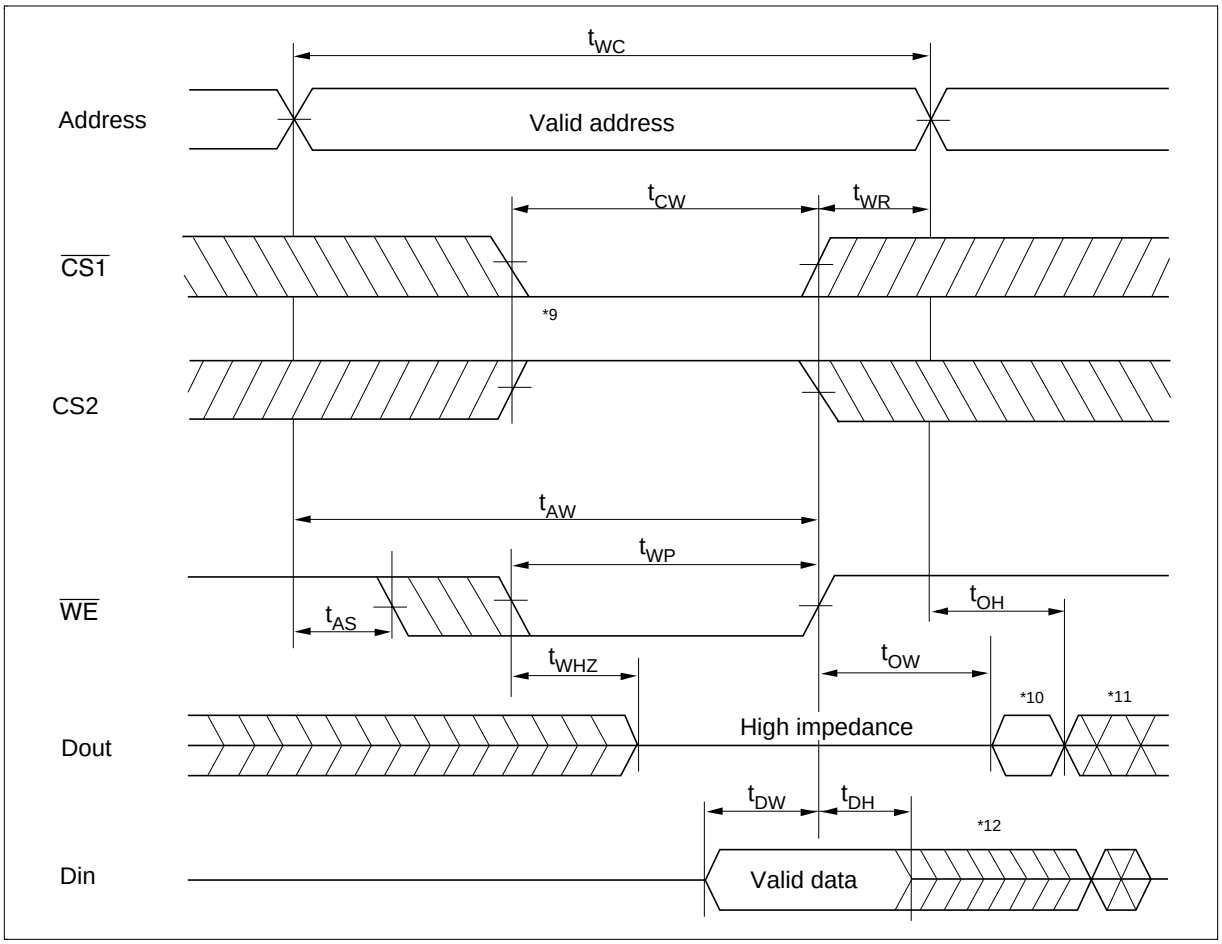
Read Cycle ($\overline{WE}$ = V_{IH})



Write Cycle (1) ($\overline{OE}$ Clock)



Write Cycle (2) ($\overline{OE}$ = V_{IL})



Low V_{CC} Data Retention Characteristics (Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ*3	Max	Unit	Test conditions*2
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Data retention current	I_{CCDR}*1	—	1.0	15	µA	V_{CC} = 3.0 V, Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

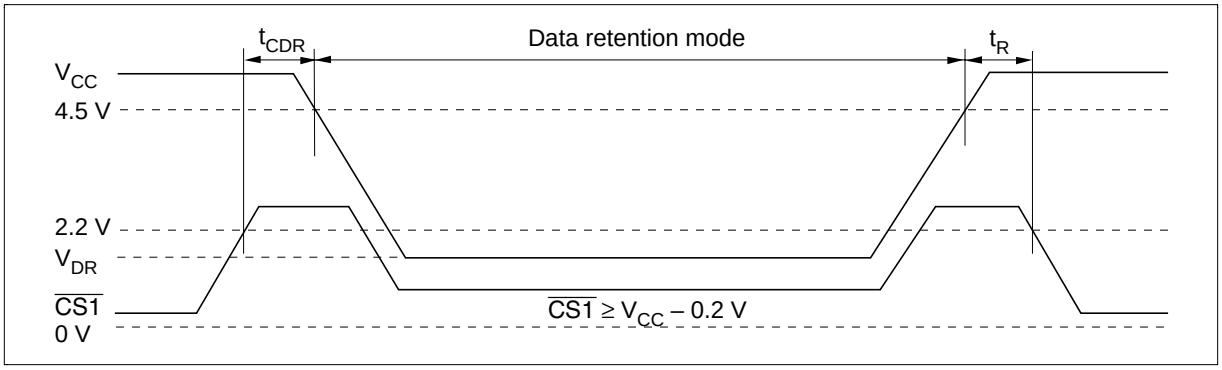
Notes: 1. This characteristic is guaranteed only for L-SL-version, 3 µA max. at Ta = –20 to +40°C.

2. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

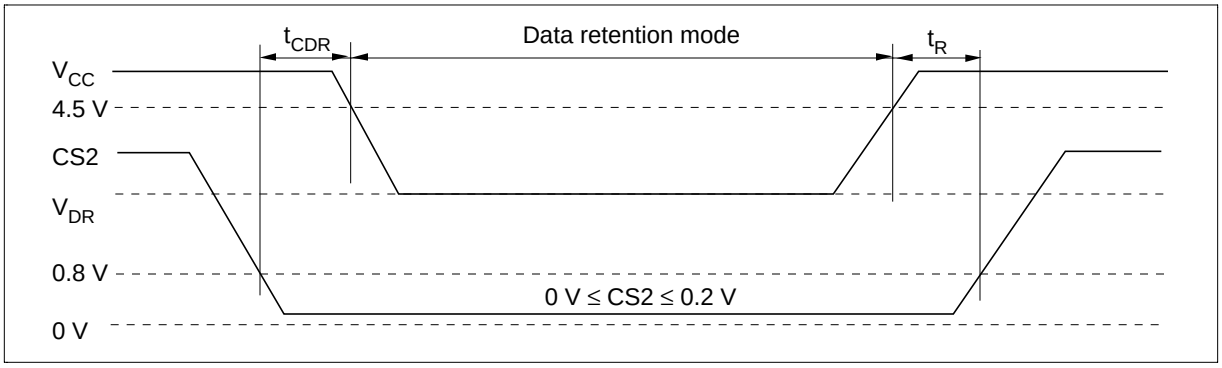
3. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.

4. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



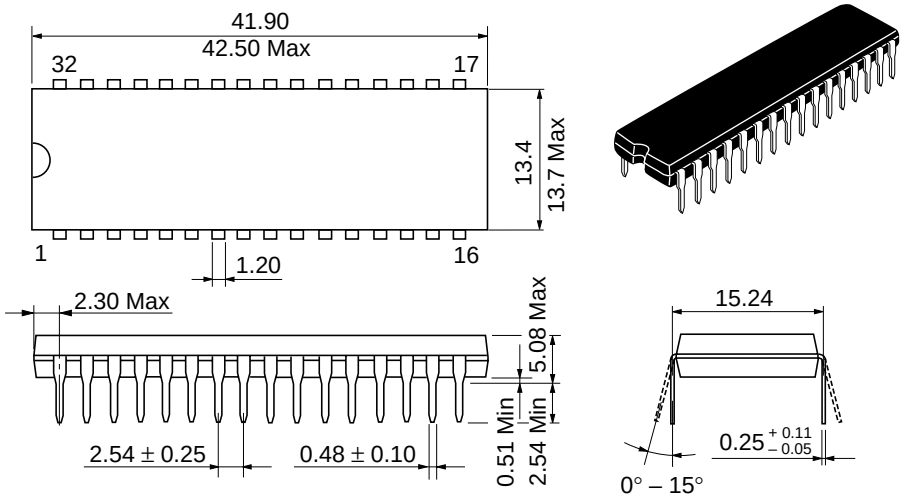
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM628128DLP Series (DP-32)

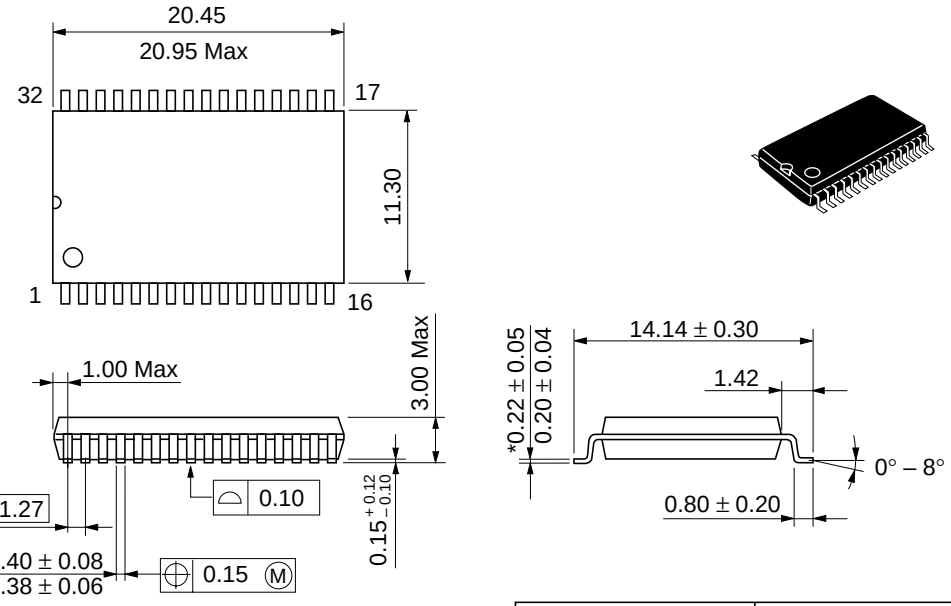
Unit: mm



Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

HM628128DLFP Series (FP-32D)

Unit: mm

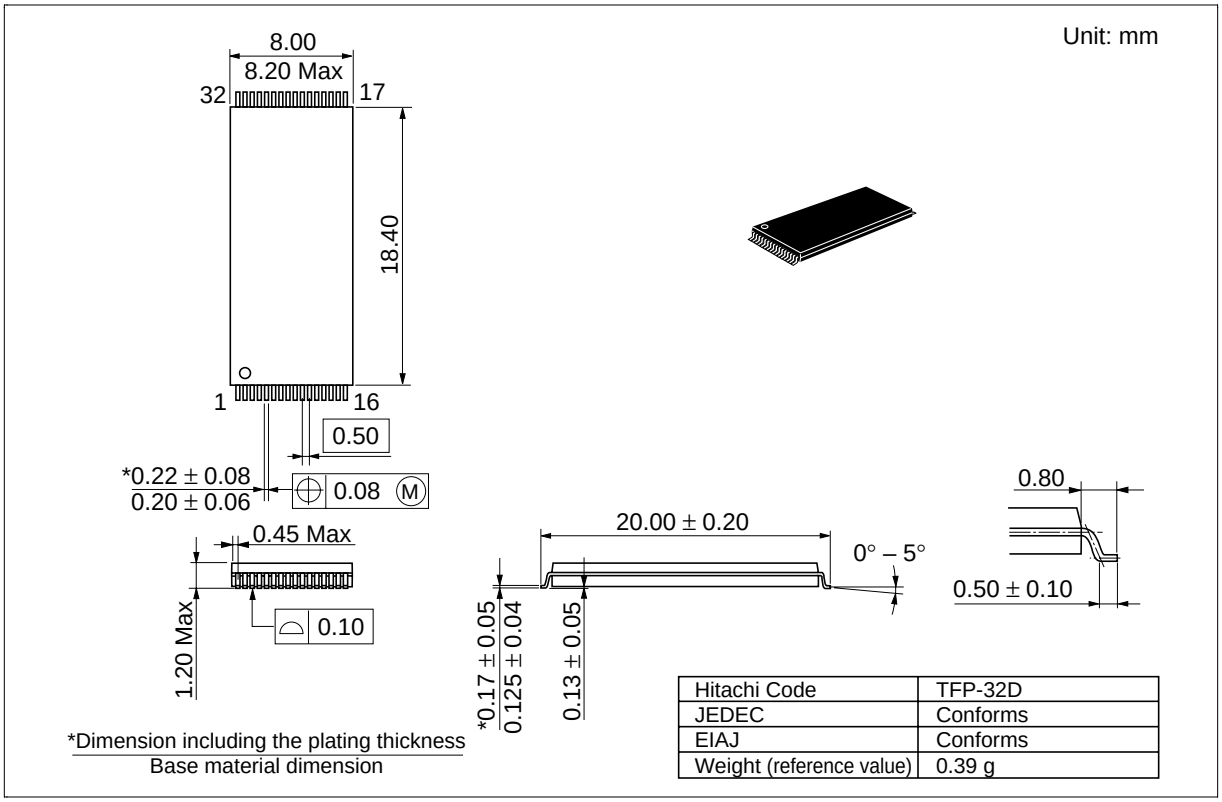


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

HM628128DLT Series (TFP-32D)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-32D
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.39 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jan. 20, 1999	Initial issue	H.Nakamura	K. Imato
0.1	Jul. 8, 1999	Deletion of HM628128D-7 Series Deletion of HM628128DLTS Series (TFP-32DC) and HM628128DLR Series (TFP-32DR) Deletion of L-version and L-UL version DC Characteristics I_{SB1} max: 100 µA to 50 µA Deletion of Notes2 and 4 AC Characteristics Test Conditions Output load: 1TTL Gate+CL(50 pF) to 1TTL Gate+CL(30 pF) t_{DW} min: 20 ns to 25 ns Correct error: Notes4 Low V_{CC} Data Retention Characteristics Deletion of Notes1 and 3	H.Nakamura	K. Imato
1.0	Aug. 23, 1999	Deletion of Preliminary		