

**NEC****MOS INTEGRATED CIRCUITS** **$\mu$ PD789101, 789102, 789104****8-BIT SINGLE-CHIP MICROCONTROLLER**

The  $\mu$ PD789101,  $\mu$ PD789102, and  $\mu$ PD789104 are  $\mu$ PD789104 sub-series products of the 78K/0S series.

These microcontrollers feature an 8-bit CPU, I/O ports, timers, a serial interface, A/D converters, and interrupt control circuits.

In addition, a flash memory product ( $\mu$ PD78F9116) that can operate within the same voltage range as the mask ROM models, and a range of related development tools are being developed.

**The functions of these microcontrollers are described in the following user's manual. Refer to this manual when designing a system based on any of these microcontrollers.**

**$\mu$ PD789134 Sub-Series User's Manual : To be created**

**78K/0S Series User's Manual, Instruction : U11047E**

**FEATURES**

- Built-in two 8-bit multipliers: 16 bits
- ROM and RAM sizes

| Item<br>Product name | Program memory<br>(ROM) | Data memory<br>(Internal high-speed RAM) | Package                             |
|----------------------|-------------------------|------------------------------------------|-------------------------------------|
| $\mu$ PD789101       | 2 Kbytes                | 256 bytes                                | 28-pin plastic shrink DIP (400 mil) |
| $\mu$ PD789102       | 4 Kbytes                |                                          | 30-pin plastic shrink SOP (300 mil) |
| $\mu$ PD789104       | 8 Kbytes                |                                          |                                     |

- Variable minimum instruction execution time: From high-speed (0.4  $\mu$ s) to low-speed (1.6  $\mu$ s) (operation with the main system clock running at 5.0 MHz)
- 20 I/O ports
- Serial interface channel: Switchable between three-wire serial I/O and UART modes
- Four-channel A/D converters with an 8-bit resolution
- Three timers:
  - 16-bit timer 20
  - 8-bit timer/event counter 80
  - Watchdog timer
- Power supply voltage  $V_{DD}$ : 1.8 to 5.5 V

**APPLICATIONS**

Cleaners, washing machines, and refrigerators

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

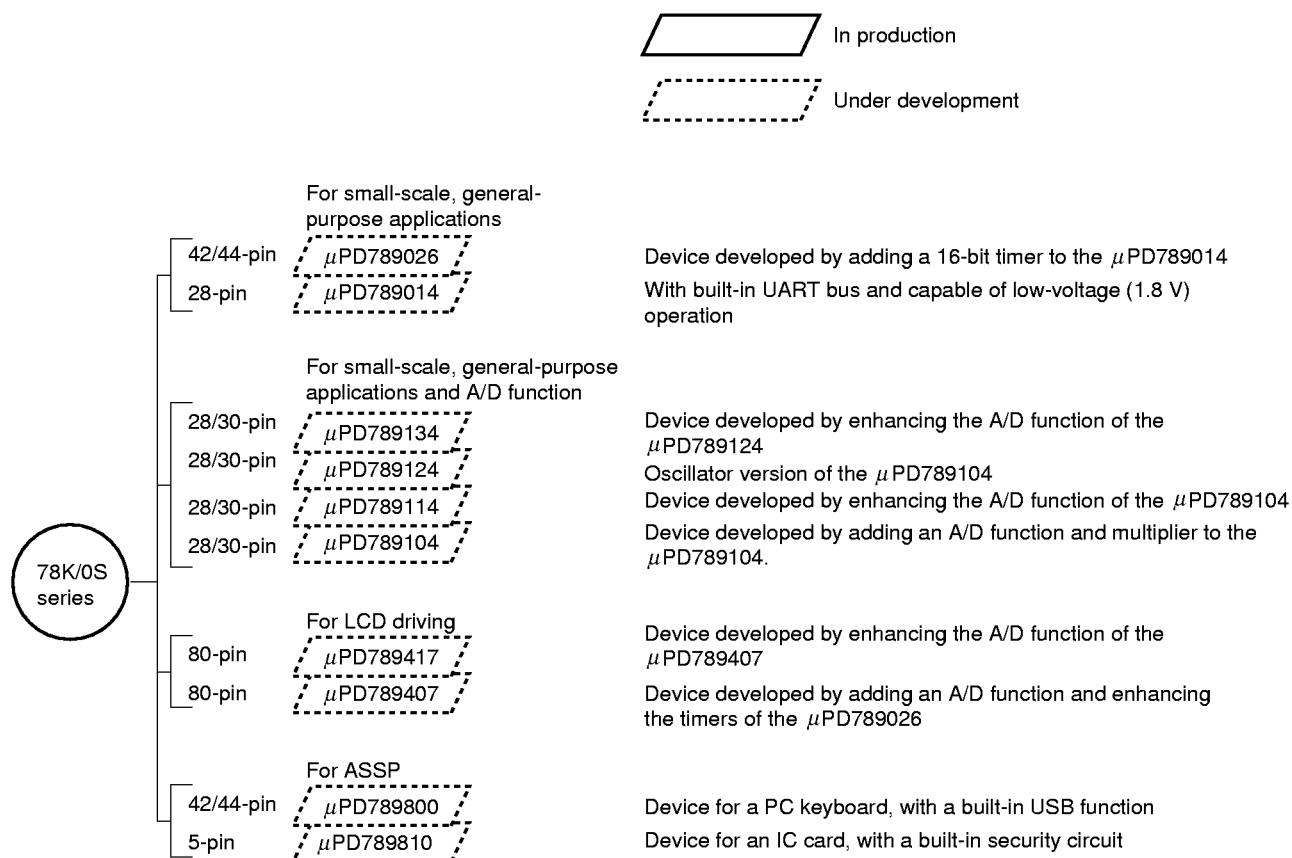
**ORDERING INFORMATION**

| Part number          | Package                             |
|----------------------|-------------------------------------|
| $\mu$ PD789101CT-xxx | 28-pin plastic shrink DIP (400 mil) |
| $\mu$ PD789101GS-xxx | 30-pin plastic shrink SOP (300 mil) |
| $\mu$ PD789102CT-xxx | 28-pin plastic shrink DIP (400 mil) |
| $\mu$ PD789102GS-xxx | 30-pin plastic shrink SOP (300 mil) |
| $\mu$ PD789104CT-xxx | 28-pin plastic shrink DIP (400 mil) |
| $\mu$ PD789104GS-xxx | 30-pin plastic shrink SOP (300 mil) |

**Remark** xxx indicates the ROM code number.

## 78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The sub-series names are indicated in frames.



The following table lists the major differences in functions between the sub-series.

| Sub-series                                                 | Function  | ROM size  | Timer |        |       |      | 8-bit A/D | 10-bit A/D | Serial interface  | I/O     | Minimum V <sub>DD</sub> value | Remarks               |
|------------------------------------------------------------|-----------|-----------|-------|--------|-------|------|-----------|------------|-------------------|---------|-------------------------------|-----------------------|
|                                                            |           |           | 8-bit | 16-bit | Clock | WDT  |           |            |                   |         |                               |                       |
| Small-scale general purpose                                | μPD789026 | 4 K-16 K  | 1 ch  | 1 ch   | -     | 1 ch | -         | -          | 1 ch (UART: 1 ch) | 34 pins | 1.8 V                         | -                     |
|                                                            | μPD789014 | 2 K-4 K   | 2 ch  | -      | -     | -    | -         | -          | -                 | 22 pins | -                             | -                     |
| Small-scale, general-purpose applications and A/D function | μPD789134 | 2 K-8 K   | 1 ch  | 1 ch   | -     | 1 ch | -         | 4 ch       | 1 ch (UART: 1 ch) | 20 pins | 1.8 V                         | RC-oscillator version |
|                                                            | μPD789124 |           |       |        |       |      | 4 ch      | -          |                   |         |                               | -                     |
|                                                            | μPD789114 |           |       |        |       |      | -         | 4 ch       |                   |         |                               | -                     |
|                                                            | μPD789104 |           |       |        |       |      | 4 ch      | -          |                   |         |                               | -                     |
| LCD driving                                                | μPD789417 | 12 K-24 K | 3 ch  | 1 ch   | 1 ch  | 1 ch | -         | 7 ch       | 1 ch (UART: 1 ch) | 43 pins | 1.8 V                         | -                     |
|                                                            | μPD789407 |           |       |        |       |      | 7 ch      | -          |                   |         |                               |                       |
| ASSP                                                       | μPD789800 | 8 K       | 2 ch  | -      | -     | 1 ch | -         | -          | 2 ch (USB: 1 ch)  | 31 pins | 4.0 V                         | -                     |
|                                                            | μPD789810 | 6 K       | -     | -      | -     | -    | -         | -          | -                 | 1 pin   | 1.8 V                         | -                     |

**FUNCTIONS**

| Item                               |                | $\mu$ PD789101                                                                                                                                                                                      | $\mu$ PD789102 | $\mu$ PD789104 |
|------------------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------|
| Built-in memory                    | ROM            | 2 Kbytes                                                                                                                                                                                            | 4 Kbytes       | 8 Kbytes       |
|                                    | High-speed RAM | 256 bytes                                                                                                                                                                                           |                |                |
| Minimum instruction execution time |                | 0.4/1.6 $\mu$ s (operation with main system clock running at 5.0 MHz)                                                                                                                               |                |                |
| General-purpose registers          |                | 8 bits $\times$ 8 registers                                                                                                                                                                         |                |                |
| Instruction set                    |                | <ul style="list-style-type: none"> <li>• 16-bit operations</li> <li>• Bit manipulations (such as set, reset, and test)</li> </ul>                                                                   |                |                |
| Multiplier                         |                | 8 bits $\times$ 2 = 16 bits                                                                                                                                                                         |                |                |
| I/O ports                          |                | Total of 20 port pins <ul style="list-style-type: none"> <li>• 4 CMOS input pins</li> <li>• 12 CMOS input/output pins</li> <li>• 4 N-channel open-drain pins (withstand voltage of 12 V)</li> </ul> |                |                |
| A/D converters                     |                | Four channels with 8-bit resolution                                                                                                                                                                 |                |                |
| Serial interface                   |                | <ul style="list-style-type: none"> <li>• Switchable between three-wire serial I/O and UART modes</li> </ul>                                                                                         |                |                |
| Timers                             |                | <ul style="list-style-type: none"> <li>• 16-bit timer 20</li> <li>• 8-bit timer/event counter 80</li> <li>• Watchdog timer</li> </ul>                                                               |                |                |
| Timer output                       |                | One output                                                                                                                                                                                          |                |                |
| Vectored interrupt sources         | Maskable       | 7 internal and 3 external interrupts                                                                                                                                                                |                |                |
|                                    | Non-maskable   | Internal interrupt                                                                                                                                                                                  |                |                |
| Power supply voltage               |                | $V_{DD} = 1.8$ to 5.5 V                                                                                                                                                                             |                |                |
| Operating ambient temperature      |                | $T_A = -40$ to +85 °C                                                                                                                                                                               |                |                |
| Package                            |                | <ul style="list-style-type: none"> <li>• 28-pin plastic shrink DIP (400 mil)</li> <li>• 30-pin plastic shrink SOP (300 mil)</li> </ul>                                                              |                |                |

## CONTENTS

|                                                                 |    |
|-----------------------------------------------------------------|----|
| 1. PIN CONFIGURATION (TOP VIEW) .....                           | 6  |
| 2. BLOCK DIAGRAM .....                                          | 8  |
| 3. PIN FUNCTIONS .....                                          | 9  |
| 3.1 Port Pins .....                                             | 9  |
| 3.2 Non-Port Pins .....                                         | 10 |
| 3.3 Pin Input/Output Circuits and Handling of Unused Pins ..... | 11 |
| 4. MEMORY SPACE .....                                           | 13 |
| 5. PERIPHERAL HARDWARE FUNCTIONS .....                          | 14 |
| 5.1 Ports .....                                                 | 14 |
| 5.2 Clock Generator .....                                       | 15 |
| 5.3 Timer .....                                                 | 16 |
| 5.4 A/D Converter .....                                         | 18 |
| 5.5 Serial Interface Channel .....                              | 19 |
| 5.6 Multiplier .....                                            | 20 |
| 6. INTERRUPT FUNCTION .....                                     | 21 |
| 7. STANDBY FUNCTION .....                                       | 23 |
| 8. RESET FUNCTION .....                                         | 23 |
| 9. INSTRUCTION SET .....                                        | 24 |
| 10. ELECTRICAL CHARACTERISTICS (TARGET VALUES) .....            | 27 |
| 11. PACKAGE DRAWINGS .....                                      | 39 |
| APPENDIX A DEVELOPMENT TOOLS .....                              | 41 |
| APPENDIX B RELATED DOCUMENTS .....                              | 42 |

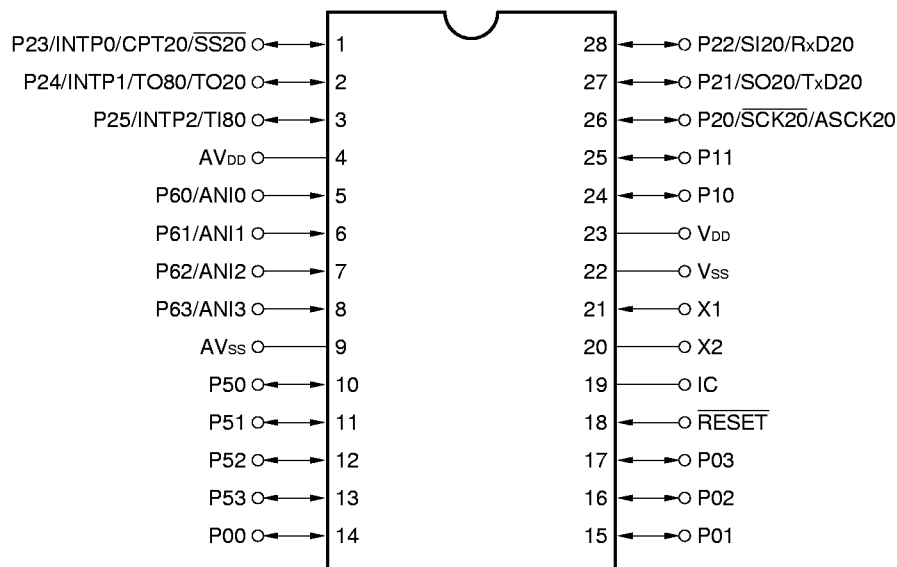
# 1. PIN CONFIGURATION (TOP VIEW)

- 28-pin plastic shrink DIP (400 mil)

μPD789101CT-xxx

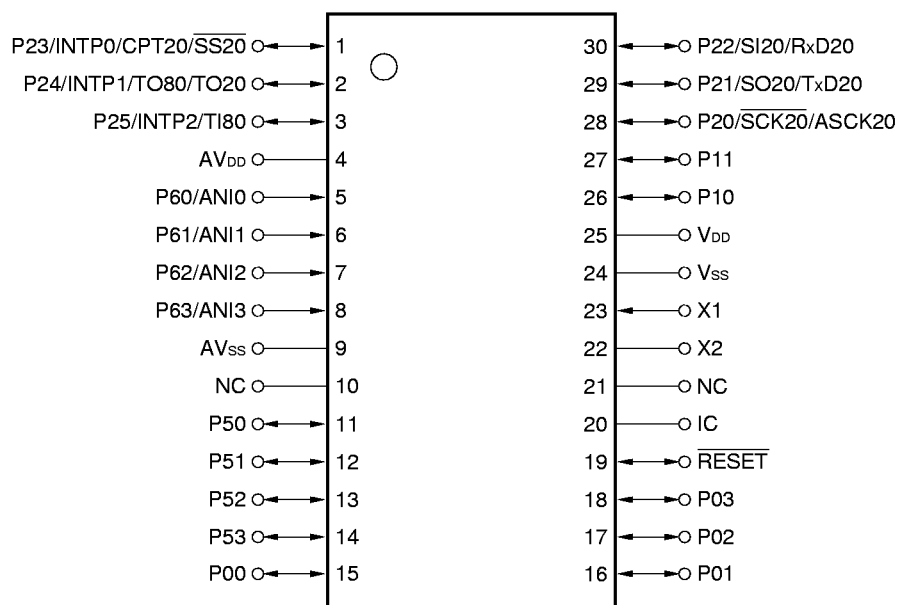
μPD789102CT-xxx

μPD789104CT-xxx



- Cautions**
1. Connect the IC (Internally connected) pin directly to the VSS pin.
  2. Connect the AVDD pin to the VDD pin.
  3. Connect the AVSS pin to the VSS pin.

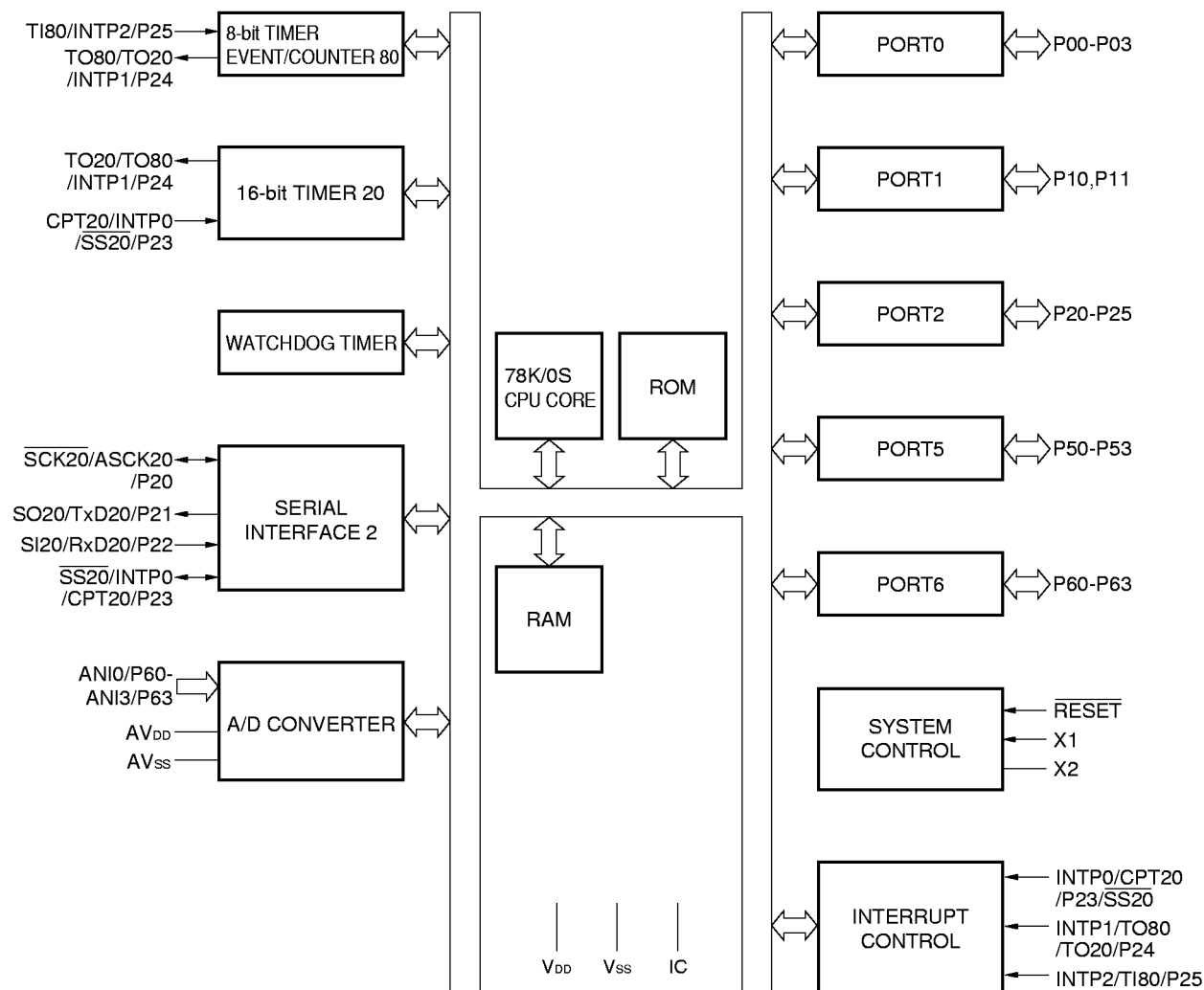
- 30-pin plastic shrink SOP (300 mil)  
μPD789101GS-xxx  
μPD789102GS-xxx  
μPD789104GS-xxx



- Cautions**
1. Connect the IC (internally connected) pin directly to the V<sub>SS</sub> pin.
  2. Connect the AV<sub>DD</sub> pin to the V<sub>DD</sub> pin.
  3. Connect the AV<sub>SS</sub> pin to the V<sub>SS</sub> pin.

|                  |                              |                    |                     |
|------------------|------------------------------|--------------------|---------------------|
| ANI0-ANI3        | : Analog Input               | P60-P63            | : Port6             |
| ASCK20           | : Asynchronous Serial Input  | $\overline{RESET}$ | : Reset             |
| AV <sub>DD</sub> | : Analog Power Supply        | RxD20              | : Receive Data      |
| AV <sub>SS</sub> | : Analog Ground              | $\overline{SCK20}$ | : Serial Clock      |
| CPT20            | : Capture Trigger Input      | SI20               | : Serial Input      |
| IC               | : Internally Connected       | SO20               | : Serial Output     |
| INTP0-INTP2      | : Interrupt from Peripherals | $\overline{SS20}$  | : Chip Select Input |
| NC               | : Non-connection             | TI80               | : Timer Input       |
| P00-P03          | : Port0                      | TO20, TO80         | : Timer Output      |
| P10, P11         | : Port1                      | TxD20              | : Transmit Data     |
| P20-P25          | : Port2                      | V <sub>DD</sub>    | : Power Supply      |
| P50-P53          | : Port5                      | V <sub>SS</sub>    | : Ground            |
|                  |                              | X1, X2             | : Crystal 1, 2      |

## 2. BLOCK DIAGRAM



**Remark** The size of the built-in ROM varies depending on the model.

### 3. PIN FUNCTIONS

#### 3.1 Port Pins

| Pin name | I/O   | Function                                                                                                                                                                                                  | When reset | Also used as      |
|----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------|
| P00-P03  | I/O   | Port 0<br>4-bit input/output port<br>Can be set to either input or output in 1-bit units<br>When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. | Input      | -                 |
| P10, P11 | I/O   | Port 1<br>2-bit input/output port<br>Can be set to either input or output in 1-bit units<br>When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. | Input      | -                 |
| P20      | I/O   | Port 2<br>6-bit input/output port<br>Can be set to either input or output in 1-bit units<br>When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. | Input      | SCK20/ASCK20      |
| P21      |       |                                                                                                                                                                                                           |            | SO20/TxD20        |
| P22      |       |                                                                                                                                                                                                           |            | SI20/RxD20        |
| P23      |       |                                                                                                                                                                                                           |            | INTP0/CPT20 /SS20 |
| P24      |       |                                                                                                                                                                                                           |            | INTP1/TO80/TO20   |
| P25      |       |                                                                                                                                                                                                           |            | INTP2/TI80        |
| P50-P53  | I/O   | Port 5<br>4-bit N-channel open-drain input/output port<br>Can be set to either input or output in 1-bit units<br>Whether a pull-up resistor is to be incorporated can be specified by a mask option.      | Input      | -                 |
| P60-P63  | Input | Port 6<br>4-bit input-only port                                                                                                                                                                           | Input      | ANI0-ANI3         |

### 3.2 Non-Port Pins

| Pin name         | I/O    | Function                                                                                          | When reset | Also used as    |
|------------------|--------|---------------------------------------------------------------------------------------------------|------------|-----------------|
| INTP0            | Input  | External interrupt input for which effective edges (rising and/or falling edges) can be specified | Input      | P23/CPT20/SS20  |
| INTP1            |        |                                                                                                   |            | P24/TO80/TO20   |
| INTP2            |        |                                                                                                   |            | P25/TI80        |
| SI20             | Input  | Serial data input to serial interface                                                             | Input      | P22/RxD20       |
| SO20             | Output | Serial data output from serial interface                                                          | Input      | P21/TxD20       |
| SCK20            | I/O    | Serial clock input/output for serial interface                                                    | Input      | P20/ASCK20      |
| ASCK20           | Input  | Serial clock input to asynchronous serial interface                                               | Input      | P20/SCK20       |
| SS20             | Input  | Chip select input to serial interface                                                             | Input      | P23/CPT20/INTP0 |
| RxD20            | Input  | Serial data input to asynchronous serial interface                                                | Input      | P22/SI20        |
| TxD20            | Output | Serial data output from asynchronous serial interface                                             | Input      | P21/SO20        |
| TI80             | Input  | External count clock input to 8-bit timer (TM80)                                                  | Input      | P25/INTP2       |
| TO80             | Output | 8-bit timer (TM80) output                                                                         | Input      | P24/INTP1/TO20  |
| TO20             | Output | 16-bit timer (TM20) output                                                                        | Input      | P24/INTP1/TO80  |
| CPT20            | Input  | Capture edge input                                                                                | Input      | P23/INTP0/SS20  |
| ANI0-ANI3        | Input  | A/D converter analog input                                                                        | Input      | P60-P63         |
| AV <sub>SS</sub> | -      | A/D converter ground potential                                                                    | -          | -               |
| AV <sub>DD</sub> | -      | A/D converter analog power supply                                                                 | -          | -               |
| X1               | Input  | Connected to crystal for main system clock oscillation                                            | -          | -               |
| X2               | -      |                                                                                                   | -          | -               |
| RESET            | Input  | System reset input                                                                                | Input      | -               |
| V <sub>DD</sub>  | -      | Positive supply voltage                                                                           | -          | -               |
| V <sub>SS</sub>  | -      | Ground potential                                                                                  | -          | -               |
| IC               | -      | Internally connected directly to the V <sub>SS</sub> pin                                          | -          | -               |

### 3.3 Pin Input/Output Circuits and Handling of Unused Pins

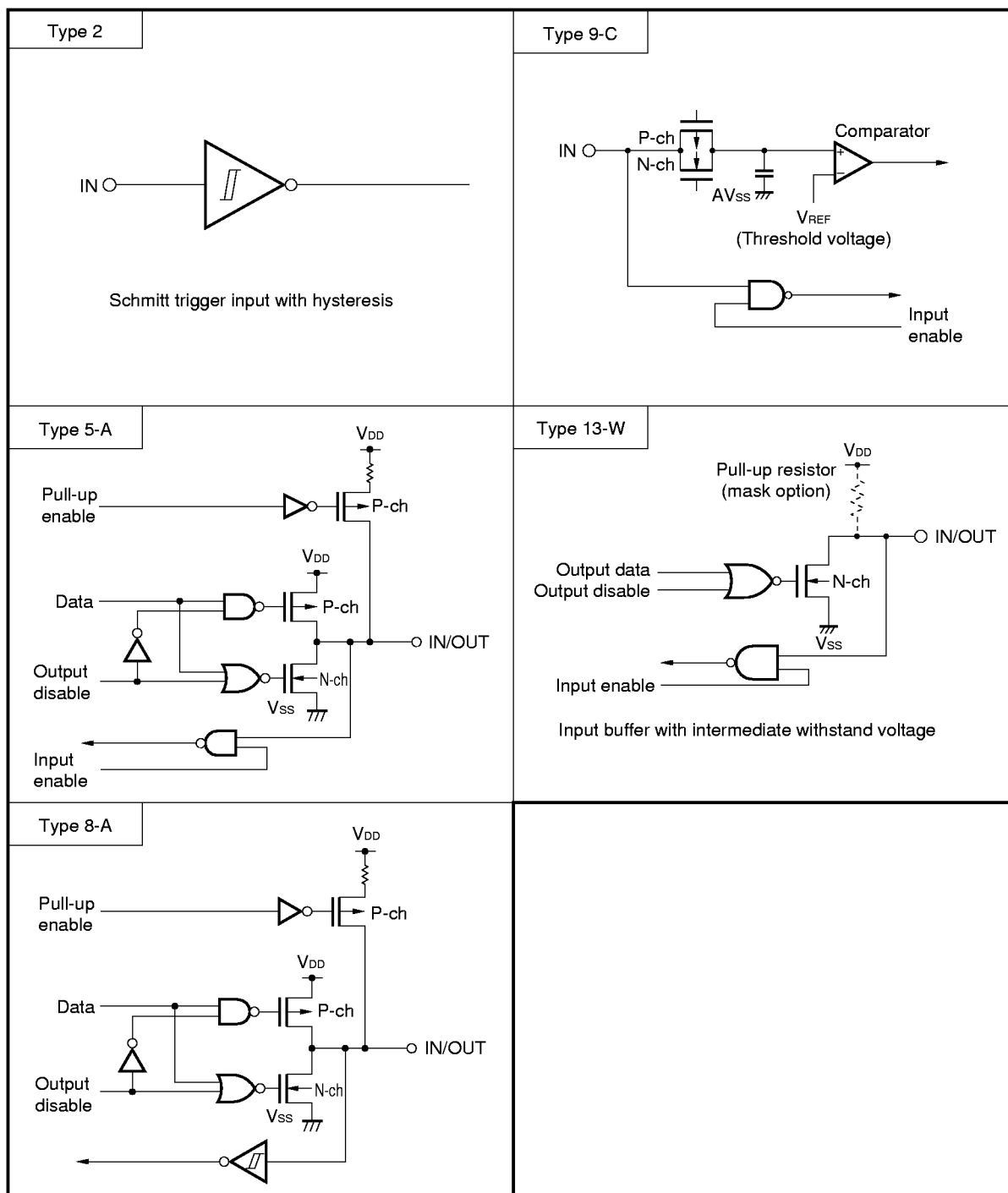
Table 3-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.

Figure 3-1 shows the configuration of each type of input/output circuit.

**Table 3-1. Type of Input/Output Circuit for Each Pin and Handling of Unused Pins**

| Pin name             | I/O circuit type | I/O                                                                        | Recommended connection of unused pins                                                         |
|----------------------|------------------|----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| P00-P03              | 5-A              | I/O                                                                        | Connect these pins to the V <sub>DD</sub> or V <sub>SS</sub> pin through a separate resistor. |
| P10, P11             |                  |                                                                            |                                                                                               |
| P20/SCK20/ASCK20     | 8-A              |                                                                            |                                                                                               |
| P21/SO20/TxD20       |                  |                                                                            |                                                                                               |
| P22/SI20/RxD20       |                  |                                                                            |                                                                                               |
| P23/INTP0/CPT20/SS20 |                  |                                                                            | Connect these pins to the V <sub>SS</sub> pin through a separate resistor.                    |
| P24/INTP1/TO80/TO20  |                  |                                                                            |                                                                                               |
| P25/INTP2/TI80       |                  |                                                                            |                                                                                               |
| P50-P53              | 13-W             | Connect these pins to the V <sub>DD</sub> pin through a separate resistor. |                                                                                               |
| P60/ANI0-P63/ANI3    | 9-C              | Input                                                                      | Connect these pins to the V <sub>DD</sub> or V <sub>SS</sub> pin through a separate resistor. |
| AV <sub>DD</sub>     | -                | -                                                                          | Connect this pin to the V <sub>DD</sub> pin through a resistor.                               |
| AV <sub>SS</sub>     | -                | -                                                                          | Connect this pin to the V <sub>SS</sub> pin through a resistor.                               |
| RESET                | 2                | Input                                                                      | -                                                                                             |
| IC                   | -                | -                                                                          | Connect this pin directly to the V <sub>SS</sub> pin.                                         |

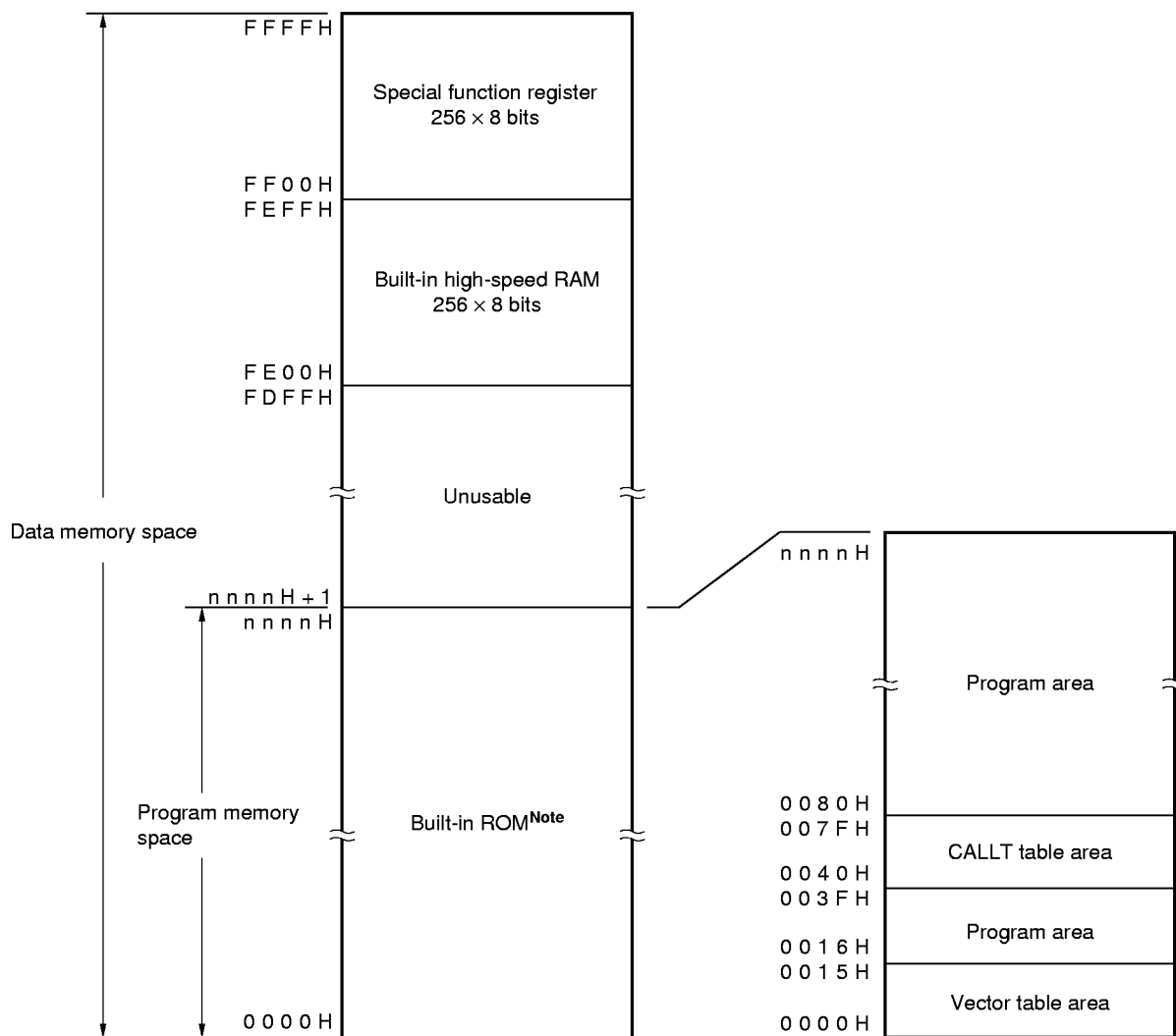
Figure 3-1. Pin Input/Output Circuits



## 4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD789101, μPD789102, and μPD789104.

Figure 4-1. Memory Map



**Note** The size of the built-in ROM varies depending on the model. (See the following table.)

| Product name | Last address of built-in ROM<br>nnnnH |
|--------------|---------------------------------------|
| μPD789101    | 07FFH                                 |
| μPD789102    | 0FFFH                                 |
| μPD789104    | 1FFFH                                 |

## 5. PERIPHERAL HARDWARE FUNCTIONS

### 5.1 Ports

The following three types of I/O ports are supported:

- CMOS Input ports (port 6) : 4 pins
  - CMOS input/output ports (ports 0 to 2) : 12 pins
  - N-ch open-drain input/output ports (port 5) : 4 pins
- 
- Total : 20 pins

**Table 5-1. Port Functions**

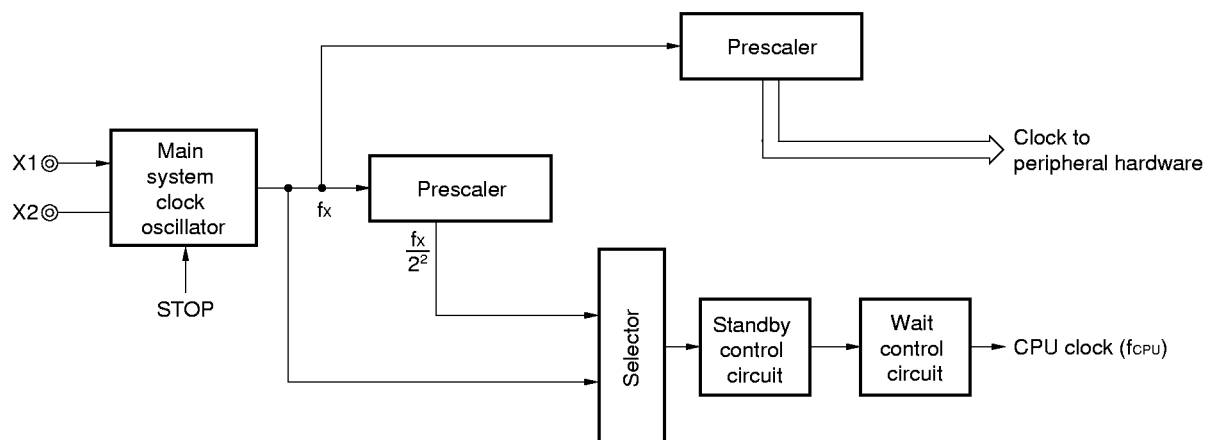
| Port name | Pin name | Description                                                                                                                                                                                                      |
|-----------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Port 0    | P00-P03  | Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.     |
| Port 1    | P10, P11 | Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.     |
| Port 2    | P20-P25  | Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.     |
| Port 5    | P50-P53  | N-channel open-drain input/output port. Each bit of the port can be separately specified as being for input or output. Whether the port itself is to contain a pull-up resistor is specified with a mask option. |
| Port 6    | P60-P63  | Input-only port                                                                                                                                                                                                  |

## 5.2 Clock Generator

An on-chip main system clock generator is provided.  
It is possible to change the instruction execution time.

- 0.4  $\mu$ s/ 1.6  $\mu$ s (when the main system clock operates at 5.0 MHz)

Figure 5-1. Block Diagram of Clock Generator



### 5.3 Timer

Three on-chip timers are provided.

- 16-bit timer 20 : 1 channel
- 8-bit timer/event counter 80 : 1 channel
- Watchdog timer : 1 channel

### Table 5-2. Timer Operation

|                |                         | 16-bit timer 20 | 8-bit timer/event counters 80 | Watchdog timer |
|----------------|-------------------------|-----------------|-------------------------------|----------------|
| Operation mode | Interval timer          | 1 channel       | 1 channel                     | 1 channel      |
|                | External event counter  | -               | 1 channel                     | -              |
| Function       | Timer output            | 1 output        | 1 output                      | -              |
|                | PWM output              | -               | 1 output                      | -              |
|                | Pulse-width measurement | 1 input         | -                             | -              |
|                | Square wave output      | 1 output        | 1 output                      | -              |
|                | Interrupt request       | 1               | 1                             | 1              |

**Figure 5-2. Block Diagram of 16-Bit Timer 20 (TM20)**

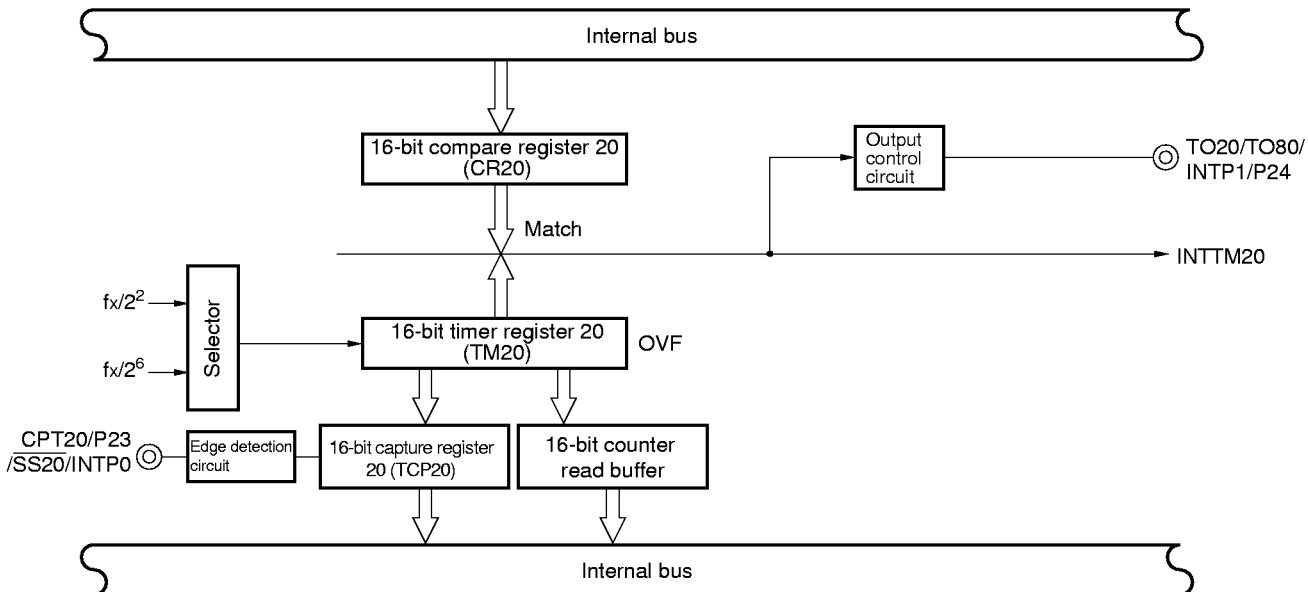


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80 (TM80)

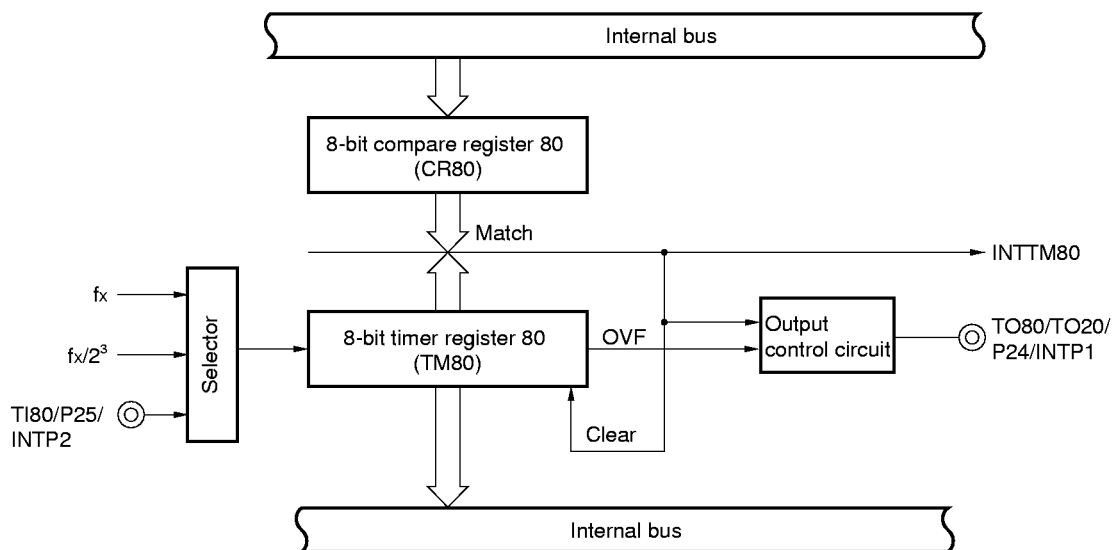
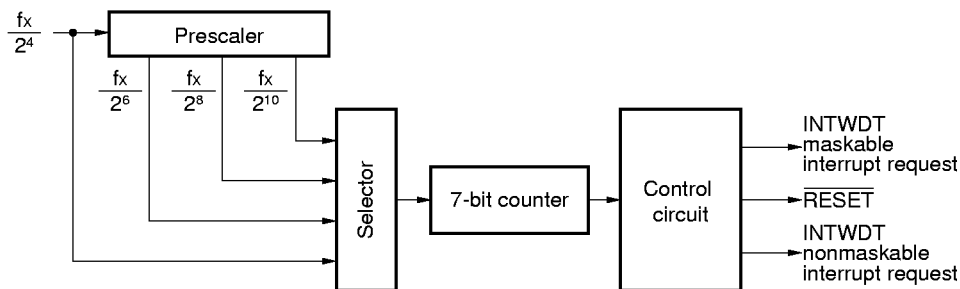


Figure 5-4. Block Diagram of Watchdog Timer

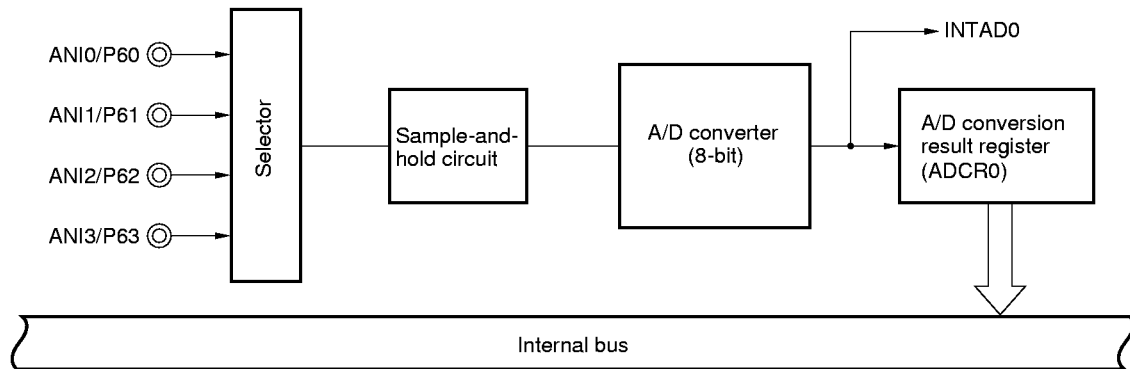


## 5.4 A/D Converter

Four-channel A/D converters with an 8-bit resolution are incorporated.

A/D conversion can be started only by software.

**Figure 5-5. A/D Converter Block Diagram**



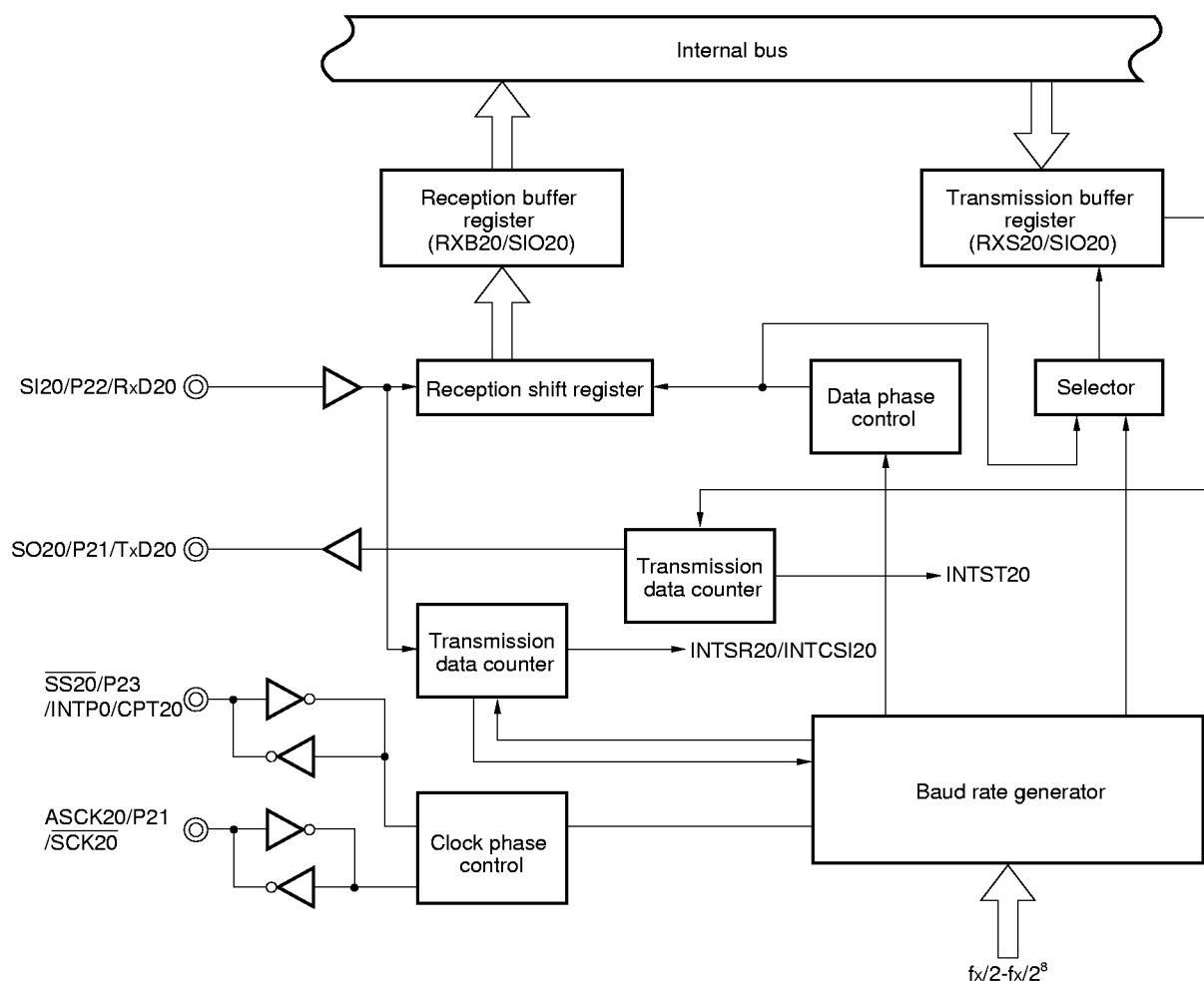
## 5.5 Serial Interface Channel

One-channel serial interface is incorporated.

Serial interface channel 2 supports the following two modes:

- Three-wire serial I/O mode : A function to select the clock phase or data phase is incorporated.
- Asynchronous serial interface (UART) mode : The dedicated baud rate generator is incorporated.

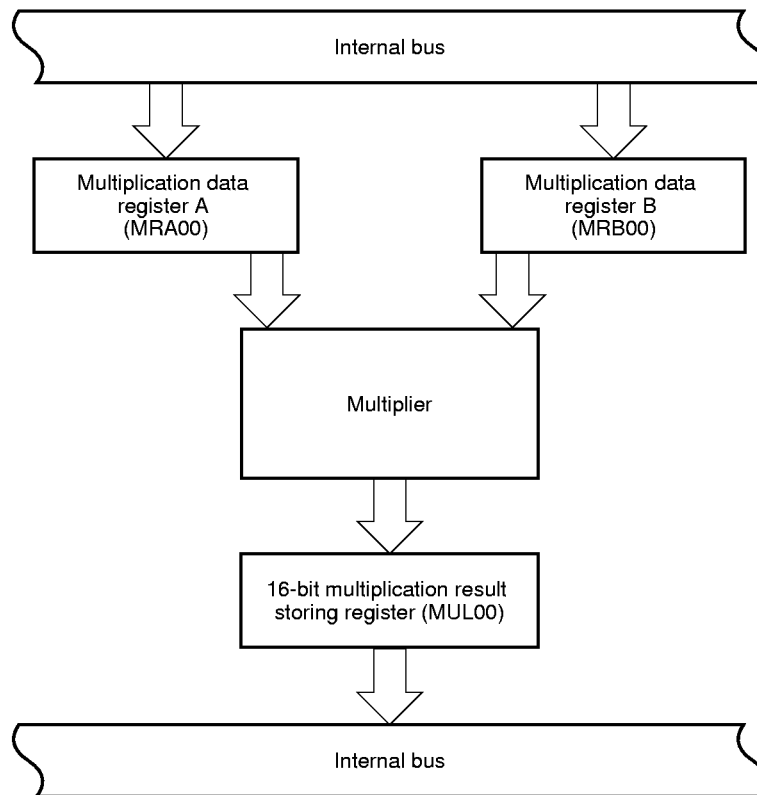
Figure 5-6. Block Diagram of Serial Interface Channel 2



## 5.6 Multiplier

Calculation of 16 bits (8 bits × 2) can be performed.

Figure 5-7. Multiplier Block Diagram



## 6. INTERRUPT FUNCTION

There are two types and 11 sources of interrupt function as shown below.

- Nonmaskable interrupt : 1 source
- Maskable interrupts : 10 sources

**Table 6-1. Interrupt Sources**

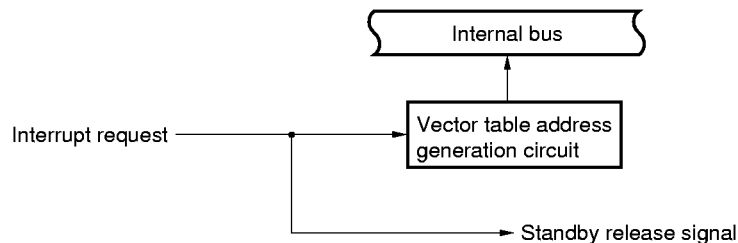
| Interrupt type        | Priority <sup>Note 1</sup> | Interrupt source |                                                                        | Internal/external | Vector table address | Basic configuration type <sup>Note 2</sup> |
|-----------------------|----------------------------|------------------|------------------------------------------------------------------------|-------------------|----------------------|--------------------------------------------|
|                       |                            | Name             | Trigger                                                                |                   |                      |                                            |
| Nonmaskable interrupt | -                          | INTWDT           | Watchdog timer overflow (when watchdog timer mode 1 is selected)       | Internal          | 0004H                | (A)                                        |
| Maskable              | 0                          | INTWDT           | Watchdog timer overflow (when the interval timer mode is selected)     |                   |                      | (B)                                        |
|                       | 1                          | INTP0            | Pin input edge detection                                               | External          | 0006H                | (C)                                        |
|                       | 2                          | INTP1            |                                                                        |                   | 0008H                |                                            |
|                       | 3                          | INTP2            |                                                                        |                   | 000AH                |                                            |
|                       | 4                          | INTSR20          | End of UART reception on serial interface channel 2                    | Internal          | 000CH                | (B)                                        |
|                       |                            | INTCSI20         | End of three-wire SIO transfer reception on serial interface channel 2 |                   |                      |                                            |
|                       | 5                          | INTST20          | End of UART transmission on serial interface channel 2                 |                   | 000EH                |                                            |
|                       | 6                          | INTTM80          | Generation of match signal for 8-bit timer/event counter 80            |                   | 0010H                |                                            |
|                       | 7                          | INTTM20          | Generation of match signal for 16-bit timer 20                         |                   | 0012H                |                                            |
|                       | 8                          | INTAD0           | A/D conversion completion signal                                       |                   | 0014H                |                                            |

**Notes** 1. The priority regulates which maskable interrupt is higher, when two or more maskable interrupts are requested simultaneously. Zero signifies the highest priority, while 8 is the lowest.

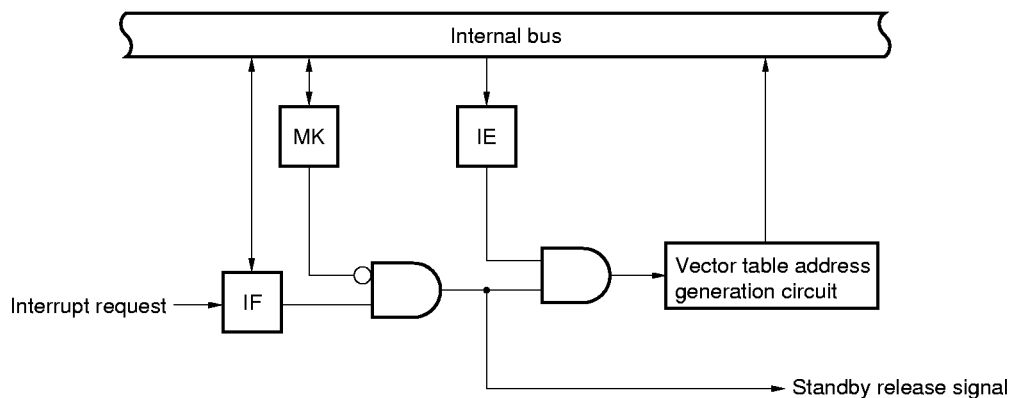
2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Functions

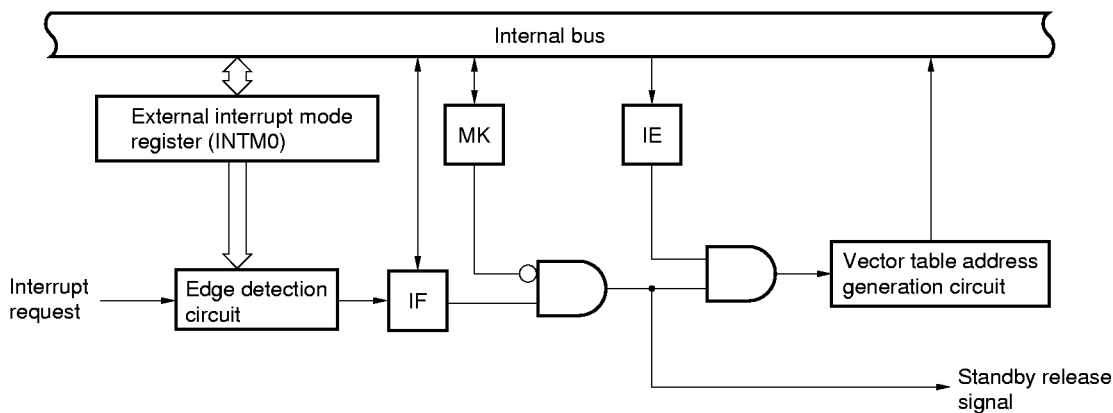
(A) Internal nonmaskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



IF : Interrupt request flag

IE : Interrupt enable flag

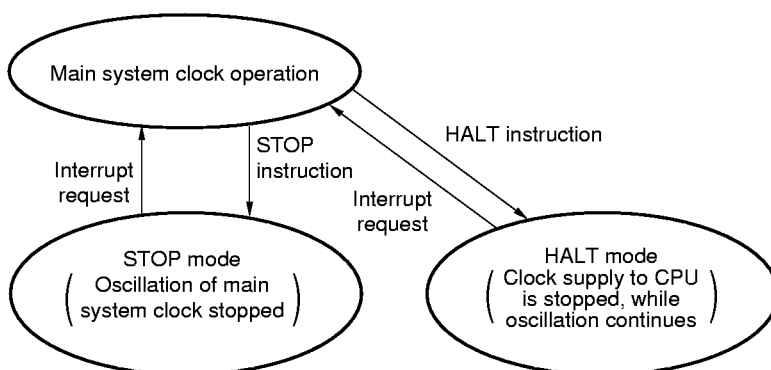
MK : Interrupt mask flag

## 7. STANDBY FUNCTION

The standby function is a function to reduce current consumption and there are two kinds of standby function as shown below.

- **HALT mode :** Stops the operating clock of the CPU. Intermittent operation together with normal operation can reduce average current consumption.
- **STOP mode:** Stops oscillation of the main system clock. Stops the entire operation by the main system clock and minimizes power consumption.

Figure 7-1. Standby Function



## 8. RESET FUNCTION

The system is reset in the following two ways.

- External reset by RESET pin
- Internal reset by detection of inadvertent program loop time of watchdog timer

## 9. INSTRUCTION SET

### (1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

| 2nd operand<br>1st operand | #byte                                                        | A                   | r                                                                                                   | sfr        | saddr                                                               | laddr16                                                             | PSW | [DE]       | [HL]                                                                | [HL + byte]                                                         | \$addr16 | 1                          | None        |
|----------------------------|--------------------------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|-----|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|----------|----------------------------|-------------|
| A                          | ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP        |                     | MOV <sup>Note</sup><br>XCH <sup>Note</sup><br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV | MOV<br>XCH | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP |          | ROR<br>ROL<br>RORC<br>ROLC |             |
| r                          | MOV                                                          | MOV <sup>Note</sup> |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            | INC<br>DEC  |
| B, C                       |                                                              |                     |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     | DBNZ     |                            |             |
| sfr                        | MOV                                                          | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |             |
| saddr                      | MOV<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     | DBNZ     |                            | INC<br>DEC  |
| laddr16                    |                                                              | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |             |
| PSW                        | MOV                                                          | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            | PUSH<br>POP |
| [DE]                       |                                                              | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |             |
| [HL]                       |                                                              | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |             |
| [HL + byte]                |                                                              | MOV                 |                                                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |             |

**Note** Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

| 2nd operand<br>1st operand | #word                | AX                   | rp <sup>Note</sup> | saddrp | SP   | None                        |
|----------------------------|----------------------|----------------------|--------------------|--------|------|-----------------------------|
| AX                         | ADDW<br>SUBW<br>CMPW |                      | MOVW<br>XCHW       | MOVW   | MOVW |                             |
| rp                         | MOVW                 | MOVW <sup>Note</sup> |                    |        |      | INCW<br>DECW<br>PUSH<br>POP |
| saddrp                     |                      | MOVW                 |                    |        |      |                             |
| SP                         |                      | MOVW                 |                    |        |      |                             |

**Note** Only when rp = BC, DE, HL

(3) Bit manipulation instructions

SET1, CLR1, NOT1, BT, BF

| 2nd operand<br>1st operand | \$addr16 | None                 |
|----------------------------|----------|----------------------|
| A.bit                      | BT<br>BF | SET1<br>CLR1         |
| sfr.bit                    | BT<br>BF | SET1<br>CLR1         |
| saddr.bit                  | BT<br>BF | SET1<br>CLR1         |
| PSW.bit                    | BT<br>BF | SET1<br>CLR1         |
| [HL] .bit                  |          | SET1<br>CLR1         |
| CY                         |          | SET1<br>CLR1<br>NOT1 |

**(4) Call instructions/ branch instructions**

CALL, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, DBNZ

| 2nd operand<br>1st operand | AX | !addr16    | [addr5] | \$addr16                     |
|----------------------------|----|------------|---------|------------------------------|
| Basic instruction          | BR | CALL<br>BR | CALLT   | BR<br>BC<br>BNC<br>BZ<br>BNZ |
| Complex instruction        |    |            |         | DBNZ                         |

**(5) Other instructions**

RET, RETI, NOP, EI, DI, HALT, STOP

## 10. ELECTRICAL CHARACTERISTICS (TARGET VALUES)

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)

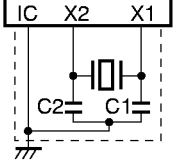
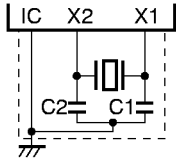
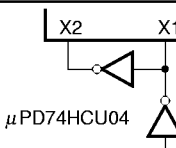
| Parameter                     | Symbol           | Conditions                       |                                  | Rated value                   | Unit |
|-------------------------------|------------------|----------------------------------|----------------------------------|-------------------------------|------|
| Supply voltage                | V <sub>DD</sub>  |                                  |                                  | -0.3 to +7.0                  | V    |
| Input voltage                 | V <sub>I1</sub>  | Pins other than those for port 5 |                                  | -0.3 to V <sub>DD</sub> + 0.3 | V    |
|                               | V <sub>I2</sub>  | P50-P53                          | With N-ch open drain             | -0.3 to +13                   | V    |
|                               |                  |                                  | With a built-in pull-up resistor | -0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output voltage                | V <sub>O</sub>   |                                  |                                  | -0.3 to V <sub>DD</sub> + 0.3 | V    |
| High-level output current     | I <sub>OH</sub>  | Each pin                         |                                  | -10                           | mA   |
|                               |                  | Total for all pins               |                                  | -30                           | mA   |
| Low-level output current      | I <sub>OL</sub>  | Each pin                         |                                  | 30                            | mA   |
|                               |                  | Total for all pins               |                                  | 160                           | mA   |
| Operating ambient temperature | T <sub>A</sub>   |                                  |                                  | -40 to +85                    | °C   |
| Storage temperature           | T <sub>stg</sub> |                                  |                                  | -65 to +150                   | °C   |

**Caution** Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

**Remark** The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

# CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATION CIRCUIT

(T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

| Resonator         | Recommended circuit                                                               | Parameter                                                          | Conditions                                                          | MIN. | TYP. | MAX. | Unit |
|-------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------|------|------|------|------|
| Ceramic resonator |  | Oscillator frequency (f <sub>x</sub> ) <sup>Note 1</sup>           | V <sub>DD</sub> = oscillation voltage range                         | 1.0  |      | 5.0  | MHz  |
|                   |                                                                                   | Oscillation settling time <sup>Note 2</sup>                        | After V <sub>DD</sub> reaches MIN. of the oscillation voltage range |      |      | 4    | ms   |
| Crystal           |  | Oscillator frequency (f <sub>x</sub> ) <sup>Note 1</sup>           |                                                                     | 1.0  |      | 5.0  | MHz  |
|                   |                                                                                   | Oscillation settling time <sup>Note 2</sup>                        | V <sub>DD</sub> = 4.5 to 5.5 V                                      |      |      | 10   | ms   |
|                   |                                                                                   |                                                                    |                                                                     |      |      | 30   |      |
| External clock    |  | X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>             |                                                                     | 1.0  |      | 5.0  | MHz  |
|                   |                                                                                   | X1 input high/low level width (t <sub>xH</sub> , t <sub>xL</sub> ) |                                                                     | 100  |      | 500  | ns   |

**Notes** 1. Only the characteristic of the oscillation circuit is indicated. See the description of the AC characteristic for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected.

**Caution** When using the main system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- Keep the wiring as short as possible.
- Do not allow signal wires to cross one another.
- Keep the wiring away from wires that carry a high, non-stable current.
- Keep the grounding point of the capacitors at the same level as V<sub>ss</sub>.
- Do not connect the grounding point to a grounding wire that carries a high current.
- Do not extract a signal from the oscillation circuit.

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

| Parameter                         | Symbol            | Conditions                                                |                                  | MIN.                                                                 | TYP.               | MAX.               | Unit |
|-----------------------------------|-------------------|-----------------------------------------------------------|----------------------------------|----------------------------------------------------------------------|--------------------|--------------------|------|
| Low-level output current          | I <sub>OL</sub>   | Each pin                                                  |                                  |                                                                      |                    | Undefined          | mA   |
|                                   |                   | Total for all pins                                        |                                  |                                                                      |                    | 80                 | mA   |
| High-level output current         | I <sub>OH</sub>   | Each pin                                                  |                                  |                                                                      |                    | Undefined          | mA   |
|                                   |                   | Total for all pins                                        |                                  |                                                                      |                    | -15                | mA   |
| High-level input voltage          | V <sub>IH1</sub>  | P00-P03, P10, P11, P60-P63                                |                                  | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0.7V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0.9V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   | V <sub>IH2</sub>  | P50-P53                                                   | With N-ch open drain             | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0.7V <sub>DD</sub> | 12                 | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0.9V <sub>DD</sub> | 12                 | V    |
|                                   |                   |                                                           | With a built-in pull-up resistor | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0.7V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0.9V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   | V <sub>IH3</sub>  | RESET, P20-P25, P40-P45                                   |                                  | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0.8V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0.9V <sub>DD</sub> | V <sub>DD</sub>    | V    |
|                                   | V <sub>IH4</sub>  | X1, X2                                                    |                                  | V <sub>DD</sub> - 0.1                                                |                    | V <sub>DD</sub>    | V    |
| Low-level input voltage           | V <sub>IL1</sub>  | P00-P03, P10, P11, P60-P63                                |                                  | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0                  | 0.3V <sub>DD</sub> | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0                  | 0.1V <sub>DD</sub> | V    |
|                                   | V <sub>IL2</sub>  | P50-P53                                                   |                                  | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0                  | 0.3V <sub>DD</sub> | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0                  | 0.1V <sub>DD</sub> | V    |
|                                   | V <sub>IL3</sub>  | RESET, P20-P25, P40-P45                                   |                                  | V <sub>DD</sub> = 2.7 to 5.5 V                                       | 0                  | 0.2V <sub>DD</sub> | V    |
|                                   |                   |                                                           |                                  |                                                                      | 0                  | 0.1V <sub>DD</sub> | V    |
|                                   | V <sub>IL4</sub>  | X1, X2                                                    |                                  | 0                                                                    |                    | 0.1                | V    |
| High-level output voltage         | V <sub>OH</sub>   | V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = -1 mA   |                                  | V <sub>DD</sub> - 1.0                                                |                    |                    | V    |
|                                   |                   | V <sub>DD</sub> = 1.8 to 5.5 V, I <sub>OH</sub> = -100 μA |                                  | V <sub>DD</sub> - 0.5                                                |                    |                    | V    |
| Low-level output voltage          | V <sub>OL1</sub>  | Pins other than those for port 5                          |                                  | V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 10 mA              |                    | 1.0                | V    |
|                                   |                   |                                                           |                                  | V <sub>DD</sub> = 1.8 to 5.5 V, I <sub>OL</sub> = 400 μA             |                    | 0.5                | V    |
|                                   | V <sub>OL2</sub>  | P50-P53                                                   |                                  | V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 10 mA              |                    | 1.0                | V    |
|                                   |                   |                                                           |                                  | V <sub>DD</sub> = 1.8 to 5.5 V, I <sub>OL</sub> = 1.6 mA             |                    | 0.4                | V    |
| High-level input leakage current  | I <sub>LIH1</sub> | V <sub>IN</sub> = V <sub>DD</sub>                         |                                  | Pins other than the X1 pin, X2 pin, or those for port 5              |                    | 3                  | μA   |
|                                   | I <sub>LIH2</sub> |                                                           |                                  | X1, X2                                                               |                    | 20                 | μA   |
|                                   | I <sub>LIH3</sub> | V <sub>IN</sub> = 12 V                                    |                                  | P50-P53 (N-channel open drain)                                       |                    | 20                 | μA   |
| Low-level input leakage current   | I <sub>LIL1</sub> | V <sub>IN</sub> = 0 V                                     |                                  | Pins other than the X1 pin, X2 pin, or those for port 5              |                    | -3                 | μA   |
|                                   | I <sub>LIL2</sub> |                                                           |                                  | X1, X2                                                               |                    | -20                | μA   |
|                                   | I <sub>LIL3</sub> |                                                           |                                  | P50-P53 (N-channel open drain)<br>During input instruction execution |                    | -30                | μA   |
| High-level output leakage current | I <sub>LOH</sub>  | V <sub>OUT</sub> = V <sub>DD</sub>                        |                                  |                                                                      |                    | 3                  | μA   |
| Low-level output leakage current  | I <sub>LOL</sub>  | V <sub>OUT</sub> = 0 V                                    |                                  |                                                                      |                    | -3                 | μA   |

**Remark** The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

**DC CHARACTERISTICS** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                              | Symbol           | Conditions                                                  |                                                  | MIN. | TYP. | MAX. | Unit |
|----------------------------------------|------------------|-------------------------------------------------------------|--------------------------------------------------|------|------|------|------|
| Software-specified pull-up resistor    | R <sub>1</sub>   | V <sub>IN</sub> = 0 V, for pins other than those for port 5 |                                                  | 50   | 100  | 200  | kΩ   |
| Mask option-specified pull-up resistor | R <sub>2</sub>   | V <sub>IN</sub> = 0 V, P50-P53                              |                                                  | 15   | 30   | 60   | kΩ   |
| Power supply current <sup>Note 1</sup> | I <sub>DD1</sub> | 5.0-MHz crystal oscillation operating mode                  | V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup> |      | 5.5  | 16.5 | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 3.0 V ± 10 %                   |      | 0.7  | 2.1  | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 2.0 V ± 10 %                   |      | 0.4  | 1.2  | mA   |
|                                        | I <sub>DD2</sub> | 5.0-MHz crystal oscillation HALT mode                       | V <sub>DD</sub> = 5.0 V ± 10 %                   |      | 1.2  | 3.6  | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 3.0 V ± 10 %                   |      | 0.5  | 1.5  | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 2.0 V ± 10 %                   |      | 0.3  | 0.9  | mA   |
|                                        | I <sub>DD3</sub> | STOP mode                                                   | V <sub>DD</sub> = 5.0 V ± 10 %                   |      | 0.1  | 30   | μA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 3.0 V ± 10 %                   |      | 0.05 | 10   | μA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 2.0 V ± 10 %                   |      | 0.05 | 10   | μA   |
|                                        | I <sub>DD4</sub> | 5.0-MHz crystal oscillation A/D operating mode              | V <sub>DD</sub> = 5.0 V ± 10 %                   |      | 6.1  | 18.3 | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 3.0 V ± 10 %                   |      | 1.3  | 2.9  | mA   |
|                                        |                  |                                                             | V <sub>DD</sub> = 2.0 V ± 10 %                   |      | 1.0  | 3.0  | mA   |

**Notes** 1. The power supply current does not include  $AV_{DD}$  or the port current (including the current flowing through the built-in pull-up resistor).

2. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H.)

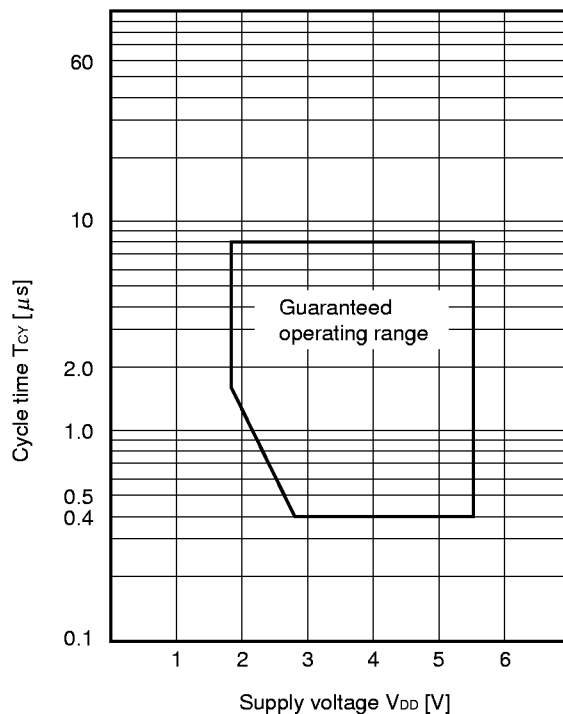
**Remark** The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

# AC CHARACTERISTICS

## (1) Basic operations (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

| Parameter                                             | Symbol            | Conditions                     | MIN.                           | TYP. | MAX. | Unit |
|-------------------------------------------------------|-------------------|--------------------------------|--------------------------------|------|------|------|
| Cycle time<br>(minimum instruction<br>execution time) | T <sub>CY</sub>   | V <sub>DD</sub> = 2.7 to 5.5 V | 0.4                            |      | 8    | μs   |
|                                                       |                   |                                | 1.6                            |      | 8    | μs   |
| Tl80 input high/low<br>level width                    | t <sub>TIH</sub>  | V <sub>DD</sub> = 2.7 to 5.5 V | 0.1                            |      |      | μs   |
|                                                       | t <sub>TIL</sub>  |                                | 1.8                            |      |      | μs   |
| Tl80 input<br>frequency                               | f <sub>TI</sub>   | V <sub>DD</sub> = 2.7 to 5.5 V | 0                              |      | 4    | MHz  |
|                                                       |                   |                                | 0                              |      | 275  | kHz  |
| Interrupt input<br>high/low level width               | t <sub>INTH</sub> | INTP0-INTP2                    | V <sub>DD</sub> = 2.7 to 5.5 V | 10   |      | μs   |
|                                                       | t <sub>INTL</sub> |                                |                                | 20   |      | μs   |
| RESET low level<br>width                              | t <sub>RSL</sub>  | V <sub>DD</sub> = 2.7 to 5.5 V | 10                             |      |      | μs   |
|                                                       |                   |                                | 20                             |      |      | μs   |

T<sub>CY</sub> vs V<sub>DD</sub> (main system clock)



(2) Serial interface channel 2 ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

(i) Three-wire serial I/O mode ( $\overline{SCK20}$ ...Internal clock output)

| Parameter                                               | Symbol                   | Conditions                                           | MIN.                      | TYP. | MAX.  | Unit |
|---------------------------------------------------------|--------------------------|------------------------------------------------------|---------------------------|------|-------|------|
| $\overline{SCK20}$ cycle time                           | $t_{KCY1}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 800                       |      |       | ns   |
|                                                         |                          |                                                      | 3 200                     |      |       | ns   |
| $\overline{SCK20}$ high/low level width                 | $t_{KH1}$ ,<br>$t_{KL1}$ | $V_{DD} = 2.7$ to $5.5$ V                            | $t_{KCY1}/2-50$           |      |       | ns   |
|                                                         |                          |                                                      | $t_{KCY1}/2-150$          |      |       | ns   |
| SI20 setup time<br>(for $\overline{SCK20}$ latch edge)  | $t_{SIK1}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 150                       |      |       | ns   |
|                                                         |                          |                                                      | 500                       |      |       | ns   |
| SI20 hold time<br>(for $\overline{SCK20}$ latch edge)   | $t_{KSI1}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 400                       |      |       | ns   |
|                                                         |                          |                                                      | 600                       |      |       | ns   |
| Delay from $\overline{SCK20}$ shift edge to SO20 output | $t_{KSO1}$               | $R = 1$ k $\Omega$ ,<br>$C = 100$ pF <sup>Note</sup> | $V_{DD} = 2.7$ to $5.5$ V | 0    | 250   | ns   |
|                                                         |                          |                                                      |                           | 0    | 1 000 | ns   |

**Note** R and C are the resistance and capacitance of the SO20 output line, respectively.

(ii) Three-wire serial I/O mode ( $\overline{SCK20}$ ...External clock output)

| Parameter                                                                     | Symbol                   | Conditions                                           | MIN.                      | TYP. | MAX.  | Unit |
|-------------------------------------------------------------------------------|--------------------------|------------------------------------------------------|---------------------------|------|-------|------|
| $\overline{SCK20}$ cycle time                                                 | $t_{KCY2}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 800                       |      |       | ns   |
|                                                                               |                          |                                                      | 3 200                     |      |       | ns   |
| $\overline{SCK20}$ high/low level width                                       | $t_{KH2}$ ,<br>$t_{KL2}$ | $V_{DD} = 2.7$ to $5.5$ V                            | 400                       |      |       | ns   |
|                                                                               |                          |                                                      | 1 600                     |      |       | ns   |
| SI20 setup time<br>(for $\overline{SCK20}$ latch edge)                        | $t_{SIK2}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 100                       |      |       | ns   |
|                                                                               |                          |                                                      | 150                       |      |       | ns   |
| SI20 hold time<br>(for $\overline{SCK20}$ latch edge)                         | $t_{KSI2}$               | $V_{DD} = 2.7$ to $5.5$ V                            | 400                       |      |       | ns   |
|                                                                               |                          |                                                      | 600                       |      |       | ns   |
| Delay from $\overline{SCK20}$ shift edge to SO20 output                       | $t_{KSO2}$               | $R = 1$ k $\Omega$ ,<br>$C = 100$ pF <sup>Note</sup> | $V_{DD} = 2.7$ to $5.5$ V | 0    | 300   | ns   |
|                                                                               |                          |                                                      |                           | 0    | 1 000 | ns   |
| SO20 setup time<br>(for $\overline{SS20}$ ↓ when $\overline{SS20}$ is used)   | $t_{KAS2}$               | $V_{DD} = 2.7$ to $5.5$ V                            |                           |      | 120   | ns   |
|                                                                               |                          |                                                      |                           |      | 400   | ns   |
| SO20 disable time<br>(for $\overline{SS20}$ ↑ when $\overline{SS20}$ is used) | $t_{KDS2}$               | $V_{DD} = 2.7$ to $5.5$ V                            |                           |      | 240   | ns   |
|                                                                               |                          |                                                      |                           |      | 800   | ns   |

**Note** R and C are the resistance and capacitance of the SO20 output line, respectively.

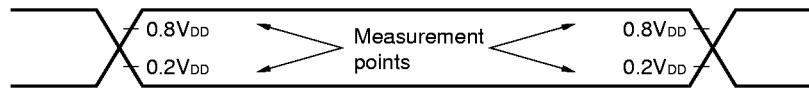
(iii) UART mode (Internal clock output)

| Parameter     | Symbol | Conditions                | MIN. | TYP. | MAX.   | Unit |
|---------------|--------|---------------------------|------|------|--------|------|
| Transfer rate |        | $V_{DD} = 2.7$ to $5.5$ V |      |      | 78 125 | bps  |
|               |        |                           |      |      | 19 531 | bps  |

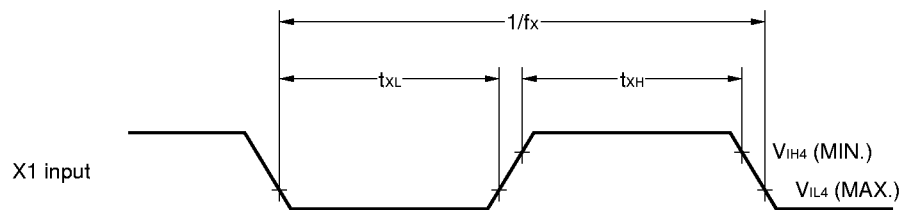
(iv) UART mode (external clock input)

| Parameter                        | Symbol                                 | Conditions                     | MIN.  | TYP. | MAX.   | Unit |
|----------------------------------|----------------------------------------|--------------------------------|-------|------|--------|------|
| ASCK20 cycle time                | t <sub>KCY3</sub>                      | V <sub>DD</sub> = 2.7 to 5.5 V | 800   |      |        | ns   |
|                                  |                                        |                                | 3 200 |      |        | ns   |
| ASCK20 high/low level width      | t <sub>KH3</sub> ,<br>t <sub>KL3</sub> | V <sub>DD</sub> = 2.7 to 5.5 V | 400   |      |        | ns   |
|                                  |                                        |                                | 1 600 |      |        | ns   |
| Transfer rate                    |                                        | V <sub>DD</sub> = 2.7 to 5.5 V |       |      | 39 063 | bps  |
|                                  |                                        |                                |       |      | 9 766  | bps  |
| ASCK20 rising time, falling time | t <sub>R</sub> ,<br>t <sub>F</sub>     |                                |       |      | 1      | μs   |

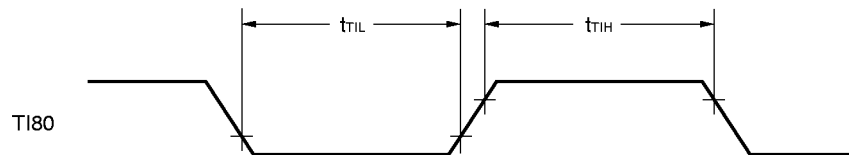
**AC TIMING MEASUREMENT POINTS (except the X1 and XT1 inputs)**



**CLOCK TIMING**

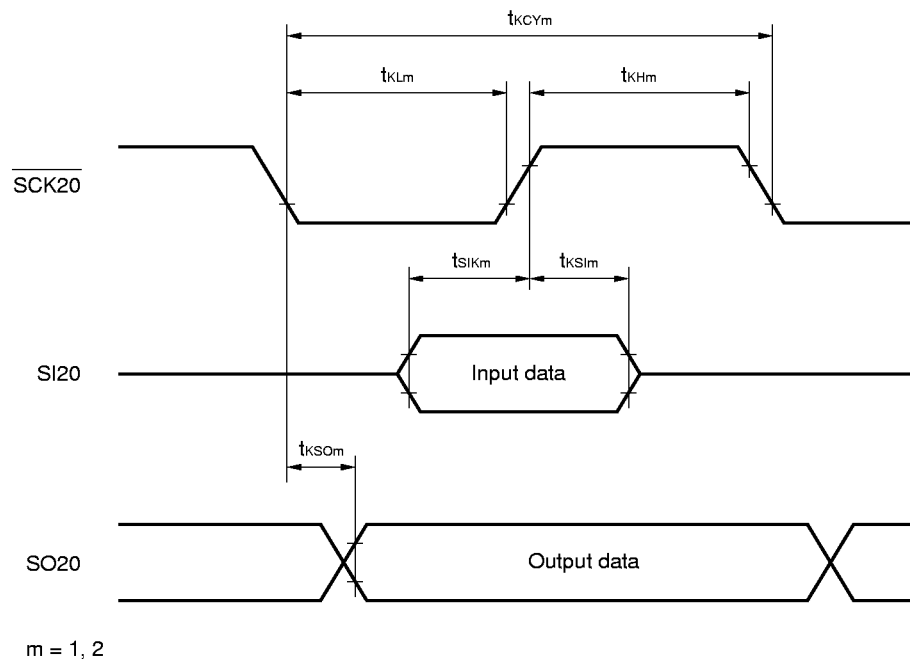


**TI TIMING**

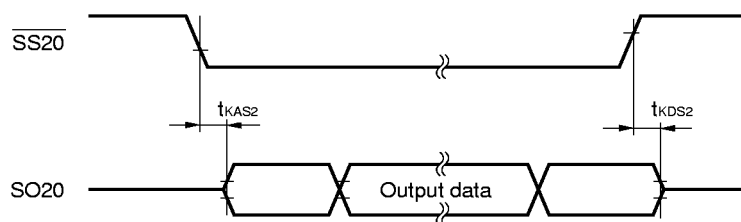


# SERIAL TRANSFER TIMING

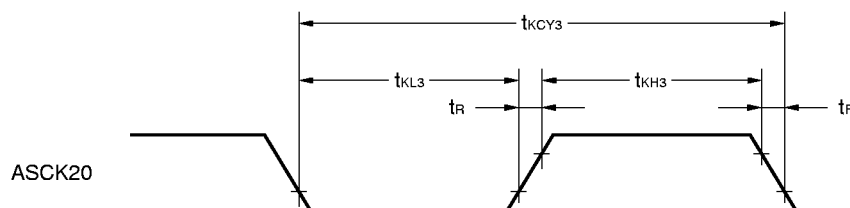
## Three-Wire Serial I/O Mode:



## Three-wire serial I/O mode (when $\overline{\text{SS20}}$ is used):



## UART Mode (External Clock Input):



**A/D CONVERTER CHARACTERISTICS** ( $T_A = -40$  to  $+85$  °C,  $AV_{DD} = V_{DD} = 1.8$  to  $5.5$  V,  $AV_{SS} = V_{SS} = 0$  V)

| Item                                      | Symbol      | Conditions | MIN.      | TYP. | MAX.      | Unit       |
|-------------------------------------------|-------------|------------|-----------|------|-----------|------------|
| Resolution                                |             |            | 8         | 8    | 8         | bit        |
| Total error <sup>Note</sup>               |             |            |           |      | 0.6       | %          |
| Conversion time                           | $T_{CONV}$  |            | Undefined |      | Undefined | $\mu$ s    |
| Analog input voltage                      | $V_{IAN}$   |            | 0         |      | $AV_{DD}$ | V          |
| Resistor between $AV_{REF}$ and $AV_{SS}$ | $R_{AIREF}$ |            |           | 46.9 |           | k $\Omega$ |

**Note** No quantization error ( $\pm 1/2$  LSB) is included.

**DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA HOLD CHARACTERISTICS**

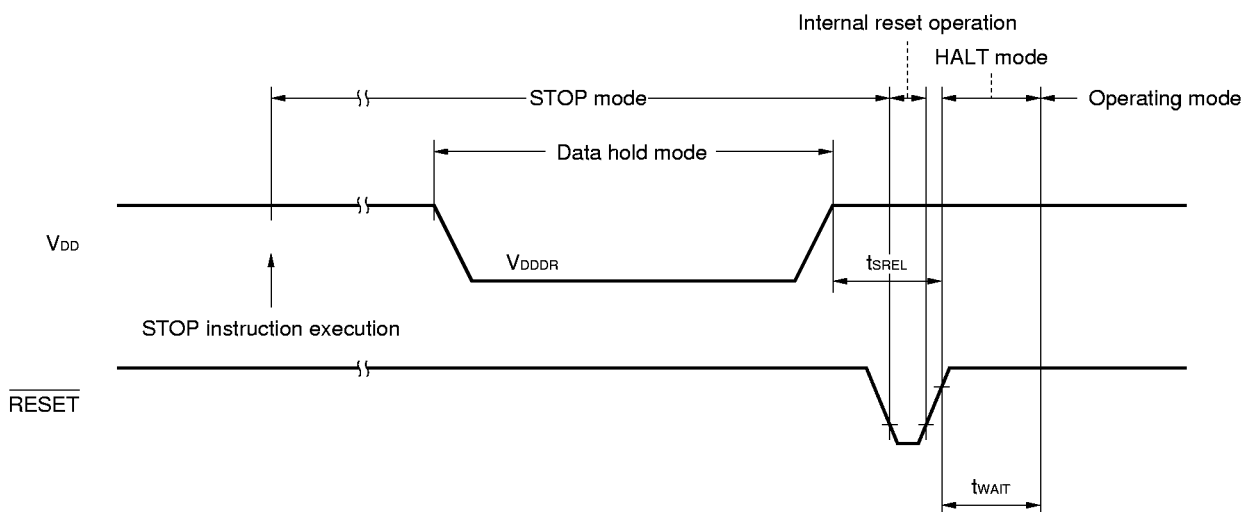
( $T_A = -40$  to  $+85$  °C)

| Item                      | Symbol     | Conditions                  | MIN. | TYP.         | MAX. | Unit    |
|---------------------------|------------|-----------------------------|------|--------------|------|---------|
| Data hold supply voltage  | $V_{DDDR}$ |                             | 1.8  |              | 5.5  | V       |
| Release signal set time   | $t_{SREL}$ |                             | 0    |              |      | $\mu$ s |
| Oscillation settling time | $t_{WAIT}$ | Reset by $\overline{RESET}$ |      | $2^{15}/f_x$ |      | ms      |
|                           |            | Reset by interrupt          |      | <b>Note</b>  |      | ms      |

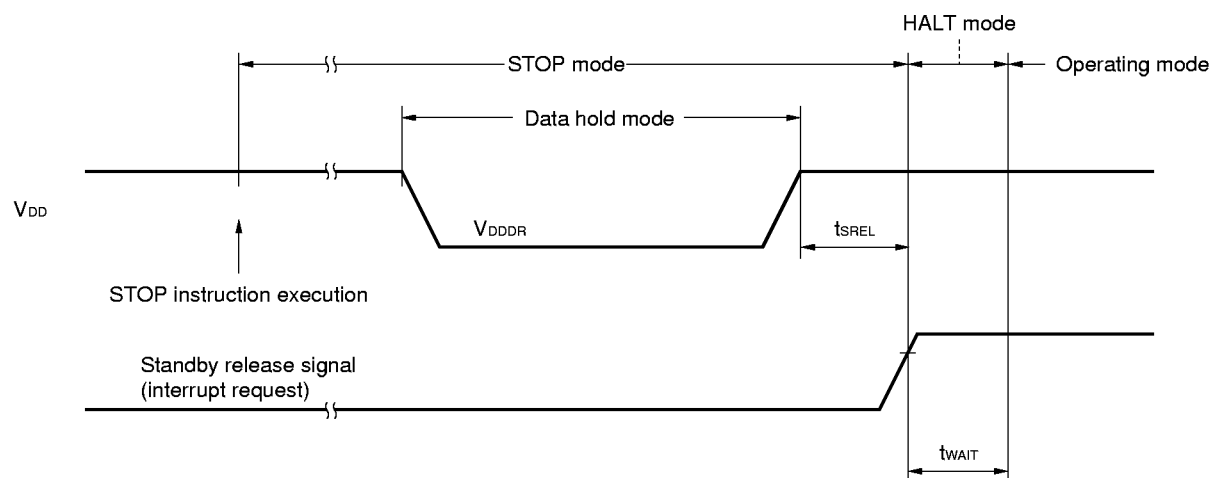
**Note**  $2^{12}/f_x$ ,  $2^{15}/f_x$ , or  $2^{17}/f_x$  can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register.

**Remark**  $f_x$ : Main system clock oscillation frequency

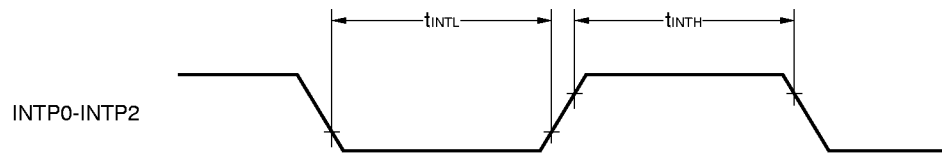
**DATA HOLD TIMING (STOP mode release by RESET)**



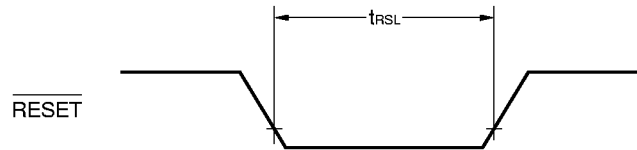
**DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)**



**INTERRUPT INPUT TIMING**

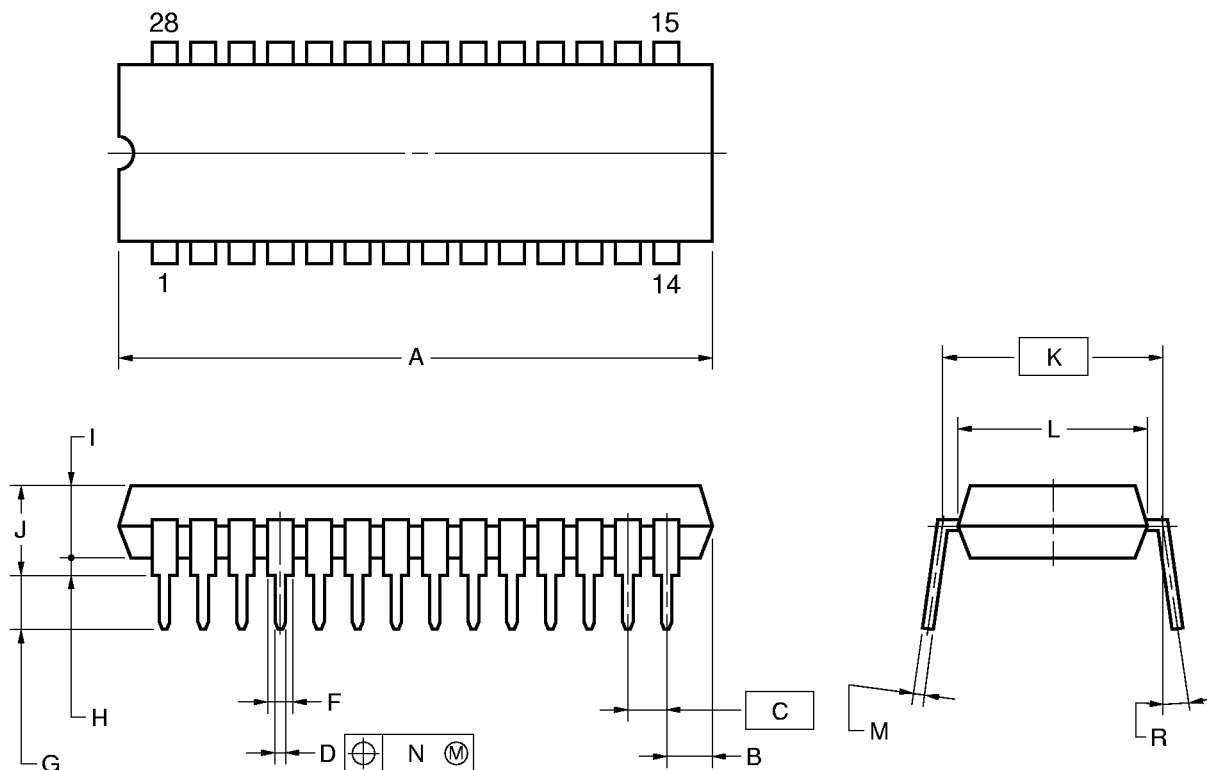


**RESET INPUT TIMING**



# 11. PACKAGE DRAWINGS

## 28PIN PLASTIC SHRINK DIP (400 mil)



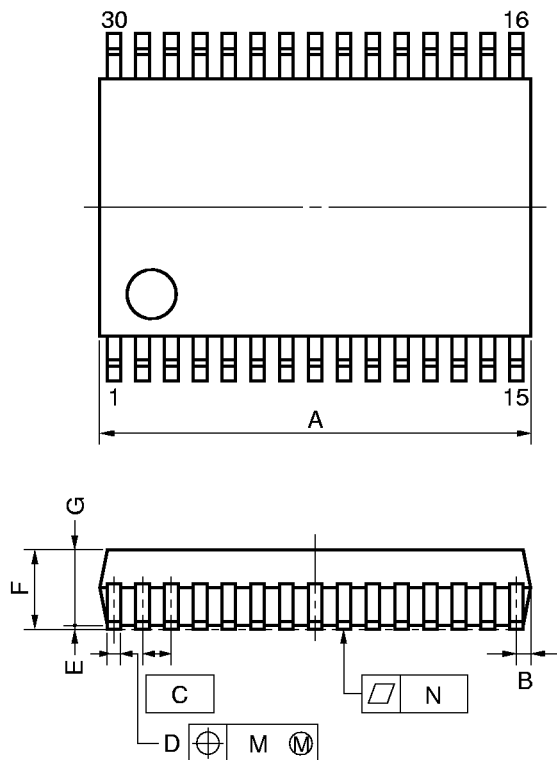
### NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

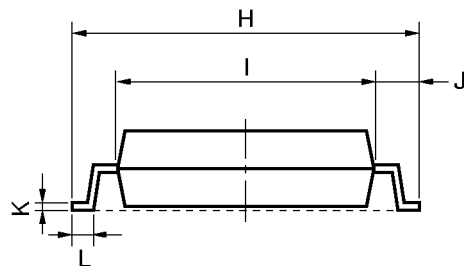
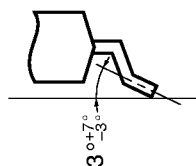
| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 28.46 MAX.                             | 1.121 MAX.                                |
| B    | 2.67 MAX.                              | 0.106 MAX.                                |
| C    | 1.778 (T.P.)                           | 0.070 (T.P.)                              |
| D    | 0.50±0.10                              | 0.020 <sup>+0.004</sup> <sub>-0.005</sub> |
| F    | 0.9 MIN.                               | 0.035 MIN.                                |
| G    | 3.2±0.3                                | 0.126±0.012                               |
| H    | 0.51 MIN.                              | 0.020 MIN.                                |
| I    | 4.31 MAX.                              | 0.170 MAX.                                |
| J    | 5.08 MAX.                              | 0.200 MAX.                                |
| K    | 10.16 (T.P.)                           | 0.400 (T.P.)                              |
| L    | 8.6                                    | 0.339                                     |
| M    | 0.25 <sup>+0.10</sup> <sub>-0.05</sub> | 0.010 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.17                                   | 0.007                                     |
| R    | 0~15°                                  | 0~15°                                     |

P28C-70-400A-1

30 PIN PLASTIC SHRINK SOP (300 mil)



detail of lead end



**NOTE**

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

P30GS-65-300B-1

| ITEM | MILLIMETERS                 | INCHES                         |
|------|-----------------------------|--------------------------------|
| A    | 10.11 MAX.                  | 0.398 MAX.                     |
| B    | 0.51 MAX.                   | 0.020 MAX.                     |
| C    | 0.65 (T.P.)                 | 0.026 (T.P.)                   |
| D    | 0.30 <sup>+0.10/-0.05</sup> | 0.012 <sup>+0.004/-0.003</sup> |
| E    | 0.125±0.075                 | 0.005±0.003                    |
| F    | 2.0 MAX.                    | 0.079 MAX.                     |
| G    | 1.7±0.1                     | 0.067±0.004                    |
| H    | 8.1±0.2                     | 0.319±0.008                    |
| I    | 6.1±0.2                     | 0.240±0.008                    |
| J    | 1.0±0.2                     | 0.039 <sup>+0.009/-0.008</sup> |
| K    | 0.15 <sup>+0.10/-0.05</sup> | 0.006 <sup>+0.004/-0.002</sup> |
| L    | 0.5±0.2                     | 0.020 <sup>+0.008/-0.009</sup> |
| M    | 0.10                        | 0.004                          |
| N    | 0.10                        | 0.004                          |

## APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD789101, μPD789102, and μPD789104.

### LANGUAGE PROCESSING SOFTWARE

|                                       |                                                            |
|---------------------------------------|------------------------------------------------------------|
| RA78K0S <sup>Notes 1, 2, 3</sup>      | Assembler package common to the 78K/0S series              |
| CC78K0S <sup>Notes 1, 2, 3</sup>      | C compiler package common to the 78K/0S series             |
| DF789134 <sup>Notes 1, 2, 3, 7</sup>  | Device file for the μPD789134 sub-series                   |
| CC78K0S-L <sup>Notes 1, 2, 3, 7</sup> | C compiler library source file common to the 78K/0S series |

### FLASH MEMORY WRITE TOOLS

|                                             |                                             |
|---------------------------------------------|---------------------------------------------|
| Flashpro II <sup>Note 4</sup>               | Dedicated flash writer (formerly, Flashpro) |
| FA-28CT <sup>Note 4</sup>                   | Flash memory write adapter                  |
| Undetermined product name <sup>Note 4</sup> |                                             |

### DEBUGGING TOOLS

|                                             |                                                                                                                                                |
|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| ND-K910 <sup>Notes 4, 7</sup>               | In-circuit emulator for the μPD789134 sub-series<br>The ND-K910 incorporates the NS-78K9 screen debugger.                                      |
| IF-98D <sup>Note 4</sup>                    | This is an interface board, required when a PC-9800 series (other than a notebook type) are used as the host machine for the ND-K910.          |
| IF-PCD <sup>Note 4</sup>                    | This is an interface board, required when an IBM PC/AT or compatible (other than a notebook type) is used as the host machine for the ND-K910. |
| IF-CARD <sup>Note 4</sup>                   | This is an interface board, required when a PC-9800 notebook, IBM PC/AT notebook, or compatible is used as the host machine for the ND-K910.   |
| NP-28CT <sup>Note 4</sup>                   | Emulator probe for the 28-pin plastic shrink DIP (CT type)                                                                                     |
| Undetermined product name <sup>Note 4</sup> | Emulator probe for the 30-pin plastic shrink SOP (GS type)                                                                                     |
| NJ-535 <sup>Note 4</sup>                    | 100-/120-VAC adapter                                                                                                                           |
| NJ-550W <sup>Note 4</sup>                   | 100- to 240-VAC adapter                                                                                                                        |
| SM78K0S <sup>Notes 5, 6</sup>               | System simulator common to all 78K/0S series units                                                                                             |
| DF789134 <sup>Notes 5, 6, 7</sup>           | Device file for the μPD789134 sub-series                                                                                                       |

### REAL-TIME OS

|                                  |                          |
|----------------------------------|--------------------------|
| MX78K0S <sup>Notes 1, 2, 7</sup> | OS for the 78K/0S series |
|----------------------------------|--------------------------|

- Notes**
1. Based on the PC-9800 series (MS-DOS™)
  2. Based on the IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS)
  3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and NEWS™ (NEWS-OS™)
  4. Product manufactured by and available from Naito Densai Machida Seisakusho Co., Ltd. (044-822-3813).
  5. Based on the PC-9800 series (MS-DOS + Windows™)
  6. Based on the IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
  7. Under development

**Remark** The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789134.

## APPENDIX B RELATED DOCUMENTS

### DOCUMENTS RELATED TO DEVICES

| Document name                                             | Document No.  |               |
|-----------------------------------------------------------|---------------|---------------|
|                                                           | Japanese      | English       |
| μPD789101, 789102, 789104 Preliminary Product Information | U12815J       | This manual   |
| μPD78F9116 Preliminary Product Information                | To be created | To be created |
| μPD789134 Sub-Series User's Manual                        | To be created | To be created |
| 78K/0S Series User's Manual, Instruction                  | U11047J       | U11047E       |
| 78K/0S Series Instruction Summary Sheet                   | To be created | —             |
| 78K/0S Series Instruction Set                             | To be created | —             |

### DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUAL)

| Document name                         |                                                   | Document No. |         |
|---------------------------------------|---------------------------------------------------|--------------|---------|
|                                       |                                                   | Japanese     | English |
| RA78K0S Assembler Package             | Operation                                         | U11622J      | U11622E |
|                                       | Assembly Language                                 | U11599J      | U11599E |
|                                       | Structured Assembly Language                      | U11623J      | U11623E |
| CC78K/0S C Compiler                   | Operation                                         | U11816J      | U11816E |
|                                       | Language                                          | U11817J      | U11817E |
| SM78K0S System Simulator Windows Base | Reference                                         | U11489J      | U11489E |
| SM78K Series System Simulator         | External Parts User Open Interface Specifications | U10092J      | U10092E |

### DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUAL)

| Document name                | Document No.  |               |
|------------------------------|---------------|---------------|
|                              | Japanese      | English       |
| OS for 78K/0S Series MX78K0S | To be created | To be created |

**Caution** The above documents may be revised without notice. Use the latest versions when you design application systems.

**OTHER DOCUMENTS**

| Document name                                                                      | Document No. |          |
|------------------------------------------------------------------------------------|--------------|----------|
|                                                                                    | Japanese     | English  |
| IC PACKAGE MANUAL                                                                  | C10943X      |          |
| SMD Surface Mount Technology Manual                                                | C10535J      | C10535E  |
| Quality Grades on NEC Semiconductor Device                                         | C11531J      | C11531E  |
| NEC Semiconductor Device Reliability/Quality Control System                        | C10983J      | C10983E  |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892J      | C11892E  |
| Guide to Quality Assurance for Semiconductor Device                                | C11893J      | MEI-1202 |
| Guide for Products Related to Micro-Computer: Other Companies                      | U11416J      | —        |

**Caution** The above documents may be revised without notice. Use the latest versions when you design application systems.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.