M95040
M95020, M95010

4/2/1 Kbit Serial SPI Bus EEPROM With High Speed Clock

PRELIMINARY DATA

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage:
  - 4.5V to 5.5V for M950x0
  - 2.5V to 5.5V for M950x0-W
  - 1.8V to 3.6V for M950x0-S
- 5 MHz Clock Rate (maximum)
- Status Register
- BYTE and PAGE WRITE (up to 16 Bytes)
- Self-Timed Programming Cycle
- Adjustable Size Read-Only EEPROM Area
- Enhanced ESD Protection
- More than 1,000,000 Erase/Write Cycles
- More than 40 Year Data Retention

DESCRIPTION

These SPI-compatible electrically erasable programmable memory (EEPROM) devices are organized as 512 x 8 bits, 256 x 8 bits and 128 x 8 bits (for the M95040, M95020, M95010, respectively). They operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -S version of each device).
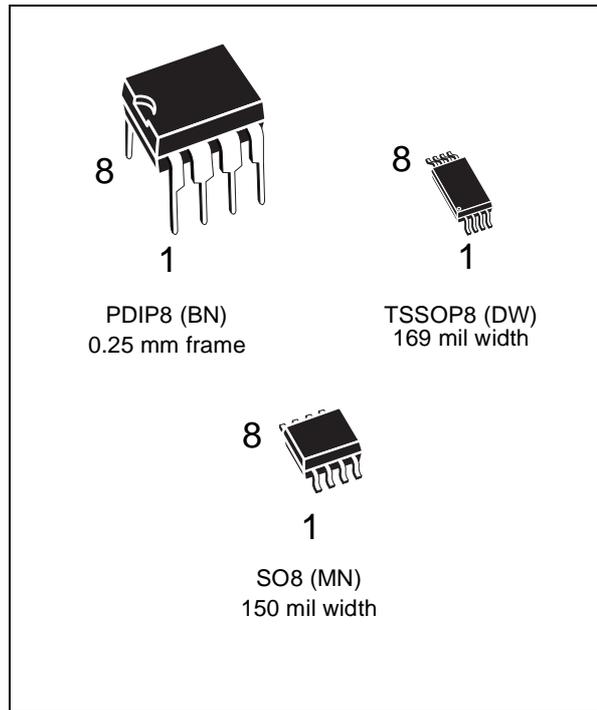

PDIP8 (BN)
0.25 mm frame
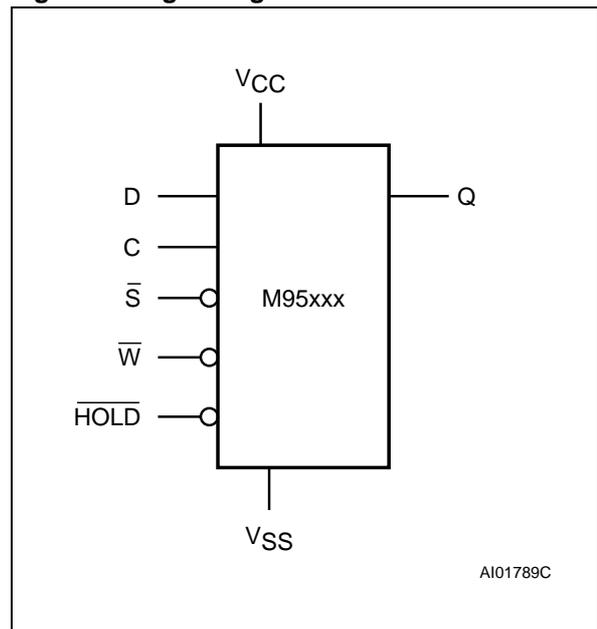
TSSOP8 (DW)
169 mil width

SO8 (MN)
150 mil width

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

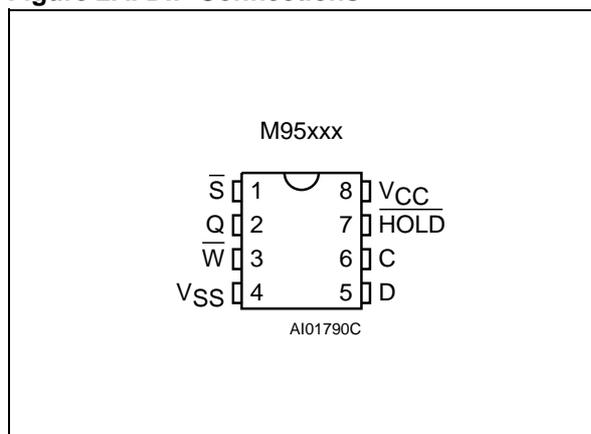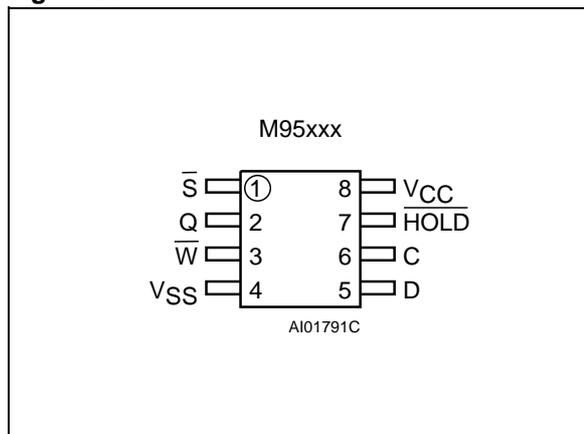AI01789C

Figure 2A. DIP Connections

Figure 2B. SO and TSSOP Connections

The M95040 and M95020, M95010 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Each device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in Table 1 and Figure 3.

The device is selected when Chip Select ($\overline{S}$) is taken Low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$). WRITE instructions are disabled by Write Protect ($\overline{W}$).

SIGNAL DESCRIPTION

V_{CC} must be held within the specified range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held High or Low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in Table 7). These signals are described next.

Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data bytes are shifted out on the falling edge of the Serial Clock (C).

Serial Data Input (D)

This input signal is used to transfer data serially into the device. Instructions, addresses, and input data bytes are shifted in on the rising edge of the Serial Clock (C).

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		−40 to 125	°C
T_{STG}	Storage Temperature		−65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP8: 10 seconds	260	°C
		SO8: 20 seconds (max) [2]	235	
		TSSOP8: 20 seconds (max) [2]	235	
V_O	Output Voltage		−0.3 to V_{CC}+0.6	V
V_I	Input Voltage		−0.3 to 6.5	V
V_{CC}	Supply Voltage		−0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. IPC/JEDEC J-STD-020A
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω).

Figure 3. Microcontroller and Memory Devices on the SPI Bus
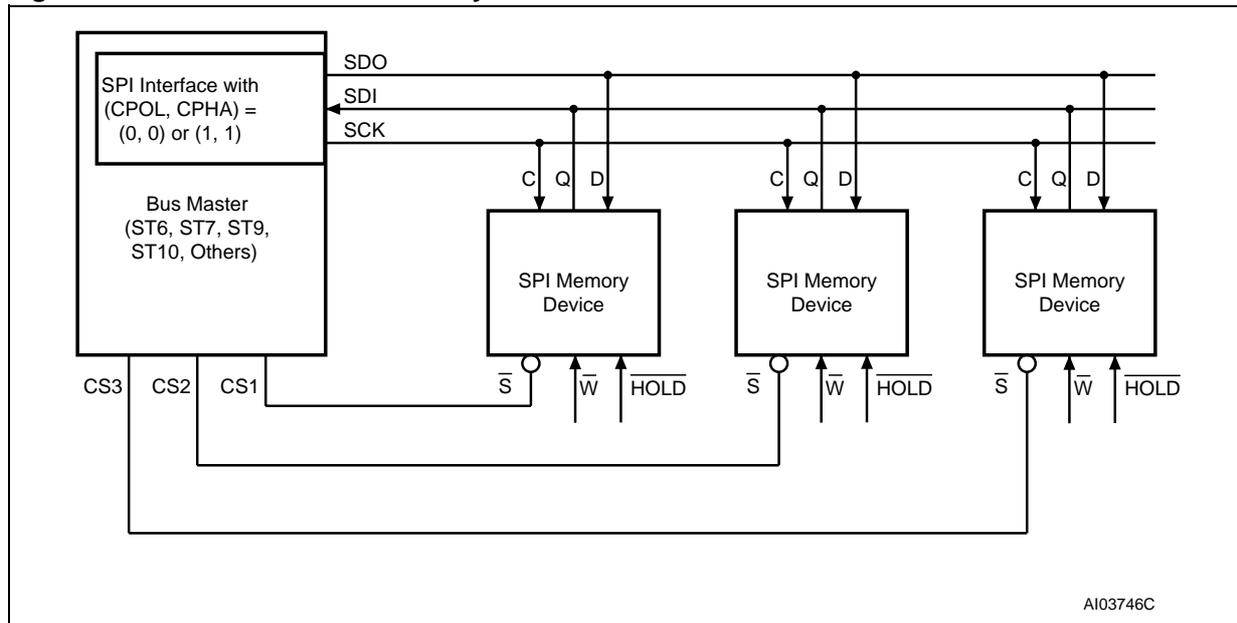
Serial Clock (C)

This input signal provides the timing for the serial interface.

Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected, and the Serial Data Output (Q) is high impedance.

Hold ($\overline{HOLD}$)

This input signal is used to pause temporarily any serial communications with the device, without losing bits that have already been passed on the serial bus.

Write Protect ($\overline{W}$)

This input signal is used to control whether the memory is write protected.

CONNECTING TO THE SPI BUS

These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes Low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3 shows three devices, connected to an MCU, on a SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, all the others being high impedance.

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

– CPOL=0, CPHA=0

– CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 4, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

– C remains at 0 for (CPOL=0, CPHA=0)

– C remains at 1 for (CPOL=1, CPHA=1)

Power-up

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. (These values are specified in Table 7).

During this time, the Chip Select ($\overline{S}$) must be allowed to follow the V_{CC} voltage. It must not be allowed to float, but should be connected to V_{CC} via a suitable pull-up resistor.

Figure 4. SPI Modes Supported by the Device
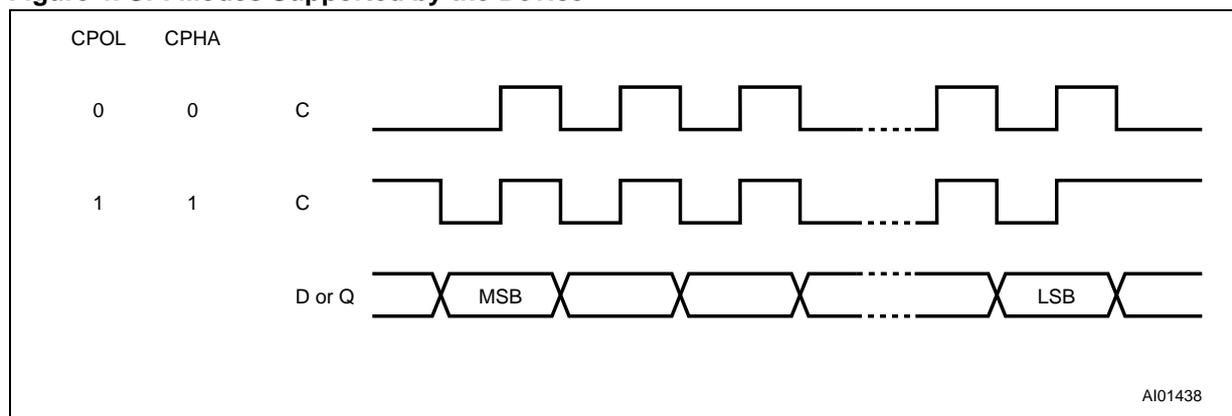
As a built in safety feature, Chip Select ($\overline{S}$) is edge sensitive as well as level sensitive. After Power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been High, prior to going Low to start the first operation.

Power-down

At Power-down, the device must be deselected. Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}.

ACTIVE POWER AND STAND-BY POWER MODES

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode. The device consumes I_{CC1}, as specified in Table 7.

When Chip Select ($\overline{S}$) is High, the device is disabled. If an Erase/Write cycle is not currently in progress, the device then goes in to the Stand-by Power mode, and the device consumption drops to I_{CC2}.

HOLD CONDITION

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 5).

The Hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial

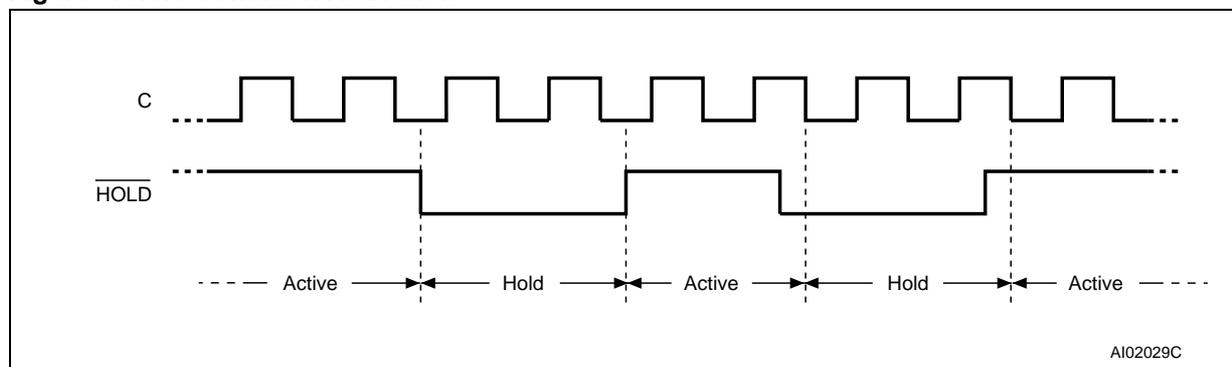**Figure 5. Hold Condition Activation**
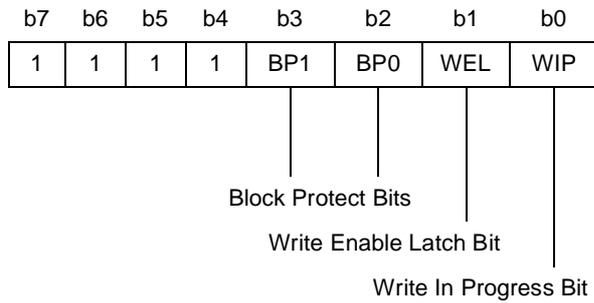
Table 3. Status Register Format

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	BP1	BP0	WEL	WIP

Block Protect Bits

Write Enable Latch Bit

Write In Progress Bit

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 X110
WRDI	Write Disable	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read from Memory Array	0000 $A_8$011
WRITE	Write to Memory Array	0000 $A_8$010

Note: 1. A_8 = 1 for the upper half of the memory array of the M95040, and 0 for the lower half, and is Don't Care for other devices.
2. X = Don't Care.

Clock (C) being Low. The Hold condition starts (or ends, as appropriate) when Serial Clock (C) next goes Low.

STATUS REGISTER

Figure 6 shows the position of the Status Register in the control logic of the device. This register contains a number of control bits and status bits, as shown in Table 3.

Bits b7, b6, b5 and b4 are always read as 1.

WIP bit: The Write In Progress bit is a volatile read-only bit that is automatically set and reset by the internal logic of the device. When set to a 1, it indicates that the memory is busy with a Write cycle.

WEL bit: The Write Enable Latch bit is a volatile read-only bit that is set and reset by specific instructions. When reset to 0, no WRITE or WRSR instructions are accepted by the device.

BP1, BP0 bits: The Block Protect bits are non-volatile read-write bits. These bits define the area of memory that is protected against the execution of Write cycles, as summarized in Table 5.

DATA PROTECTION AND PROTOCOL CONTROL

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

– The WEL bit is reset at power-up.

– Chip Select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile Write cycle (in the memory array or in the Status Register).

– Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.

– Invalid Chip Select ($\overline{S}$) and Hold ($\overline{HOLD}$) transitions are ignored.

For a WRITE or WRSR instruction to be accepted, and for a Write cycle to be started, Chip Select ($\overline{S}$) must be driven High when Serial Clock (C) goes Low, following the clocking in of the eighth bit of the last data byte.

When a Write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction until the present cycle is complete.

Table 5. Write-Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	060h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	040h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	000h - 7Fh

Figure 6. Block Diagram

AI01272B
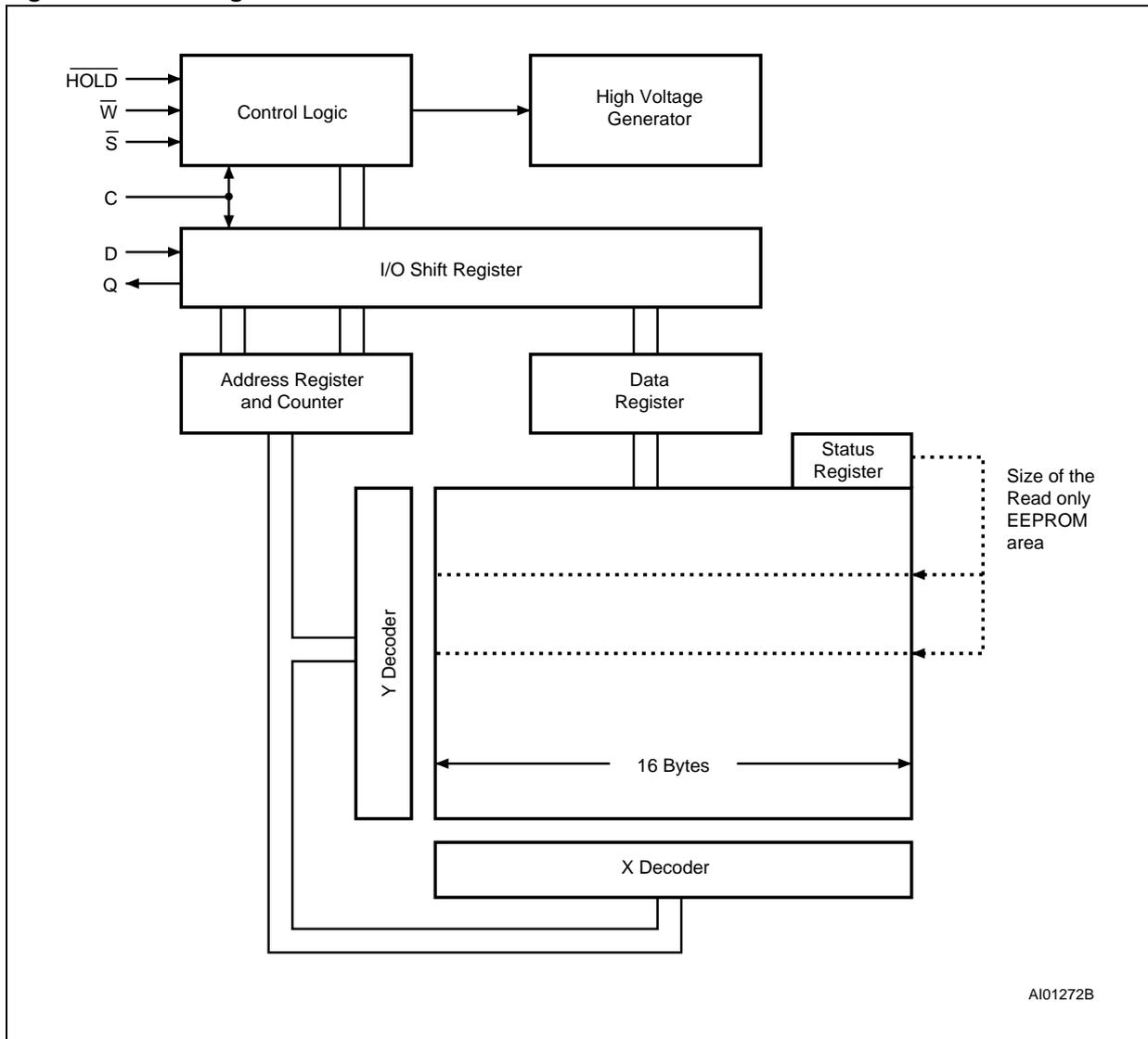
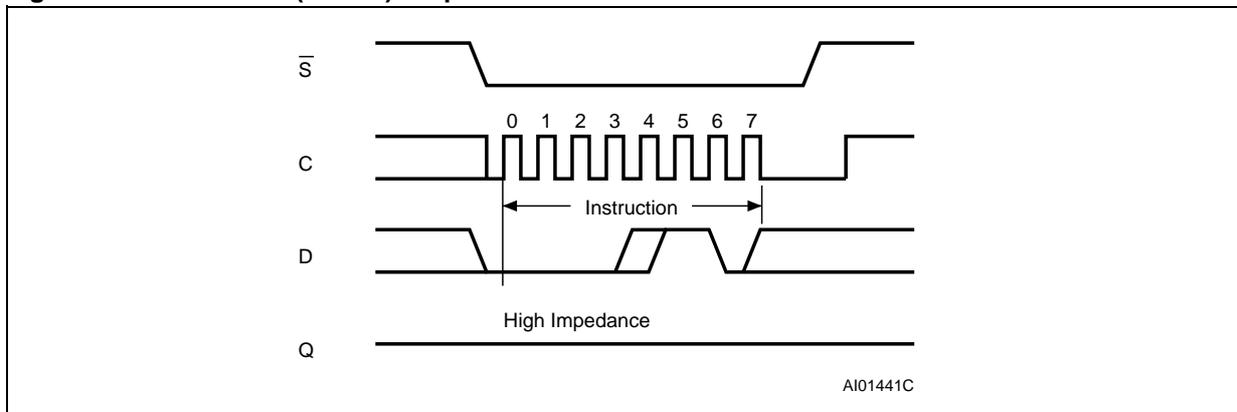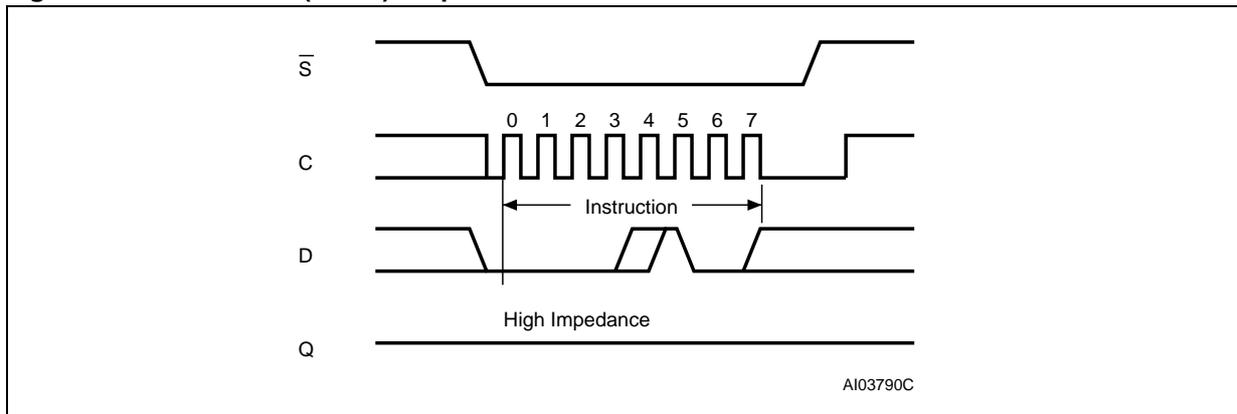**Figure 7. Write Enable (WREN) Sequence**

AI01441C

Figure 8. Write Disable (WRDI) Sequence

AI03790C

INSTRUCTIONS

Each instruction starts with a single-byte code, as summarized in Table 4.

If an invalid instruction is sent (one not contained in Table 4), the device automatically deselects itself.

Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in Figure 7, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

As shown in Figure 8, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

– Power-up
– WRDI instruction execution
– WRSR instruction completion
– WRITE instruction completion
– Write Protect ($\overline{W}$) line being held Low
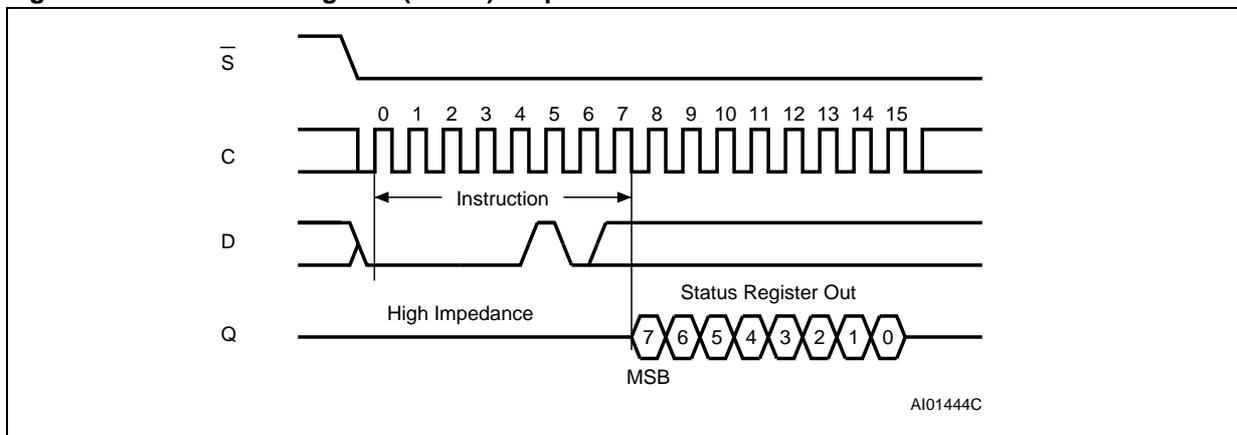
Figure 9. Read Status Register (RDSR) Sequence

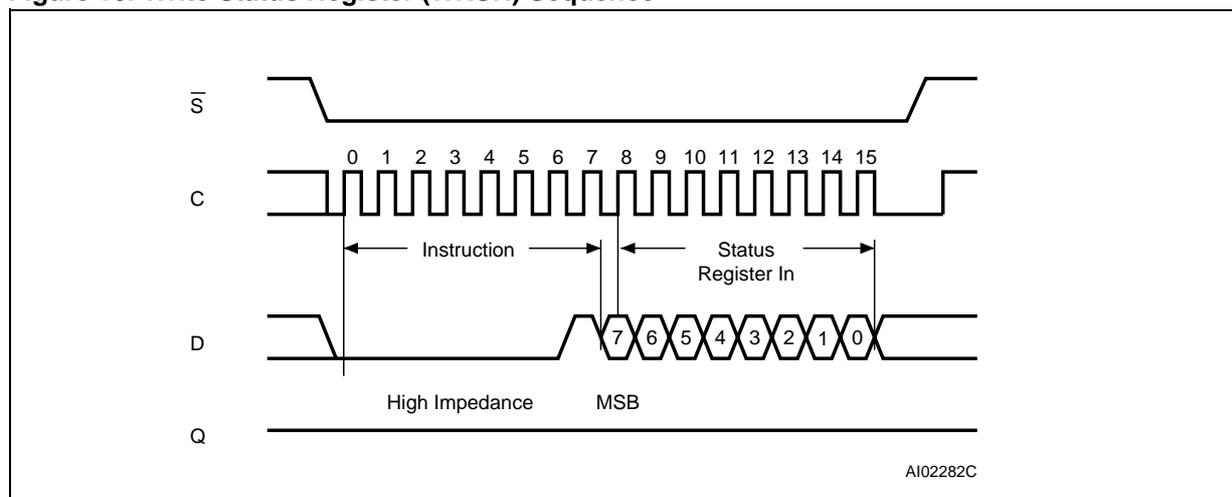AI01444C

Figure 10. Write Status Register (WRSR) Sequence

Table 6. Address Range Bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

Read Status Register (RDSR)

One of the major uses of this instruction is to allow the MCU to poll the state of the Write In Progress (WIP) bit. This is needed because the device will not accept further WRITE or WRSR instructions when the previous Write cycle is not yet finished.

As shown in Figure 9, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte are then shifted in, on Serial Data Input (D). The current state of the bits in the Status Register is shifted out, on Serial Data Out (Q). The Read Cycle is terminated by driving Chip Select ($\overline{S}$) High.

The Status Register may be read at any time, even during a Write cycle (whether it be to the memory area or to the Status Register). All bits of the Status Register remain valid, and can be read using the RDSR instruction. However, during the current Write cycle, the values of the non-volatile bits (BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the Write cycle. On the other hand, the two read-only bits (Write Enable Latch (WEL), Write In Progress (WIP)) are dynamically updated during the on-going Write cycle.

Write Status Register (WRSR)

This instruction allows the MCU to control the parameters of the Software Protected Mode (SPM) by setting the BP1, BP0 bits, and one of the conditions for entering the Hardware Protected Mode (HPM) by setting the Status Register Write Protect (SRWD) bit.

This instruction has no effect on bits b7, b6, b5, b4, b1 and b0 of the Status Register.

As shown in Figure 10, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and data byte are then shifted in on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) must be driven High when Serial Clock (C) goes Low, following the clocking in of the eighth bit of the last data byte. The self-timed Write Cycle starts, and continues for a period t_W (as specified in Tables 8A and 8B), at the end of which the Write in Progress (WIP) bit is reset to 0.

The instruction is not accepted, and is not executed, under the following conditions:

– if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)

– if a Write Cycle is already in progress

– if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, after the eighth bit, b0, of the data byte has been latched in

– if Write Protect ($\overline{W}$) is Low.

Read from Memory Array (READ)

As shown in Figure 11, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The

Figure 11. Read from Memory Array (READ) Sequence
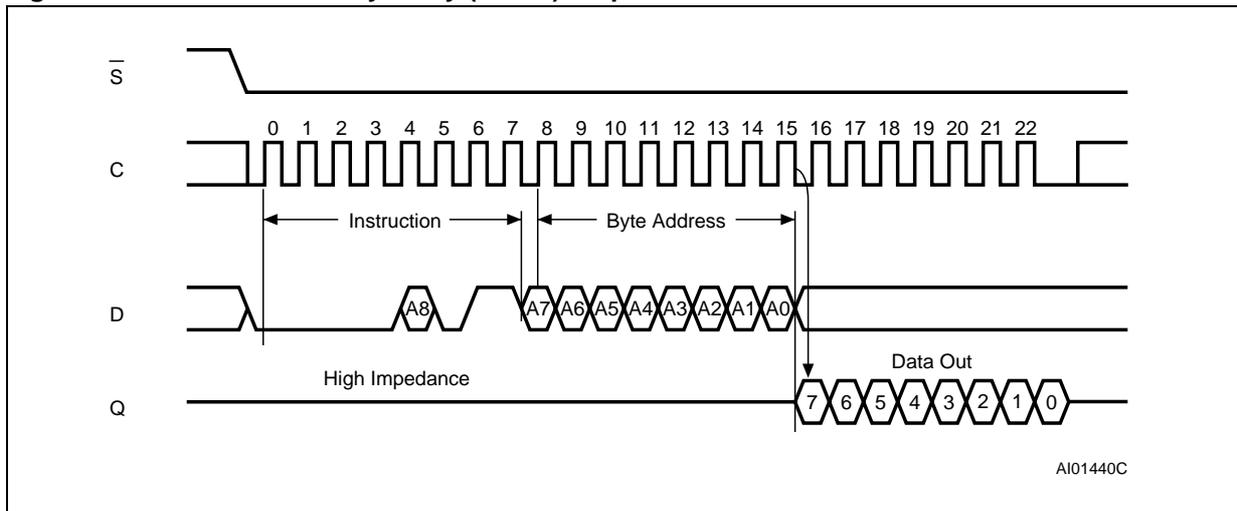
Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

bits of the instruction byte and address byte are then shifted in, on Serial Data Input (D). The most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in Table 4. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven Low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) High. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Write to Memory Array (WRITE)

As shown in Figure 12, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High. In general, the rising edge of the

Figure 12. Byte Write (WRITE) Sequence
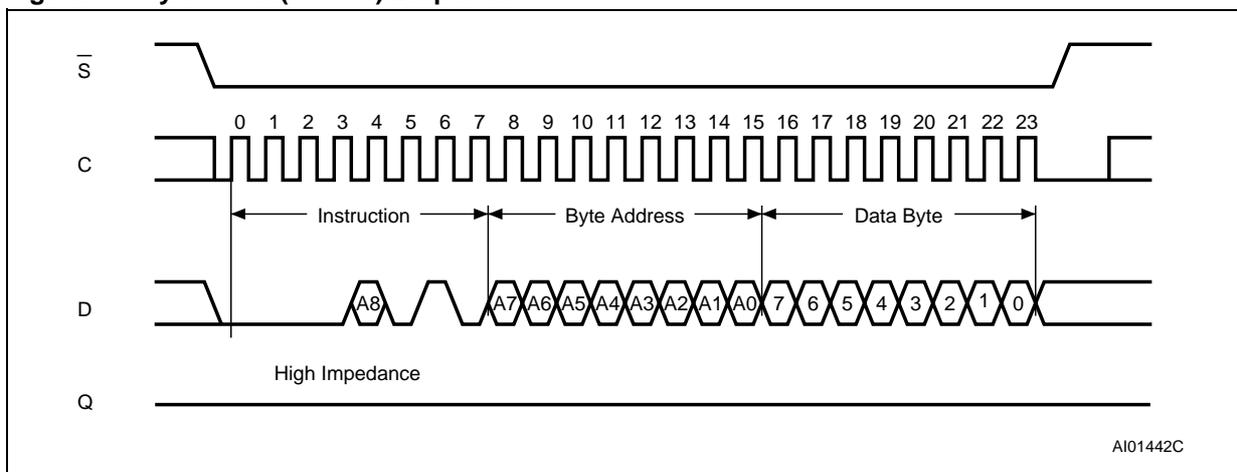
Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) Sequence

Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

Chip Select ($\overline{S}$) signal must occur at a byte boundary of the input data. In the case of Figure 12, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-tim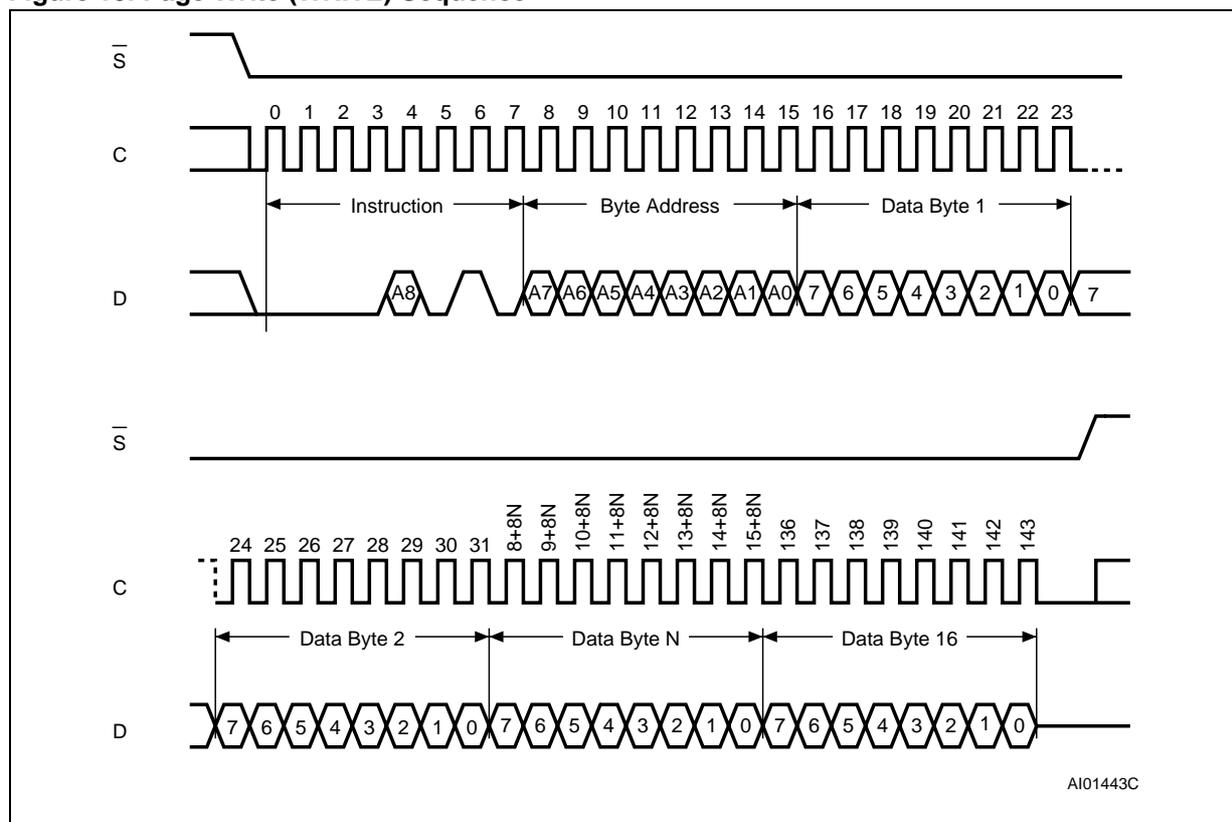ed Write cycle starts, and continues for a period t_{WC} (as specified in Tables 8A and 8B), at the end of which the Write in Progress (WIP) bit is reset to 0.

If, though, Chip Select ($\overline{S}$) continues to be driven Low, as shown in Figure 13, the next byte of input data is shifted in. In this way, all the bytes from the given address to the end of the same page can be programmed in a single instruction.

If Chip Select ($\overline{S}$) still continues to be driven Low, the next byte of input data is shifted in, and is used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

– if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)

– if a Write cycle is already in progress

– if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, at a byte boundary

(after the eighth bit, b0, of the last data byte that has been latched in)

– if Write Protect ($\overline{W}$) is Low or if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

INITIAL POWER-UP STATE

After Power-up, the device is in the following state:

– low power Stand-by mode

– deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).

– not in the Hold Condition

– the Write Enable Latch (WEL) is reset to 0

– Write In Progress (WIP) is reset to 0

the BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

Table 7. DC Characteristics

$(T_A = -40 \text{ to } 85\ °C \text{ or } -40 \text{ to } 125\ °C; V_{CC} = 4.5 \text{ to } 5.5\ V)$
$(T_A = -40 \text{ to } 85\ °C; V_{CC} = 2.5 \text{ to } 5.5\ V)$
$(T_A = -20 \text{ to } 85\ °C; V_{CC} = 1.8 \text{ to } 3.6\ V)$

Symbol	Parameter	Voltage Range	Temp. Range	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	all	all	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	all	all	All inputs driven to V_{SS} or V_{CC}		± 2	µA
I_{CC1}	Supply Current	4.5-5.5	6	C = $0.1V_{CC}/0.9V_{CC}$, at 5 MHz, $V_{CC} = 5\ V$, Q = open		5	mA
		4.5-5.5	3	C = $0.1V_{CC}/0.9V_{CC}$, at 2 MHz, $V_{CC} = 5\ V$, Q = open		5	mA
		2.5-5.5	6	C = $0.1V_{CC}/0.9V_{CC}$, at 2 MHz, $V_{CC} = 2.5\ V$, Q = open		2	mA
		1.8-3.6	5	C = $0.1V_{CC}/0.9V_{CC}$, at 1 MHz, $V_{CC} = 1.8\ V$, Q = open		2	mA
I_{CC2}	Supply Current (Stand-by)	4.5-5.5	6	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5\ V$		10	µA
		4.5-5.5	3	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5\ V$		10	µA
		2.5-5.5	6	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5\ V$		2	µA
		1.8-3.6	5	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 1.8\ V$		2	µA
V_{IL}	Input Low Voltage	all	all		− 0.3	$0.3\ V_{CC}$	V
V_{IH}	Input High Voltage	all	all		$0.7\ V_{CC}$	$V_{CC}+1$	V
V_{OL}[1]	Output Low Voltage	4.5-5.5	6	$I_{OL} = 2\ mA$		0.4	V
		4.5-5.5	3	$I_{OL} = 2\ mA$		0.4	V
		2.5-5.5	6	$I_{OL} = 1.5\ mA$		0.4	V
		1.8-3.6	5	$I_{OL} = 0.15\ mA$		0.3	V
V_{OH}[1]	Output High Voltage	4.5-5.5	6	$I_{OH} = -2\ mA$	$0.8\ V_{CC}$		V
		4.5-5.5	3	$I_{OH} = -2\ mA$	$0.8\ V_{CC}$		V
		2.5-5.5	6	$I_{OH} = -0.4\ mA$	$0.8\ V_{CC}$		V
		1.8-3.6	5	$I_{OH} = -0.1\ mA$	$0.8\ V_{CC}$		V

Note: 1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Figure 14. AC Measurement Conditions

Input Rise and Fall Times	<= 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Input Pulse Voltages	C_L = 30 pF

$0.8V_{CC}$
$0.7V_{CC}$
$0.3V_{CC}$
$0.2V_{CC}$

AI03727
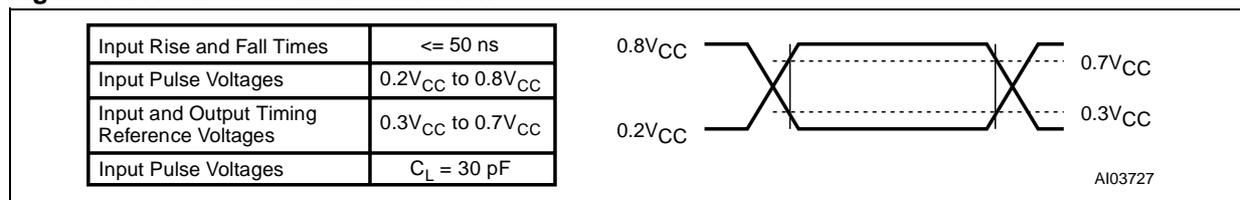
Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 8A. AC Characteristics

Symbol	Alt.	Parameter	M95040, M95020, M95010				Unit
			V_{CC}=4.5 to 5.5 V T_A=−40 to 85°C		V_{CC}=4.5 to 5.5 V T_A=−40 to 125°C		
			Min	Max	Min	Max	
f_C	f_{SCK}	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} [1]	t_{CLH}	Clock High Time	90		200		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{HHCH}	t_{CD}	Clock Low Hold Time after $\overline{HOLD}$ not Active	70		140		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		90		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WC}	Write Cycle Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
   2. Value guaranteed by characterization, not 100% tested in production.

Table 8B. AC Characteristics

Symbol	Alt.	Parameter	M950x0-W V_{CC}=2.5 to 5.5 V T_A=−40 to 85°C		M950x0-R V_{CC}=1.8 to 3.6 V T_A=−20 to 85°C		Unit
			Min	**Max**	**Min**	**Max**	
f_C	f_{SCK}	Clock Frequency	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	200		400		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		300		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		400		ns
t_{CH} [1]	t_{CLH}	Clock High Time	200		400		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{HHCH}	t_{CD}	Clock Low Hold Time after $\overline{HOLD}$ not Active	140		350		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	90		200		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		250	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250		500	ns
t_W	t_{WC}	Write Cycle Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 9. Input Parameters[1] (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)			8	pF
C_{IN}	Input Capacitance (D)			8	pF
	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested.

Figure 15. Serial Input Timing
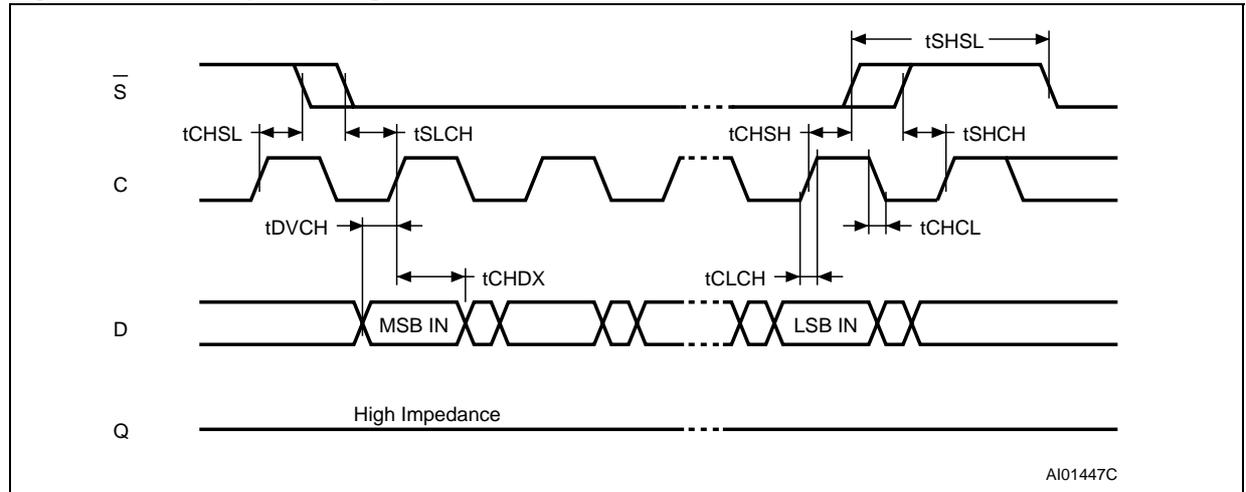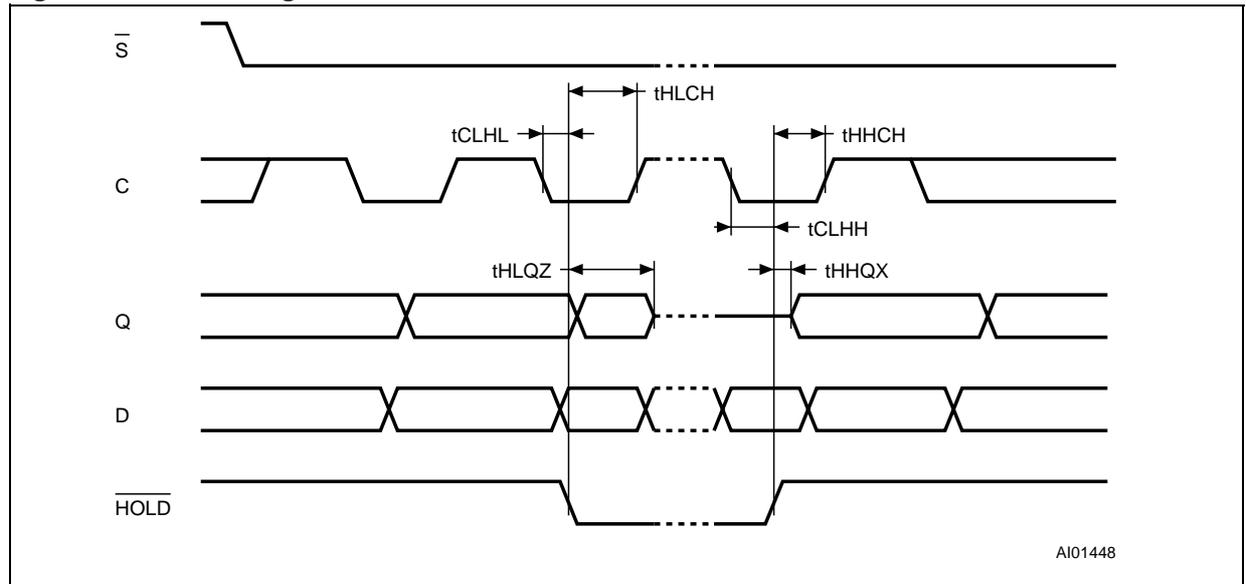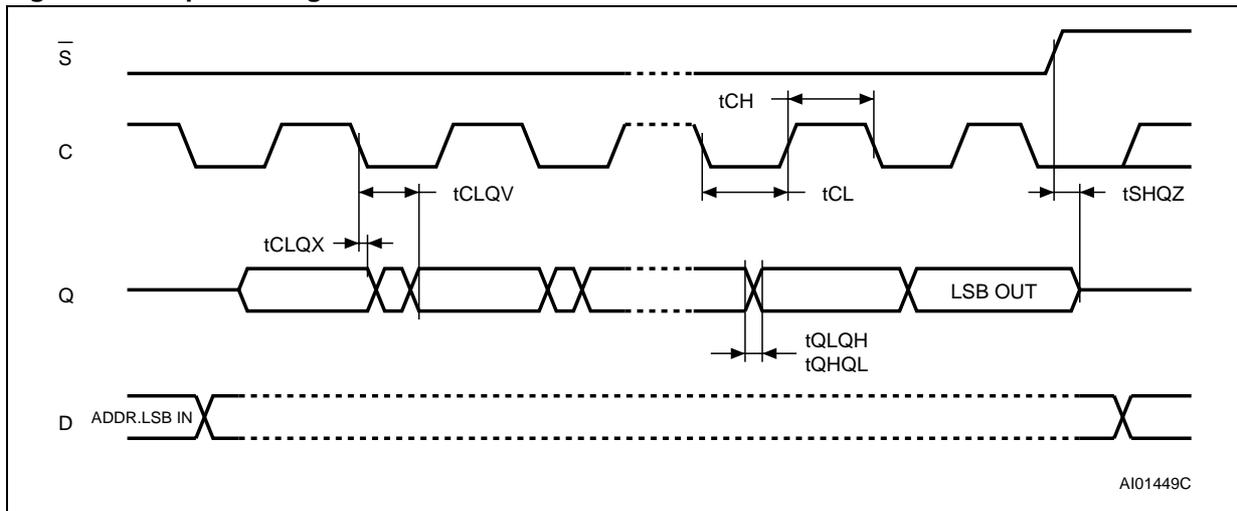

Figure 16. Hold Timing

Figure 17. Output Timing

INITIAL DELIVERY STATE

The device is delivered with the memory array set at all 1s (FFh). The Block Protect (BP1 and BP0) bits are initialized to 0.

ORDERING INFORMATION

The notation used for the device number is as shown in Table 10. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 10. Ordering Information Scheme

Example: M95040   – W   MN   6   TR

Memory Capacity[3]	
040	4 Kbit (512 x 8) with positive clock strobe
020	2 Kbit (256 x 8) with positive clock strobe
010	1 Kbit (128 x 8) with positive clock strobe

Operating Voltage	
blank	4.5 V to 5.5 V
W	2.5 V to 5.5 V
S[2]	1.8 V to 3.6 V

Option	
TR	Tape and Reel Packing

Temperature Range	
5	−20 °C to 85 °C
6	−40 °C to 85 °C
3[1]	−40 °C to 125 °C

Package	
BN	PDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
DW	TSSOP8 (169 mil width)

Note: 1. Temperature range available only on request, in V_{CC} range 4.5 V to 5.5 V only.
2. The -S version (V_{CC} range 1.8 V to 3.6 V) only available in temperature range 5.
3. All devices use a positive clock strobe: Serial Data In (D) is strobed on the rising edge of Serial Clock (C) and Serial Data Out (Q) is synchronized from the falling edge of Serial Clock (C).

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame
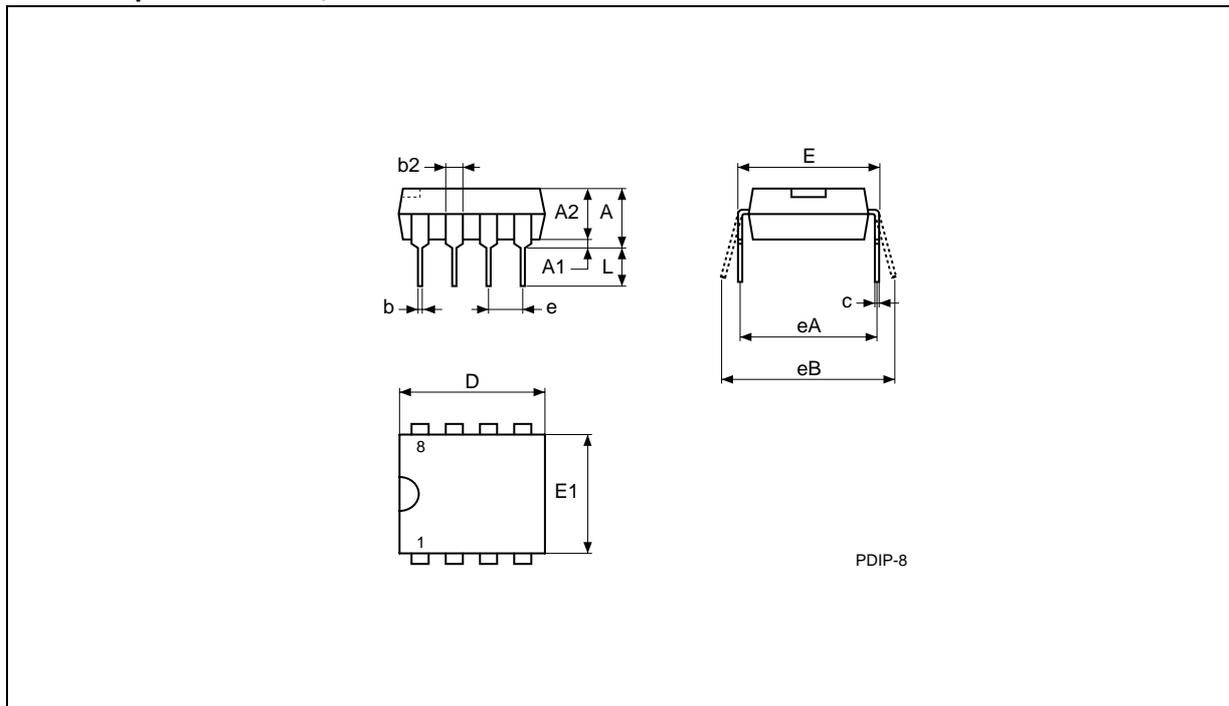
PDIP-8

Note: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150
N		8			8	

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width
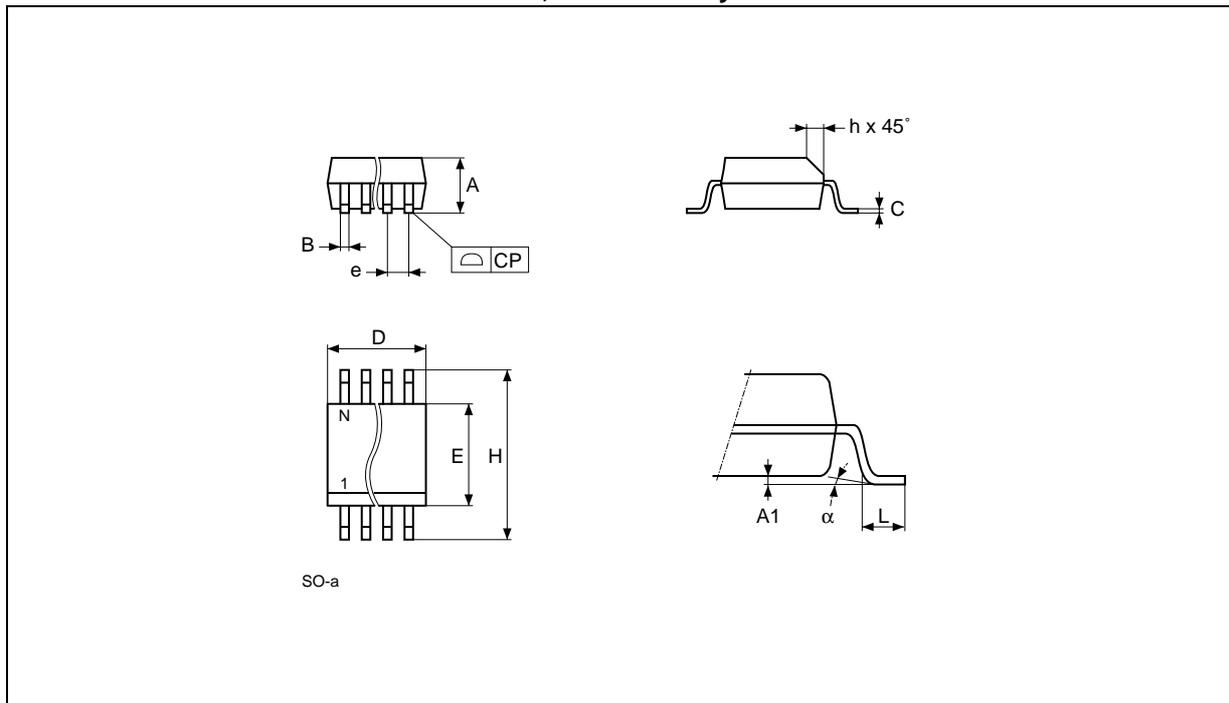
Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

TSSOP8 – 8 lead Thin Shrink Small Outline
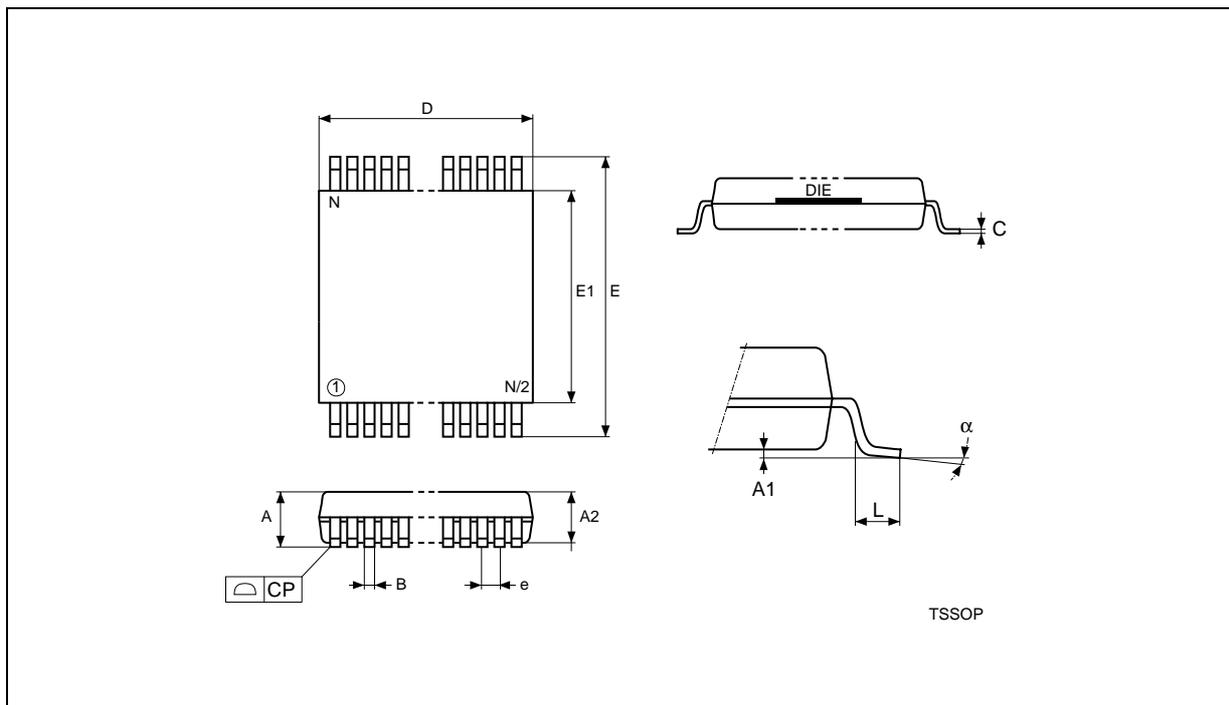
Note: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003

Revision History

Date	Description of Revision
10-May-2000	s/issuing three bytes/issuing two bytes/ in the 2nd sentence of the Byte Write Operation
16-Mar-2001	Human Body Model meets JEDEC std (Table 2). Minor adjustments to Figs 7,9,10,11 & Tab 9. Wording changes, according to the standard glossary Illustrations and Package Mechanical data updated

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

www.st.com