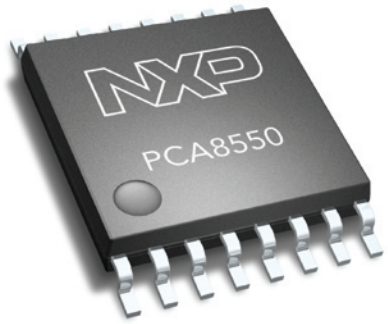


NXP 4-bit muxed / 1-bit latched I²C-bus EEPROM DIP switch PCA8550

Jumperless configuration of PC motherboards

This highly integrated, easy to use DIP switch enables single-chip supervisory configurations. Designed for use with Pentium Pro and Pentium II processors, it reduces component cost, increases reliability, and significantly shrinks the motherboard footprint.

Key features

- 4-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 5-bit internal, non-volatile register
- Override input forces all outputs to logic 0
- Internal, non-volatile register write/readable via I²C-bus
- Write-protect pin enables/disables I²C-bus writes to register
- 2.5-V multiplexed outputs
- 3.3-V non-multiplexed output (latched)
- Inputs tolerant to 5 V
- Housed in 16-pin SO, SSOP, or TSSOP

Applications

- Jumperless configuration of PC motherboards
- Pentium Pro and Pentium II systems

Designed for use with Pentium Pro and Pentium II processors, the NXP PCA8550 enables single-chip supervisory configurations, including processor frequency configuration, processor vendor identification (VID), and temperature voltage/fan sensor data recording (SDR).

The device selects a 4-bit input or data from a non-volatile register and drives the value onto the output pins. An additional, non-multiplexed register output is latched to prevent output value changes while the I²C-bus writes to the non-volatile register. The device also provides write-protect or override to automatically clear the jumpers.

Compared to a mechanical implementation, the PCA8550 greatly increases reliability and provides a much more user-friendly way to set the bits.

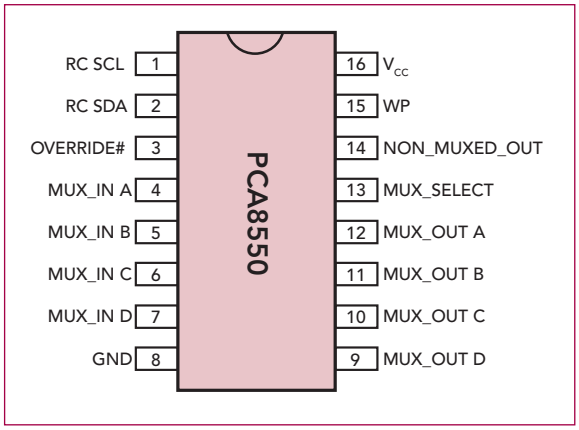
Compared to discrete solutions, the PCA8550 lowers overall cost and reduces motherboard real estate by as much as two thirds.

NXP founded by Philips

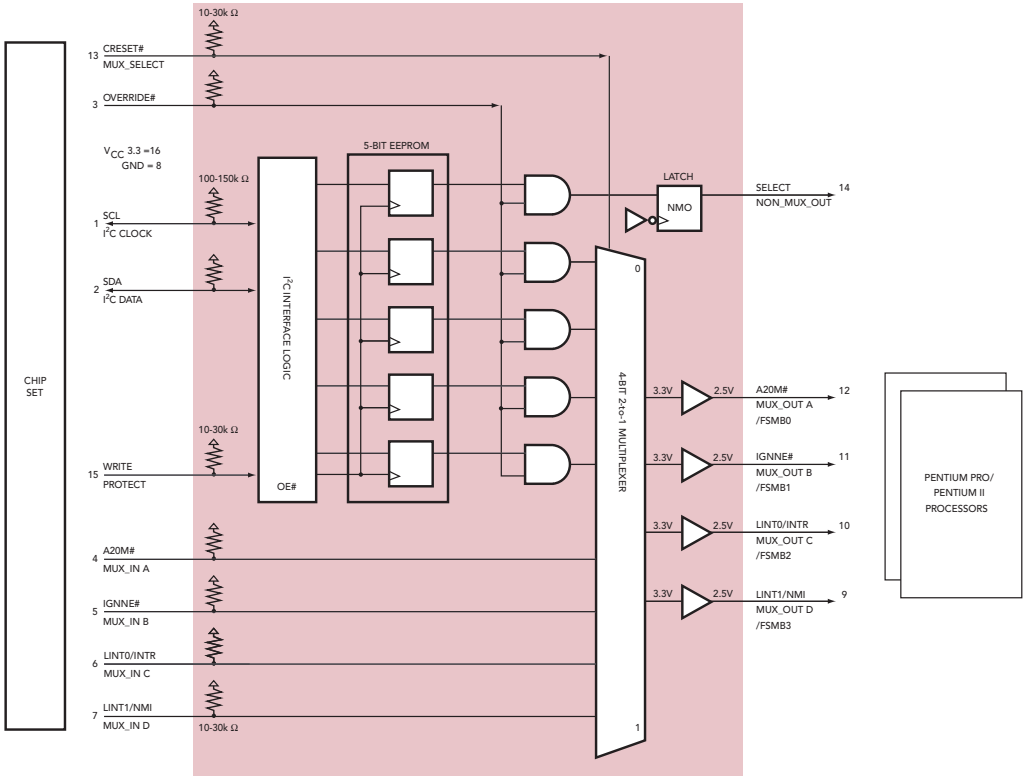
To avoid floating inputs, there are nine internal pull-ups (10- to 50-Ω). The integrated 5-bit EEPROM stores configuration packets transferred via the I²C-bus interface. An integrated latch retains the value of the fifth, non-muxed EEPROM output, and an inverter enables the latch upon request. The integrated 4-bit buffer converts 3.3-V CMOS to 2.5-V level.

A detailed description of PCA8550 design-in is given in Application Note 250.

For more information visit www.nxp.com/i2c



Pinout diagram



PCA8550 block diagram

Ordering information

Product number	Temperature range	Package
PCA8550D	0 to +70 °C	16-pin plastic SO
PCA8550DB	0 to +70 °C	16-pin plastic SSOP
PCA8550PW	0 to +70 °C	16-pin plastic TSSOP

Date of release: August 2007
Document order number: 9397 750 16082
Printed in the USA