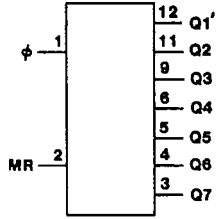


T-45-23-17

High-Speed CMOS Logic

HARRIS SEMICONDUCTOR

27E D 4302271 0017890 6 HAS



92CS-38450R1
CD54/74HC4024, HCT4024
FUNCTIONAL DIAGRAM

7-Stage Binary Ripple Counter

Type Features:

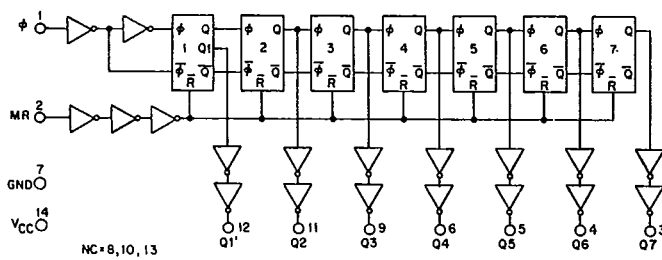
- Fully static operation:
- Buffered inputs:
- Common reset
- Typical $f_{MAX} = 50 \text{ MHz @ } V_{CC} = 5 \text{ V, } C_L = 15 \text{ pF, } T_A = 25^\circ \text{ C}$

The RCA-CD54/74HC4024 and CD54/75HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4024 and CD54HCT4024 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4024 and CD74HCT4024 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to $+85^\circ \text{ C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity: $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8 \text{ V max.}, V_{IH} = 2 \text{ V min.}$
CMOS input compatibility
 $I_i \leq 1 \mu\text{A @ } V_{OL}, V_{OH}$



NC = 8, 10, 13

92CM-38451R3

Fig. 1 - Logic diagram for the CD54/74HC/HCT4024.

TRUTH TABLE

ϕ	MR	OUTPUT STATE
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

CD54/74HC4024 CD54/74HCT4024

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_o):	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ$ C
PACKAGE TYPE E, M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE (T_{STG})	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ$ C
Unit Inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_i, V_o	0	V_{CC}	V
Operating Temperature, T_A :			$^\circ$ C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f :			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

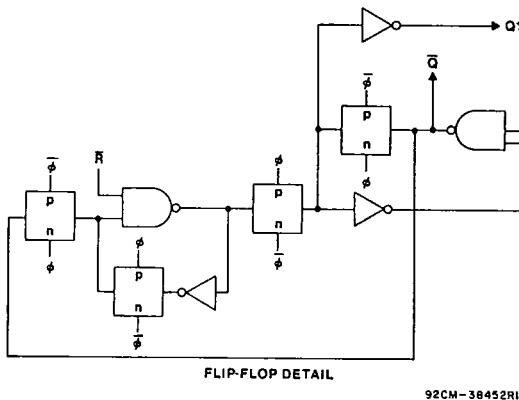


Fig. 2 - Flip-Flop No. 1 detail.

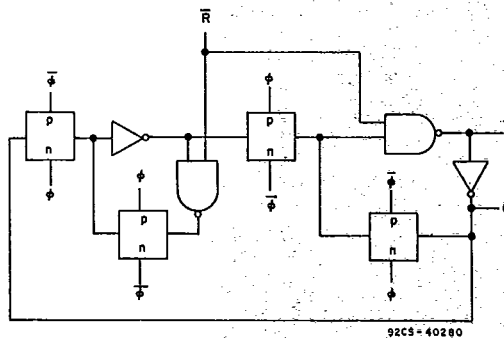


Fig. 3 - Detail for Flip-Flops 2 through 7.

HARRIS SEMICONDUCTOR 27E D 430227J 001789J 8 HAS

CD54/74HC4024
CD54/74HCT4024

STATIC ELECTRICAL CHARACTERISTICS

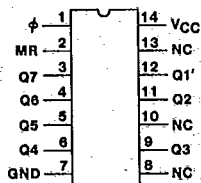
CHARACTERISTICS	CD74HC4024/CD54HC4024									CD74HCT4024/CD54HCT4024									UNITS						
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE			54HC TYPE			TEST CONDITIONS			74HCT/54HCT TYPE				74HCT TYPE			54HCT TYPE		
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Typ	Max	Min		Max	Min	Max			
High-Level Input Voltage	V _{ih}			2	1.5	—	—	1.5	—	1.5	—	—	4.5		2	—	—	2	—	2	—	—	V		
				4.5	3.15	—	—	3.15	—	3.15	—	—	to		—	—	0.8	—	0.8	—	0.8	—	V		
				6	4.2	—	—	4.2	—	4.2	—	—	5.5		—	—	—	—	—	—	—	—	V		
Low-Level Input Voltage	V _{il}			2	—	—	0.5	—	0.5	—	0.5	—	4.5		—	—	0.8	—	0.8	—	0.8	—	V		
				4.5	—	—	1.35	—	1.35	—	1.35	—	to		—	—	—	—	—	—	—	—	V		
				6	—	—	1.8	—	1.8	—	1.8	—	5.5		—	—	—	—	—	—	—	—	V		
High-Level Output Voltage	V _{oh}	V _L or -0.02		2	1.9	—	—	1.9	—	1.9	—	V _L or 4.5	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V		
CMOS Loads	V _{ih}			6	5.9	—	—	5.9	—	5.9	—	V _{ih}											V		
TTL Loads	V _{ih}	V _{ih}		—	—	—	—	—	—	—	—	V _{ih}											V		
				4	4.5	3.98	—	—	3.84	—	3.7	—	4.5	3.98	—	—	3.84	—	3.7	—	—	—	V		
				-5.2	6	5.48	—	—	5.34	—	5.2	—											V		
Low-Level Output Voltage	V _{ol}	V _L or 0.02		2	—	—	0.1	—	0.1	—	0.1	—	V _L or 4.5	4.5	—	—	0.1	—	0.1	—	0.1	—	V		
CMOS Loads	V _{ih}			6	—	—	0.1	—	0.1	—	0.1	—	V _{ih}										V		
TTL Loads	V _{ih}	V _{ih}		—	—	—	—	—	—	—	—	V _{ih}											V		
				4	4.5	—	—	0.26	—	0.33	—	0.4	—	4.5	—	—	0.26	—	0.33	—	0.4	—	V		
				5.2	6	—	—	0.26	—	0.33	—	0.4	—										V		
Input Leakage Current	I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{cc} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA		
Quiescent Device Current	I _{cc}	V _{cc} or Gnd		0	6	—	—	8	—	80	—	160	V _{cc} or Gnd	5.5	—	—	8	—	80	—	160	—	μA		
Additional Quiescent Device Current per Input Pin: 1 Unit Load	ΔI _{cc} *												V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	μA		

*For dual-supply system: theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
φ, MR	0.5

*Unit Load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 360 μA max. @25°C.



TOP VIEW

92CS-38453RI

TERMINAL ASSIGNMENT

HARRIS SEMICONDUCTOR 27E D 4302271 0017892 T HAS

CD54/74HC4024
CD54/74HCT4024

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	C _L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay φ to Q1'	t _{PHL}	15	11	17	ns
	t _{PLH}				
Q _n to Q _{n+1}	t _{PHL}	15	6	6	
	t _{PLH}				
MR to Q _n	t _{PHL}	15	14	17	
	t _{PLH}				
Power Dissipation Capacitance*	C _{PD}	—	30	30	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$ where:

$M = 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$

C_L=output load capacitance

f_i=input frequency

Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f _{MAX}	2	6	—	—	5	—	—	—	4	—	—	—	MHz	
		4.5	30	—	25	—	24	—	20	—	20	—	16		
		6	35	—	—	29	—	—	—	24	—	—	—		
Input Pulse Width	t _w	2	80	—	—	100	—	—	—	120	—	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		
		6	14	—	—	17	—	—	—	20	—	—	—		
Reset Removal Time	t _{REM}	2	50	—	—	65	—	—	—	75	—	—	—	ns	
		4.5	10	—	10	—	13	—	13	—	15	—	15		
		6	9	—	—	11	—	—	—	13	—	—	—		
Reset Pulse Width	t _w	2	80	—	—	100	—	—	—	120	—	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		
		6	14	—	—	17	—	—	—	20	—	—	—		

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, φ to Q1' Output	t _{PLH} t _{PHL}	2	—	140	—	—	175	—	—	—	210	—	—	ns	
		4.5	—	28	—	40	—	35	—	50	—	42	—		60
		6	—	24	—	—	30	—	—	—	36	—	—		—
Propagation Delay Q _n to Q _{n+1}	t _{PLH} t _{PHL}	2	—	75	—	—	95	—	—	—	110	—	—	ns	
		4.5	—	15	—	15	—	19	—	19	—	22	—		22
		6	—	13	—	—	13	—	—	—	19	—	—		—
Propagation Delay MR to Q _n	t _{PHL}	2	—	170	—	—	215	—	—	—	255	—	—	ns	
		4.5	—	34	—	40	—	43	—	50	—	51	—		60
		6	—	29	—	—	27	—	—	—	43	—	—		—
Output Transition Time	t _{TLH} t _{THL}	2	—	75	—	—	95	—	—	—	110	—	—	ns	
		4.5	—	15	—	15	—	19	—	19	—	22	—		22
		6	—	13	—	—	16	—	—	—	19	—	—		—
Input Capacitance	C _I	—	—	10	—	10	—	10	—	10	—	10	pF		

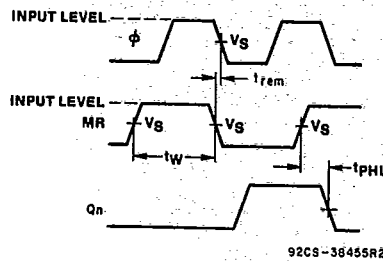
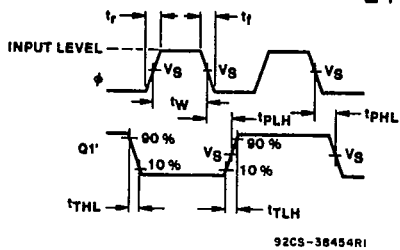
HARRIS SEMICONDUCTOR 27E D 430227J 00J7893 J HAS

CD54/74HC4024
CD54/74HCT4024

HARRIS SEMICONDUCTOR

27E D

4302271 0017894 3 HAS



	54/74HC	54/74HCT
Input Level	VCC	3 V
Switching Voltage, Vs	50% VCC	1.3 V

Fig. 4 - Input Pulse pre-requisite times, propagation delays and output transition times.

Fig. 5 - Master Reset pre-requisite and propagation delays.

