IS-2100ARH, IS-2100AEH

Radiation Hardened High Frequency Half Bridge Drivers

The radiation hardened IS-2100ARH, IS-2100AEH are high frequency, 130V half bridge N-Channel MOSFET driver ICs, which are functionally similar to industry standard 2110 types. The low-side and high-side gate drivers are independently controlled. This gives the user maximum flexibility in dead time selection and driver protocol.

In addition, the devices have on-chip error detection and correction circuitry, which monitors the state of the high-side latch and compares it to the HIN signal. If they disagree, a set or reset pulse is generated to correct the high-side latch. This feature protects the high-side latch from single event upsets (SEUs).

If the SD pin is higher than the VIH threshold, both outputs are driven low regardless of the state of the LIN or HIN pins. While SD is low, the outputs match the states of their corresponding input. The IS-2100ARH, IS-2100AEH output drivers are independent. There is no form of shoot-through protection or non-overlapping time. If shoot-through protection is necessary, that must be considered when generating the LIN and HIN signals.

Inputs			Outputs	
SD	**LIN**	**HIN**	**LO**	**HO**
1	X	X	0	0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1

Features

- Electrically screened to DLA SMD # 5962-99536
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - TID Rad Hard Assurance (RHA) testing
    - HDR (50-300rad(Si)/s): 300krad(Si)
    - LDR (≤ 10mrad(Si)/s): 50krad(Si) (AEH Only)
  - DI RSG process provides latch-up immunity
  - SEU rating: <90MeV/mg/cm^2
  - Vertical device architecture reduces sensitivity to low dose rates
- Bootstrap supply maximum voltage to 150V
- Drives 1000pF load at 1MHz with rise and fall times of 30ns (typical)
- 1.5A (typical) peak output current
- Independent inputs for non-half bridge topologies
- Low DC power consumption: 60mW (typical)
- Operates with V_{DD} = V_{CC} over 12V to 20V range
- Low-side supply undervoltage protection

Applications

- High frequency switch-mode power supplies
- Drivers for inductive loads
- DC motor drivers

1. Overview

1.1 Block Diagram

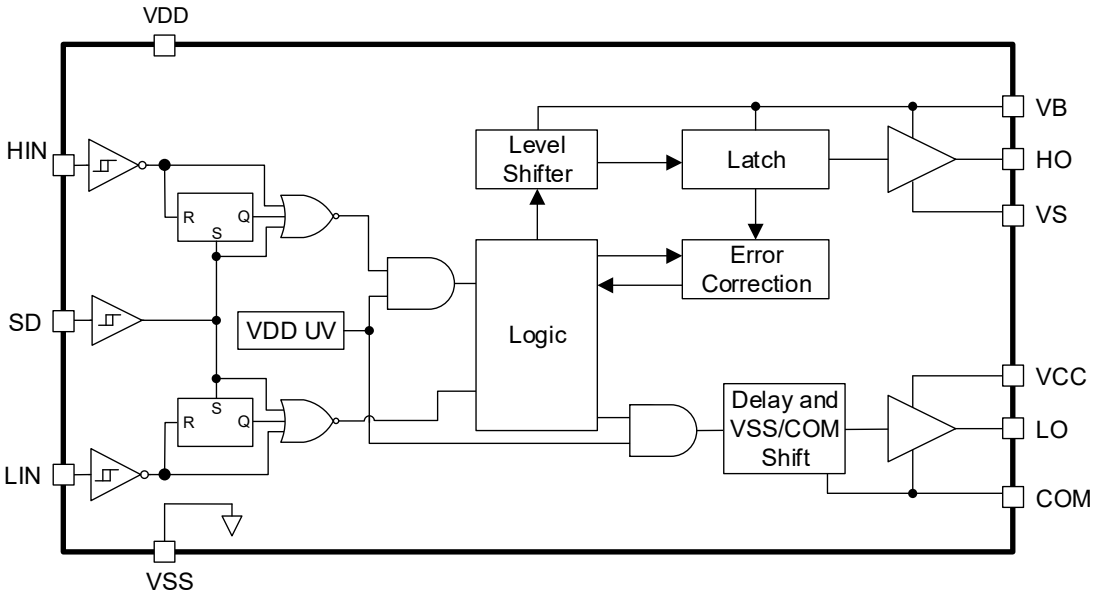


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

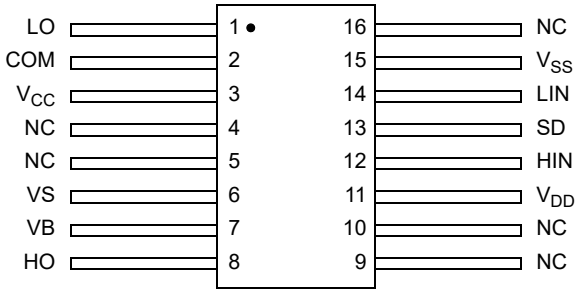


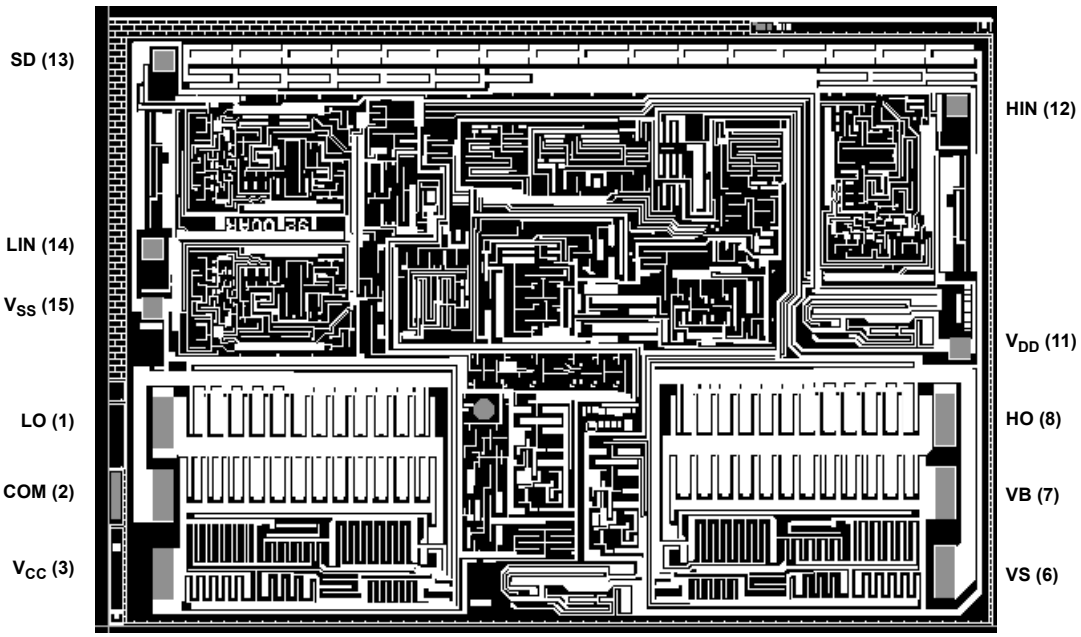
Figure 2. Pin Assignments - Top View

3. Die and Assembly Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	4820µm x 3300µm (190 mils x 130 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0kÅ ±1.0kÅ
Top Metallization	Type: ALSiCu Thickness: 16.0kÅ ±2kÅ
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Backside Finish	Silicon
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2.0 \times 10^5$ A/cm^2
Transistor Count	542
Weight of Packaged Device	0.59 grams (typical) - 16 Lead Flatpack Package (CDFP4-F16)
Lid Characteristics	Finish: Gold Potential: Unbiased

3.1 Metallization Mask Layout



IS-2100ARH, IS-2100AEH

Table 2. IS-2100ARH, ISL-2100AEH Die Layout X-Y Coordinates

Pad Number	Pad Name	Pad Center[1]		Pad Size	
		X (µm)	Y (µm)	DX (µm)	DY (µm)
3	VCC	296.5	270	109	280
6	VS	4561	284.5	109	280
7	VB	4561	711	109	280
8	HO	4561	1079	109	280
11	VDD	4645.5	1500	109	109
12	HIN	4627.5	2817	109	109
13	SD	302	3064.5	109	109
14	LIN	237.5	2040	109	109
15	VSS	239	1719	109	109
1	LO	296.5	1095	109	280
2	COM	296.5	697	109	280

1. Origin of coordinates is the lower left corner of the die.

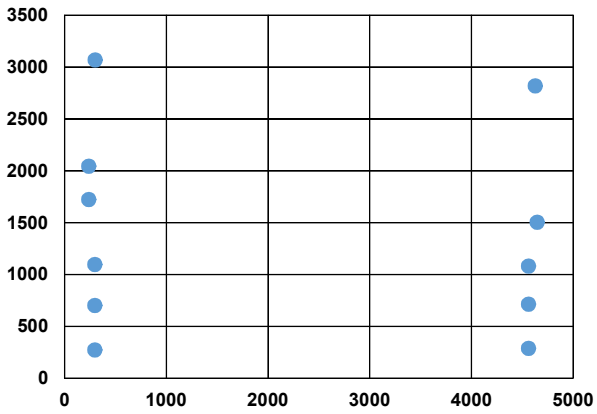


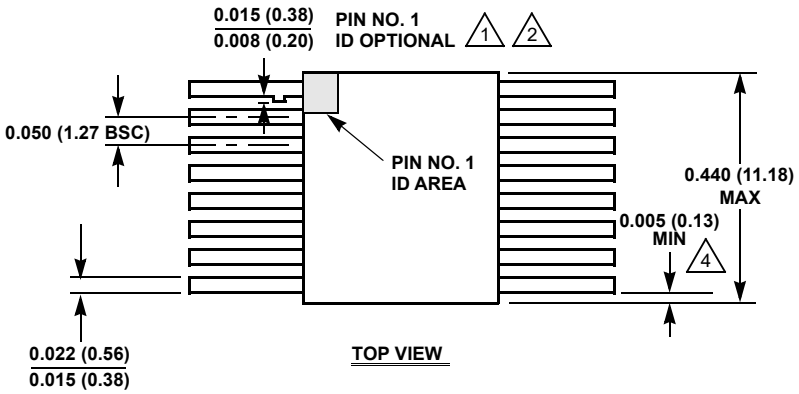
Figure 3. XY Pad Center

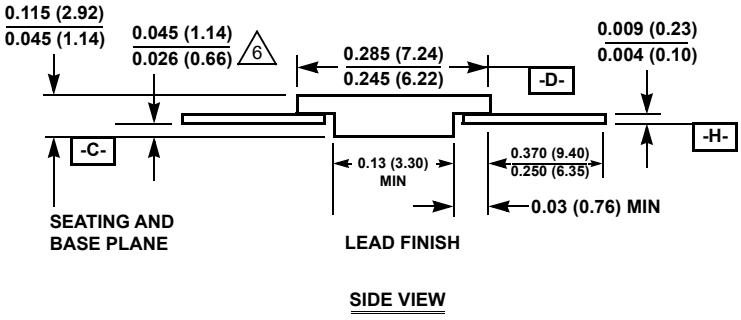
4. Package Outline Drawing

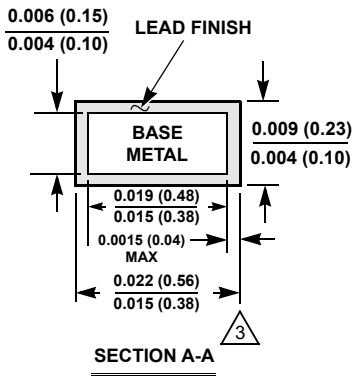
For the most recent package outline drawing, see K16.A.

K16.A

16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

5. Ordering Information

Ordering SMD Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	PKG. DWG. #	Carrier Type	Temp Range
5962F9953602V9A	IS0-2100ARH-Q[3]	HDR to 300krad(Si)	Die	-	-	-55 to +125°C
5962F9953602VXC	IS9-2100ARH-Q		16 Ld Flatpack	K16.A	Tray	
5962F9953602QXC	IS9-2100ARH-8					
N/A	IS9-2100ARH/PROTO[4]	N/A				
N/A	IS0-2100ARH/SAMPLE[3][4]	N/A	Die	-	-	
5962F9953603VXC	IS9-2100AEH-Q	HDR to 300krad(Si) LDR to 50krad(Si)	16 Ld Flatpack	K16.A	Tray	
5962F9953603V9A	IS0-2100AEH-Q[3]		Die	-	-	

1. **Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.**
2. **These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.**
3. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

6. Revision History

Revision	Date	Description
3.01	Aug 21, 2024	Applied the latest template. Updated page 1 description. Updated radiation features bullets. Added block diagram. Updated ordering information table.
3.00	May 10, 2016	Updated Ordering information table by applying new standards and adding Notes 1 and 2. Added Table 2 on page 3. Added Package Outline Drawing K16.A.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.