TC1321

10-Bit Digital-to-Analog Converter with Two-Wire Interface

Features

- 10-Bit Digital-to-Analog Converter
- 2.7-5.5V Single Supply Operation
- Simple SMBus/I^{2}C™ Serial Interface
- Low Power Operation
  - Normal Mode: 350 µA
  - Shutdown Mode: 0.5 µA
- Temperature Range: 40°C to +85°C
- 8-Pin SOIC and 8-Pin MSOP Packages

Applications

- Programmable Voltage Sources
- Digital Controlled Amplifiers/Attenuators
- Process Monitoring and Control

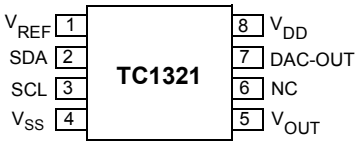
General Description

The TC1321 is a serially accessible, 10-bit voltage output, digital-to-analog converter (DAC). The DAC produces an output voltage that ranges from ground to an externally supplied reference voltage. It operates from a single power supply that can range from 2.7V to 5.5V, making it ideal for a wide range of applications. Built into the part is a Power-on Reset (POR) function that ensures that the device starts at a known condition.

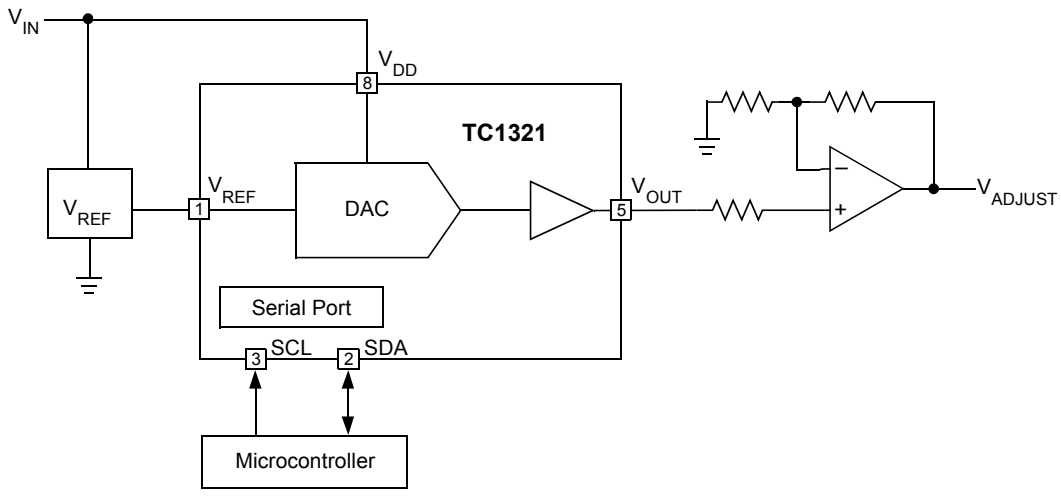
Communication with the TC1321 is accomplished via a simple 2-wire SMBus/I^{2}C compatible serial port, with the TC1321 acting as a slave only device. The host can enable the SHDN bit in the CONFIG register to activate the Low Power Standby mode.

Package Type

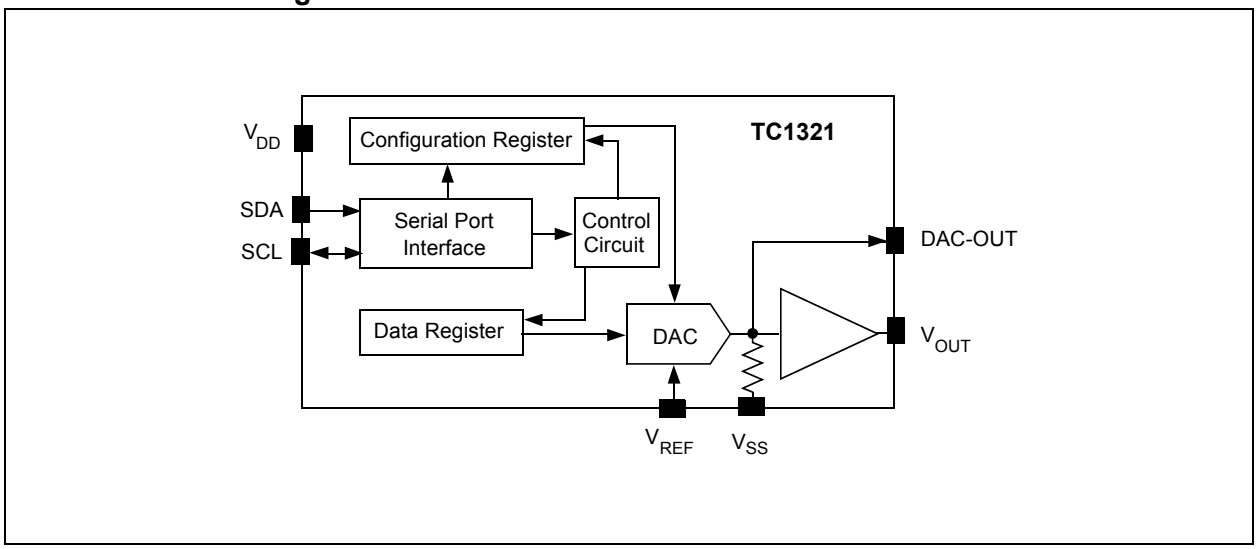
8-Pin MSOP and
8-Pin SOIC (Narrow)



Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD}) .....+6V
Voltage on any Pin .....(V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Current on any Pin .....±50 mA
Package Thermal Resistance (θ_{JA})..... 330°C C/W
Operating Temperature (T_A)..... See Below
Storage Temperature (T_{STG}).....-65°C to +150°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 2.7V to 5.5V, -40°C ≤ T_A ≤ +85°C, V_{REF} = 1.2 V unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power Supply						
V_{DD}	Supply Voltage	2.7	—	5.5	V	
I_{DD}	Operating Current	—	350	500	µA	V_{DD} = 5.5V, V_{REF} = 1.2V Serial Port Inactive **(Note 1)**
$I_{DD-STANDBY}$	Standby Supply Current	—	0.1	1	µA	V_{DD} = 3.3V Serial Port Inactive **(Note 1)**
Static Performance - Analog Section						
	Resolution	—	—	10	Bits	
INL	Integral Non-Linearity at FS, T_A = +25°C	—	—	±4.0	LSB	(**Note 2**)
FSE	Full Scale Error	—	—	±3	%FS	
DNL	Differential Non-Linearity, T_A = +25°C	-1	—	+2	LSB	All Codes **(Note 2)**
V_{OS}	Offset Error at V_{OUT}	—	±0.3	±8	mV	(**Note 2**)
TCV_{OS}	Offset Error Tempco at V_{OUT}	—	10	—	µv/°C	
PSRR	Power Supply Rejection Ratio	—	80	—	dB	V_{DD} at DC
V_{REF}	Voltage Reference Range	0	—	V_{DD} – 1.2	V	
I_{REF}	Reference Input Leakage Current	—	—	±1.0	µA	
V_{SW}	Voltage Swing	0	—	V_{REF}	V	V_{REF} ≤ (V_{DD} – 1.2V)
R_{OUT}	Output Resistance @ V_{OUT}	—	5.0	—	Ω	R_{OUT} (Ω)
I_{OUT}	Output Current (Source or Sink)	—	2	—	mA	
I_{SC}	Output Short-Circuit Current V_{DD} = 5.5V	— —	30 20	50 50	mA mA	Source Sink
Dynamic Performance						
SR	Voltage Output Slew Rate	—	0.8	—	V/µs	
t_{SETTLE}	Output Voltage Full Scale Settling Time	—	10	—	µs	
t_{WU}	Wake-up Time	—	20	—	µs	
	Digital Feed Through and Crosstalk	—	5	—	nV-s	SDA = V_{DD}, SCL = 100 kHz
Serial Port Interface						
V_{IH}	Logic Input High	2.4	—	V_{DD}	V	
V_{IL}	Logic Input Low	—	—	0.6	—	
V_{OL}	SDA Output Low	— —	— —	0.4 0.6	V V	I_{OL} = 3 mA (Sinking Current) I_{OL} = 6 mA

Note 1: SDA and SCL must be connected to V_{DD} or V_{SS}.
2: Measured at V_{OUT} ≥ 50 mV referred to V_{SS} to avoid output buffer clipping.

ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.7V to 5.5V, -40°C ≤ T_A ≤ +85°C, V_{REF} = 1.2 V unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
C_{IN}	Input Capacitance (SDA and SCL pins)	—	5	0.4	pF	
I_{LEAK}	I/O Leakage	—	—	±1.0	µA	
Serial Port AC Timing						
f_{SMB}	SMBus Clock Frequency	10	—	100	kHz	
t_{IDLE}	Bus Free Time Prior to New Transition	4.7	—	—	µs	
$t_{H(START)}$	START Condition Hold Time	4.0	—	—	µs	
$t_{SU(START)}$	START Condition Setup Time	4.7	—	—	µs	90% SCL to 10% SDA (for Repeated START Condition)
$t_{SU(STOP)}$	STOP Condition Setup Time	4.0	—	—	µs	
t_{H-DATA}	Data In Hold Time	100	—	—	ns	
$t_{SU-DATA}$	Data In Setup Time	100	—	—	ns	
t_{LOW}	Low Clock Period	4.7	—	—	µs	10% to 10%
t_{HIGH}	High Clock Period	4	—	—	µs	90% to 90%
t_F	SMBus Fall Time	—	—	300	ns	90% to 10%
t_R	SMBus Rise Time	—	—	1000	ns	10% to 90%
t_{POR}	Power-on Reset Delay	—	500	—	µs	V_{DD} ≥ V_{POR} (Rising Edge)

Note 1: SDA and SCL must be connected to V_{DD} or V_{SS}.
2: Measured at V_{OUT} ≥ 50 mV referred to V_{SS} to avoid output buffer clipping.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: V_{DD} = 2.7V to 5.5V, -40°C ≤ T_A ≤ +85°C, V_{REF} = 1.2V unless otherwise noted.						
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L MSOP	θ_{JA}	—	211	—	°C/W	

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
1	V_{REF}	Input	Voltage Reference Input Pin
2	SDA	Bi-Directional	Serial Data Input/Output Pin
3	SCL	Input	Serial Clock Input Pin
4	V_{SS}	Power	Ground Reference Pin
5	V_{OUT}	Output	Buffered Analog Voltage Output Pin
6	NC	None	No connection
7	DAC-OUT	Output	Unbuffered Analog Voltage Output Pin
8	V_{DD}	Power	Positive Power Supply Input Pin

2.1 External Voltage Reference Input (V_{REF})

Voltage Reference Input can range from 0V to 1.2V below V_{DD}.

2.2 Bi-Directional Serial Data Input and Output (SDA)

Serial data is transferred on the SMBus in both directions using this pin.

2.3 Serial Clock Input (SCL)

SMBus/I^2C serial clock. Clocks data into and out of the TC1321.

2.4 Supply Power Ground (V_{SS})

The ground reference pin.

2.5 Output (V_{OUT})

Buffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register.

2.6 No Connection (NC)

There is not a connection at this pin.

2.7 Output (DAC-OUT)

Unbuffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. This output is unbuffered and care must be taken that the pin is connected only to a high-impedance node.

2.8 Positive Power Supply Input (V_{DD})

See the Electrical Specifications table.

NOTES:

3.0 DETAILED DESCRIPTION

The TC1321 is a monolithic 10-bit digital-to-analog converter that is designed to operate from a single supply that can range from 2.7V to 5.5V. The DAC consists of a data register (DATA), a configuration register (CONF), and a current output amplifier. The TC1321 uses an external reference which also determines the maximum output voltage.

The TC1321 uses a current steering DAC based on an array of matched current sources. This current, along with a precision resistor, converts the contents of the DATA Register and V_{REF} into an output voltage, V_{OUT}, that is given by:

$$V_{OUT} = V_{REF} \times \left[\frac{DATA}{1024}\right]$$

3.1 Reference Input

The reference pin, V_{REF}, is a buffered high-impedance input. Because of this, the load regulation of the reference source needs only to be able to tolerate leakage levels of current (less than 1 µA). V_{REF} accepts a voltage range from 0 to (V_{DD} – 1.2V). Input capacitance is typically 10 pF.

3.2 Output Amplifier

The TC1321 DAC output is buffered with an internal unity gain rail-to-rail input/output amplifier with a typical slew rate of 0.8V/µs. Maximum full scale transition settling time is 10 µsec to within ±1/2LSB when loaded with 1 kΩ in parallel with 100 pF.

3.3 Standby Mode

The TC1321 allows the host to put it into a Low Power (I_{DD} = 0.5 µA, typically) Standby mode.

In this mode, the D/A conversion is halted. The SMBus port operates normally. Standby mode is enabled by setting the SHDN bit in the CONFIG register. Table 3-1 summarizes this operation.

TABLE 3-1: STANDBY MODE OPERATION

SHDN Bit	Operating Mode
0	Normal
1	Standby

3.4 SMBus Slave Address

The TC1321 is internally programmed to have a default SMBus address value of 1001 000b. Seven other addresses are available by custom order (contact Microchip Worldwide Sales and Service). See Figure 3-1 for the location of address bits in SMBus protocol.

Write 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	Data	ACK	P
	7-Bits	0		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Write 2-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	Data	ACK	Data	ACK	P
	7-Bits	0		8-Bits		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Read 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	S	Address	R/$\overline{W}$	ACK	Data	NACK	P
	7-Bits	0		8-Bits			7-Bits	1		8-Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data flow direction.

Data Byte: reads from the register set by the command byte.

Read 2-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	S	Address	R/$\overline{W}$	ACK	Data	ACK	Data	NACK	P
	7-Bits	0		8-Bits			7-Bits	1		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data flow direction.

Data Byte: reads from the register set by the command byte.

Receive 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Data	NACK	P
	7-Bits	1		8-Bits		

S = START Condition
P = STOP Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last read-byte or write-byte transmission.

Receive 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Data	ACK	Data	NACK	P
	7-Bits	1		8-Bits		8-Bits		

S = START Condition
P = STOP Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last read-byte or write-byte transmission.

FIGURE 3-1: *SMBus/I^{2}C Protocols.*

4.0 SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi-directional data port (SDA) form a 2-wire bi-directional serial port for programming and interrogating the TC1321. The following conventions are used in this bus architecture.

TABLE 4-1: TC1321 SERIAL BUS CONVENTIONS

Term	Explanation
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device that controls the bus: initiating transfers (START), generating the clock, and terminating transfers (STOP)
Slave	The device addressed by the master.
START	A unique condition signaling the beginning of a transfer, indicated by SDA falling (High - Low) while SCL is high.
STOP	A unique condition signaling the end of a transfer, indicated by SDA rising (Low - High) while SCL is high.
ACK	A receiver acknowledges the receipt of each byte with this unique condition. The receiver drives SDA low during SCL, high of the ACK clock pulse.The master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
Not Busy	When the bus is IDLE, both SDA and SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers. See START and STOP conditions.

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the master, which provides the clock signal for all transfers. The TC1321 *always* operates as a slave. The serial protocol is illustrated in Figure 4-1. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a START condition (START), followed by a device-address byte and one or more data bytes. The device-address byte includes a Read/Write selection bit. Each access must be terminated by a STOP Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is HIGH are reserved for START and STOP conditions).

4.1 START Condition (START)

The TC1321 continuously monitors the SDA and SCL lines for a START condition (a HIGH to LOW transition of SDA while SCL is HIGH), and will not respond until this condition is met.

4.2 Address Byte

Immediately following the START condition, the host must transmit the address byte to the TC1321. The 7-bit SMBus address for the TC1321 is `1001000`. The 7-bit address transmitted in the serial bit stream must match for the TC1321 to respond with an Acknowledge (indicating the TC1321 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write bit. This bit is a 1 for a read operation or 0 for a write operation. During the first phase of any transfer, this bit will be set = 0 to indicate that the command byte is being written.

4.3 Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TC1321. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the TC1321 to pull the SDA line LOW to Acknowledge that it successfully received the previous eight bits of data or address.

4.4 Data Byte

After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TC1321.

4.5 Stop Condition (STOP)

Communications must be terminated by a STOP condition (a LOW to HIGH transition of SDA while SCL is HIGH). The STOP condition must be communicated by the transmitter to the TC1321. Refer to Figure 4-1, for serial bus timing.

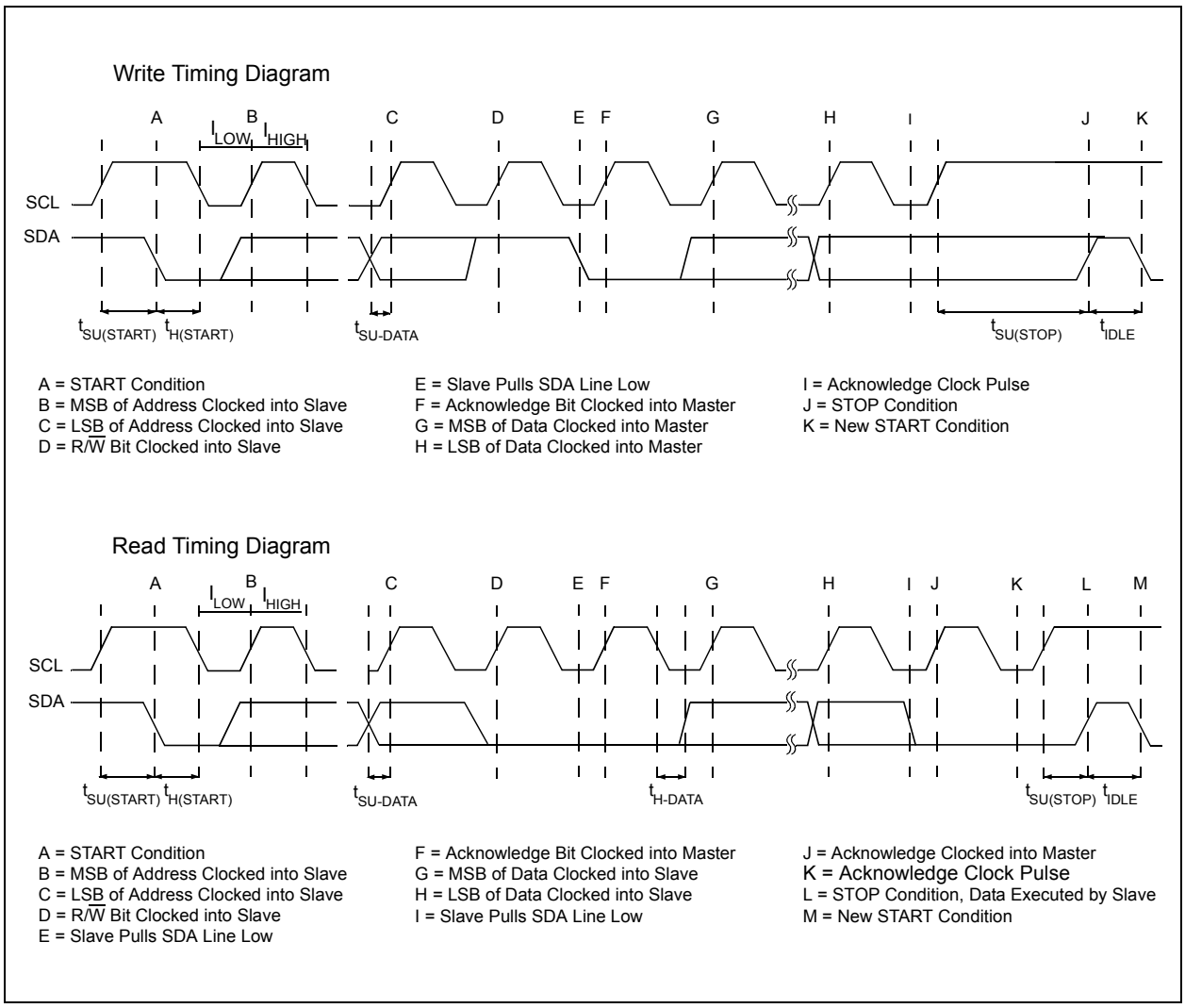


FIGURE 4-1: *SMBus/I²CTiming Diagrams.*

4.6 Register Set and Programmer's Model

TABLE 4-2: TC1321 COMMAND SET (READ_BYTE AND WRITE_BYTE)

Command Byte Description		
Command	**Code**	**Function**
RWD	00h	Read/$\overline{\text{Write}}$ Data (DATA)
RWCR	01h	Read/$\overline{\text{Write}}$ Configuration (CONFIG)

TABLE 4-3: CONFIGURATION REGISTER (CONFIG), 8-BIT, READ/WRITE

Configuration Register (CONFIG)								
Bit Name	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**
Bit Function	Reserved **(Note 1)**							SHDN **(Note 2)**

Note 1: Always returns '0' when reading
2: 1 = Standby (Shut down) mode
0 = Normal mode

TABLE 4-4: DATA REGISTER (DATA), 10-BIT, READ/WRITE

Data Register (DATA) for 1st Byte								Data Register (DATA) for 2nd Byte							
D[9]	**D[8]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	X	X	X	X	X	X
MSB	X	X	X	X	X	X	X	X	LSB	X	X	X	X	X	X

The DAC output voltage is a function of reference voltage and the binary value of the contents of the register DATA. The transfer function is given by the expression:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left[\frac{DATA}{1024}\right]$$

4.7 Register Set Summary

The register set for the TC1321 is summarized in Table 4-5.

TABLE 4-5: TC1321 REGISTER SET SUMMARY

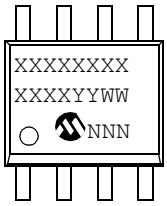
Name	Description	POR State	Read	Write
Data	DATA Register (2-Byte Format)	0000000000b	X	X
Config	CONFIG Register	0000 0000b	X	X

NOTES:

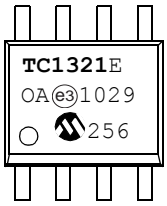
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

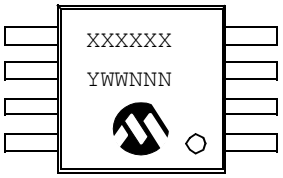
8-Lead SOIC (150 mil)



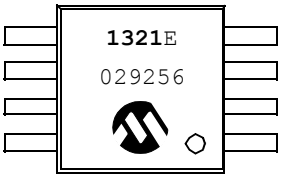
Example



8-Lead MSOP



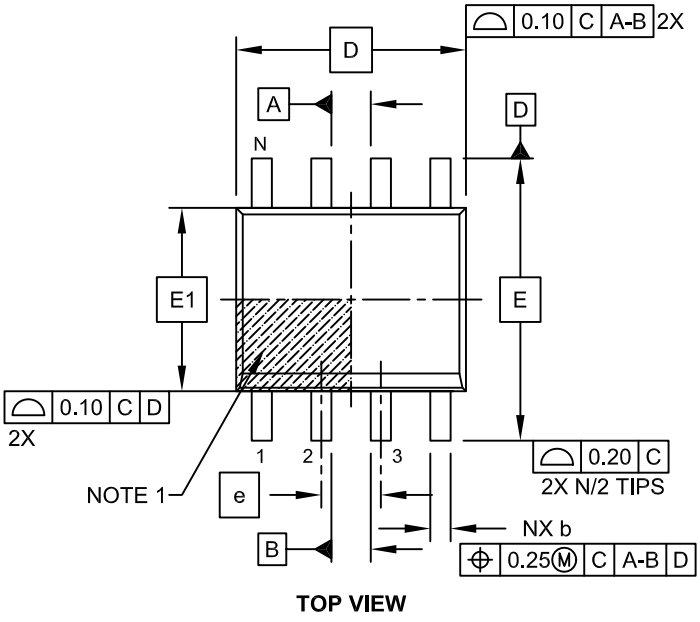
Example



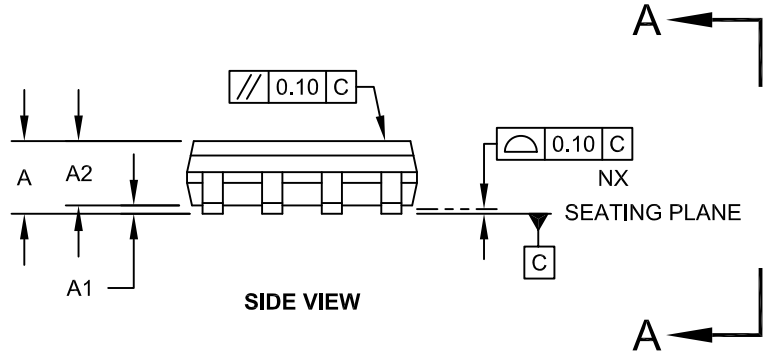
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

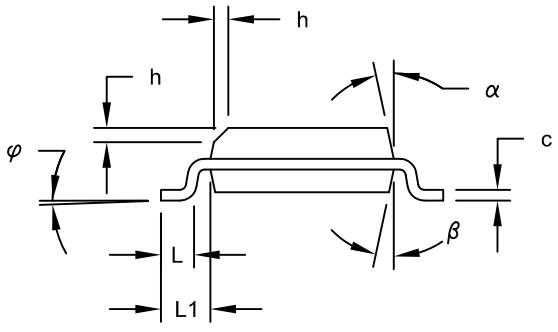
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

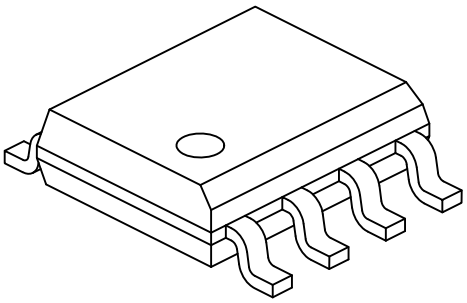


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

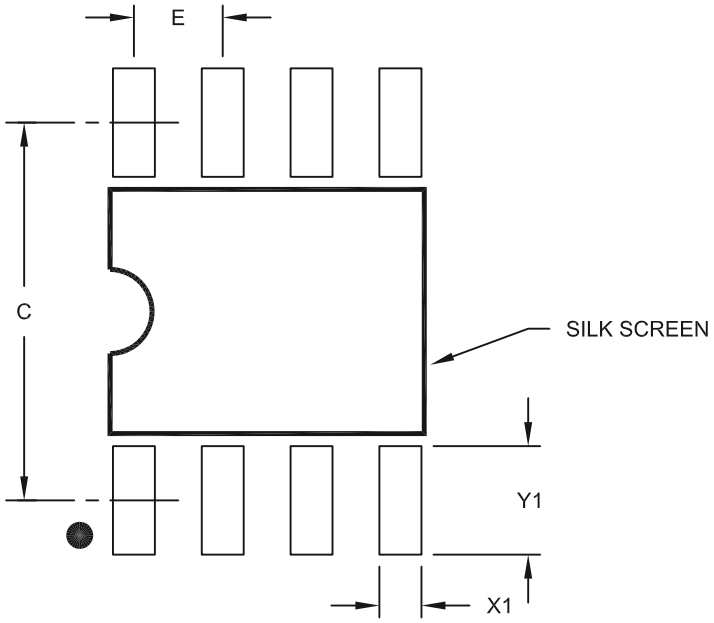
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

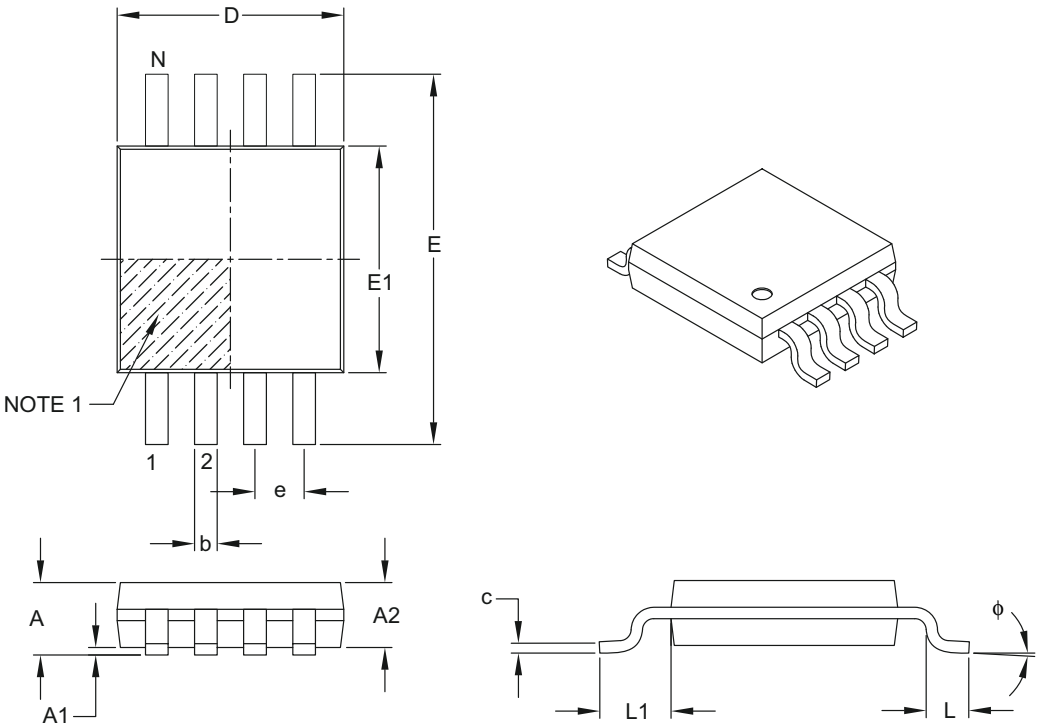
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

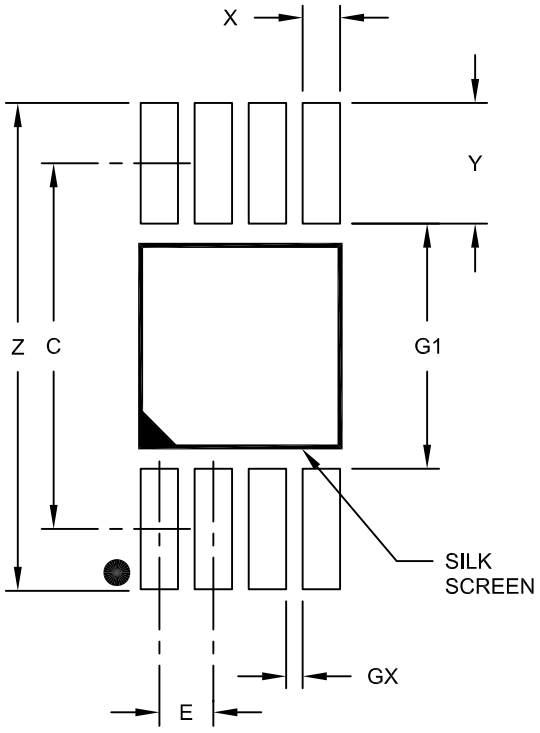
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

APPENDIX A: REVISION HISTORY

Revision C (November 2010)

The following is the list of modifications:

1. Updated the Electrical Specifications table.
2. Updated **Section 5.0 "Packaging Information"**. Replaced the older package drawings with current drawings from the *Microchip Packaging Specification* (DS00049BF).
3. Added the Revision History section.
4. Updated the Product Identification System section.

Revision B (May 2008)

- Undocumented changes.

Revision A (November 2007)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	TC1321:	10-Bit Digital-to-Analog Converter with Two-Wire Interface
Tape and Reel	TR =	Tape and Reel
Temperature Range	I =	-40°C to +85°C (Industrial)
Package	OA =	Small Outline Package (SOIC), (3,90 mm) 8-lead
	UA =	Micro Small Outline Package (MSOP), 8-lead

Examples:

a)	TC1321VUA:	8LD MSOP package.
b)	TC1321VUATR:	Tape and Reel 8LD MSOP package.
c)	TC1321EUA:	8LD MSOP package.
d)	TC1321EUATR:	Tape and Reel, 8LD MSOP package.
e)	TC1321EOA:	8LD SOIC package.
f)	TC1321EOATR:	Tape and Reel 8LD SOIC package.
g)	TC1321VOA:	8LD SOIC package.
h)	TC1321VOATR:	Tape and Reel 8LD SOIC package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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