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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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BIC702C

Bias Controlled Monolithic IC VHF/UHF RF Amplifier

RENESAS

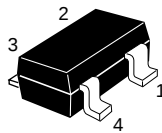
ADE-208-814D (Z)
5th. Edition
Mar. 2001

Features

- Bias Controlled Monolithic IC (No external DC biasing voltage on gate1.);
To reduce using parts cost & PC board space.
- High $|y_{fs}|$;
 $|y_{fs}| = 29 \text{ mS typ. (} f = 1\text{kHz)}$
- Low noise;
 $NF = 1.0 \text{ dB typ. (at } f = 200 \text{ MHz), } NF = 1.6 \text{ dB typ. (at } f = 900 \text{ MHz)}$
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at $C = 200\text{pF}$, $R_s = 0$ conditions.
- Provide mini mold package; CMPAK-4 (SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "BZ-".
 2. BIC702C is individual type number of HITACHI BICMIC.

Absolute Maximum Ratings (Ta = 25°C)

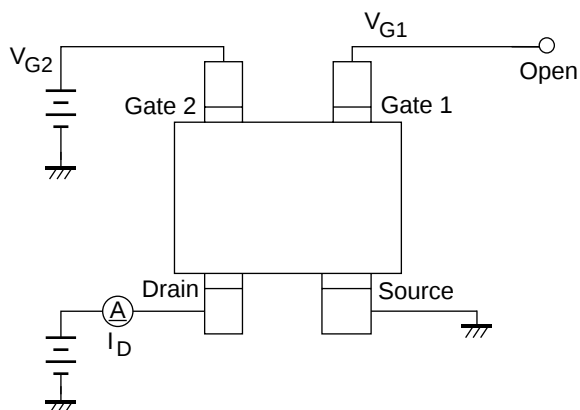
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Electrical Characteristics (Ta = 25°C)

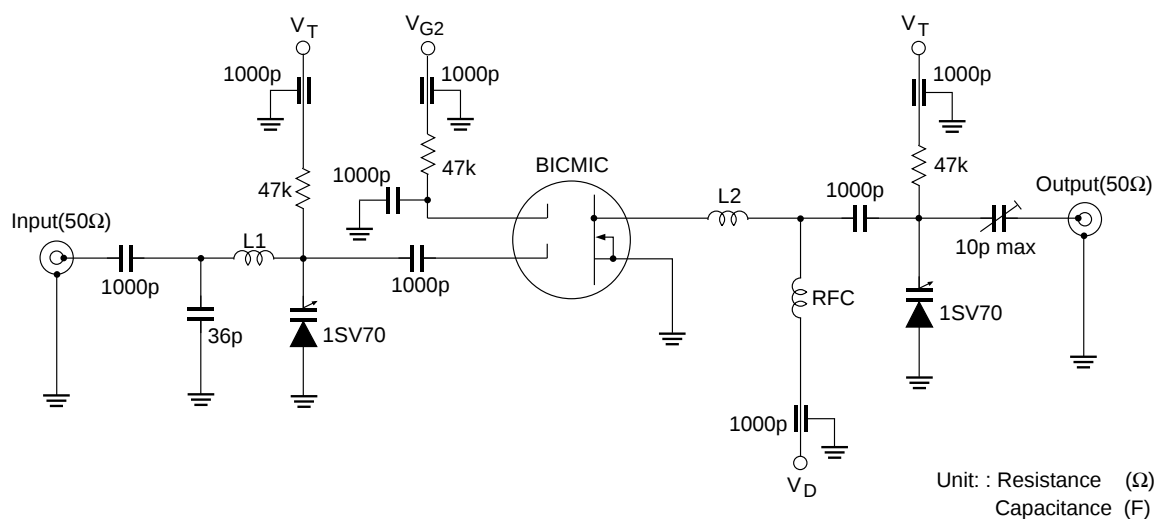
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$ $V_{G2S} = 0, V_{G1} = \text{open}$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A, V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\mu A, V_{G1S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V, V_{G1S} = V_{DS} = 0$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5V, I_D = 100\mu A$ $V_{G1} = \text{open}$
Drain current	$I_{D(op)}$	10	13	16	mA	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Forward transfer admittance	$ y_{fs} $	24	29	34	mS	$V_{DS} = 5V, I_D = 13mA$ $V_{G2S} = 4V, f = 1kHz$
Input capacitance	C_{iss}	1.6	2.0	2.3	pF	$V_{DS} = 5V, V_{G2S} = 4V$
Output capacitance	C_{oss}	0.7	1.1	1.5	pF	$V_{G1} = \text{open}$
Reverse transfer capacitance	C_{rss}	—	0.02	0.05	pF	$f = 1MHz$
Power gain	PG1	24	28.5	—	dB	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Noise figure	NF1	—	1.0	1.5	dB	$f = 200MHz$
Power gain	PG2	18	23	—	dB	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Noise figure	NF2	—	1.6	2.2	dB	$f = 900MHz$

Test Circuits

- **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF , PG)

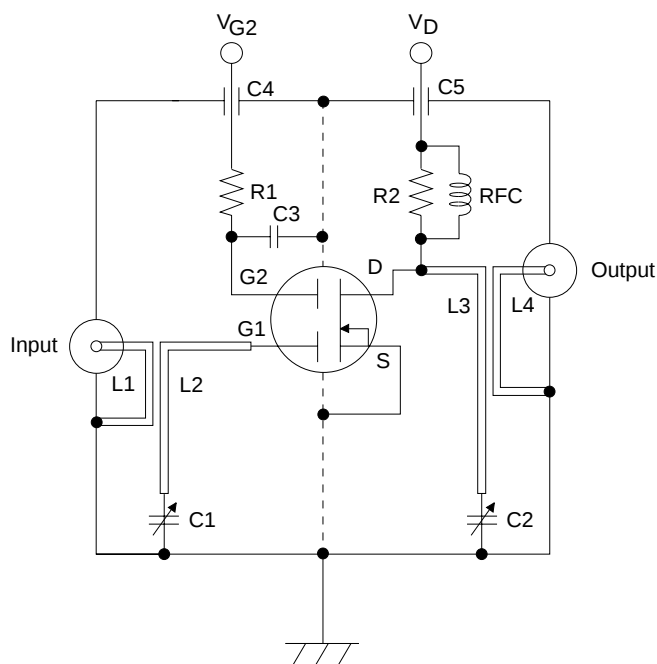


- **200 MHz Power Gain, Noise Figure Test Circuit**



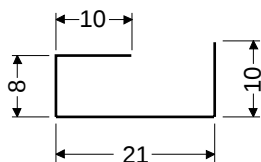
L1 : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 10mm, 2Turns
 L2 : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 10mm, 2Turns
 RFC : $\phi 1\text{mm}$ Enameled Copper Wire, Inside dia 5mm, 2Turns

• 900 MHz Power Gain, Noise Figure Test Circuit

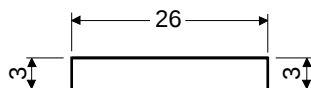


- C1, C2 : Variable Capacitor (10pF MAX)
 C3 : Disk Capacitor (1000pF)
 C4, C5 : Air Capacitor (1000pF)
 R1 : 47 k Ω
 R2 : 4.7 k Ω

L1:

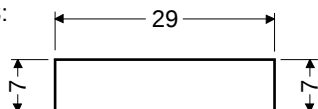


L2:

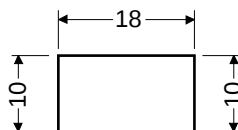


(ϕ 1mm Copper wire)
Unit : mm

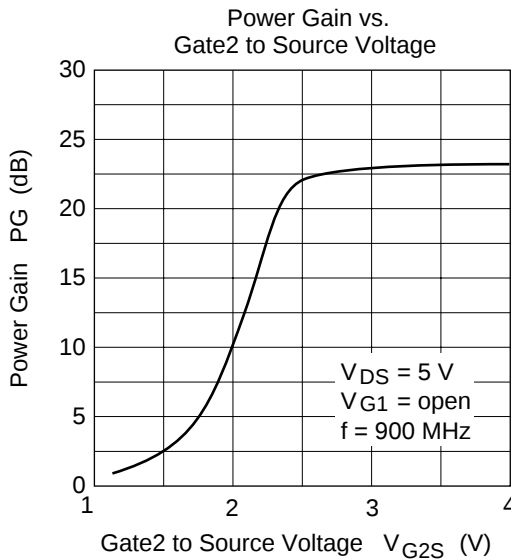
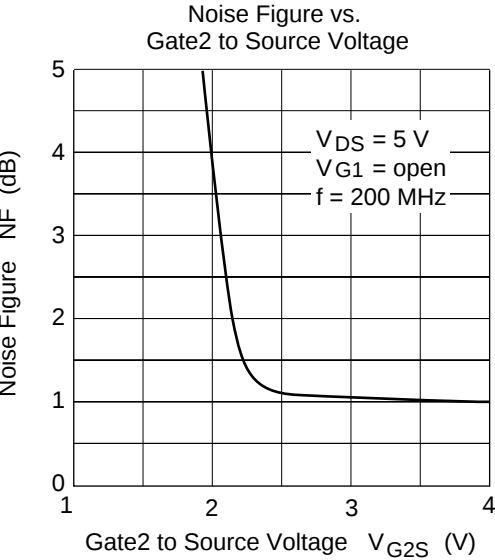
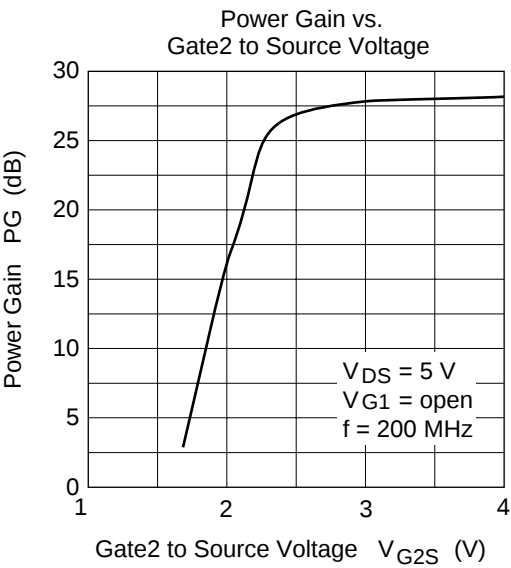
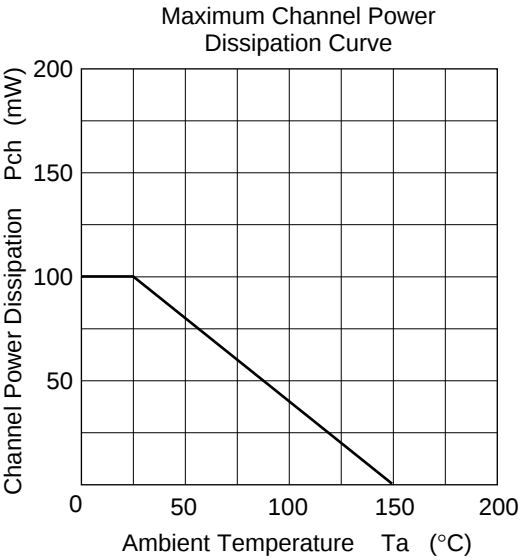
L3:

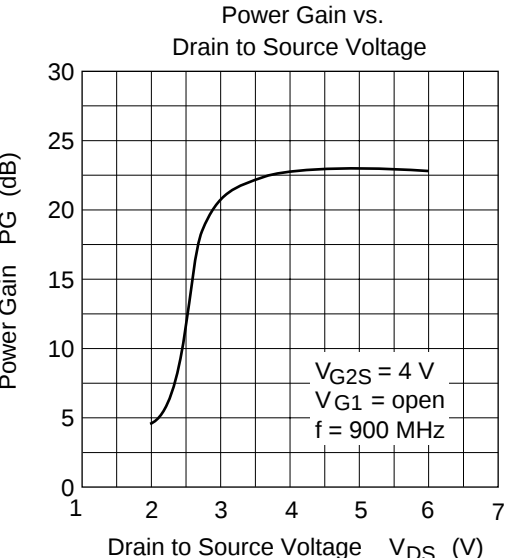
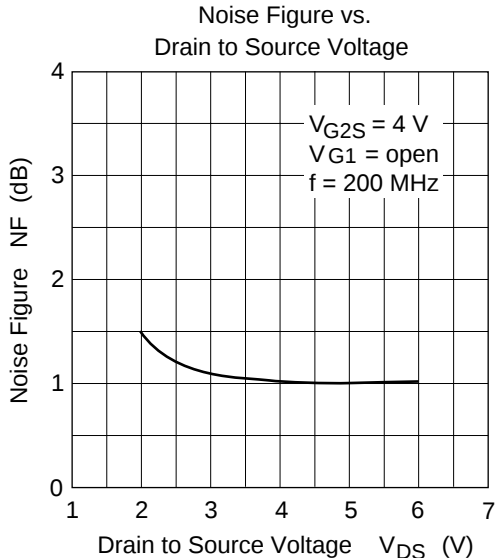
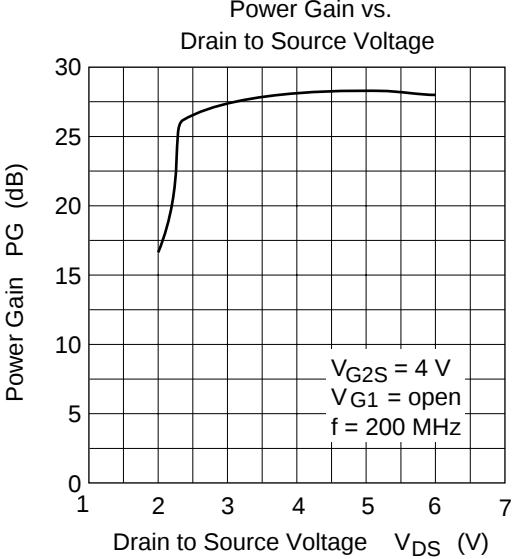
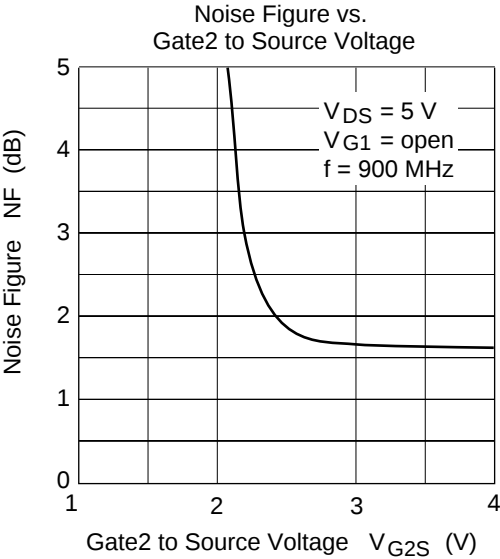


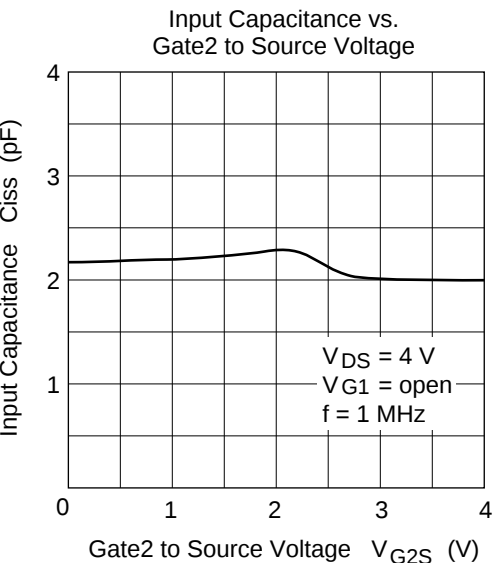
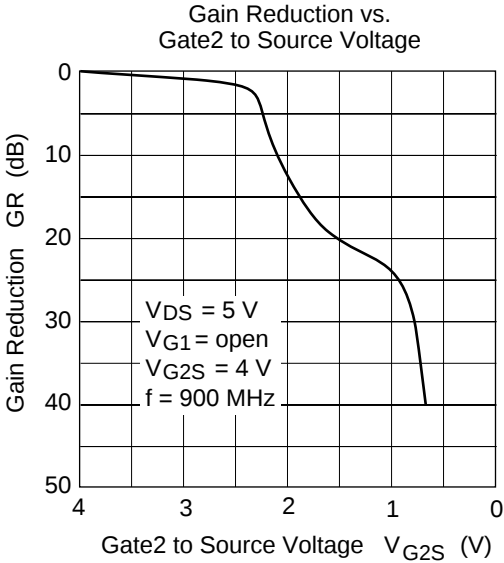
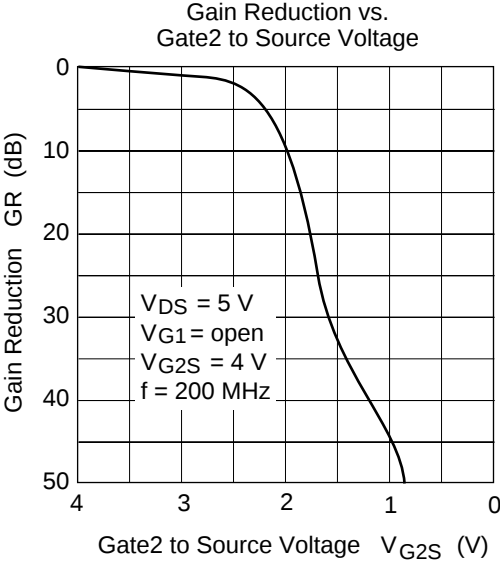
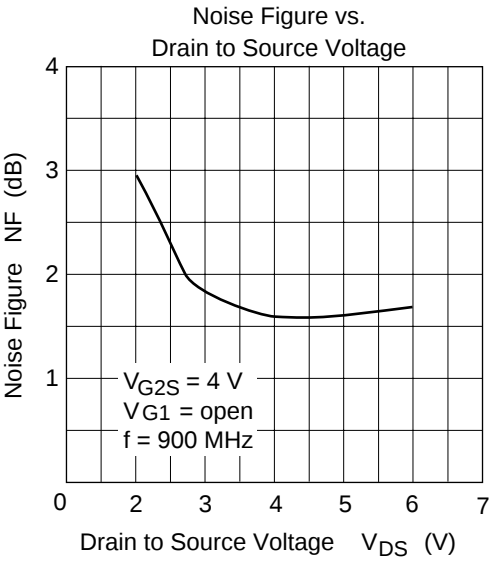
L4:



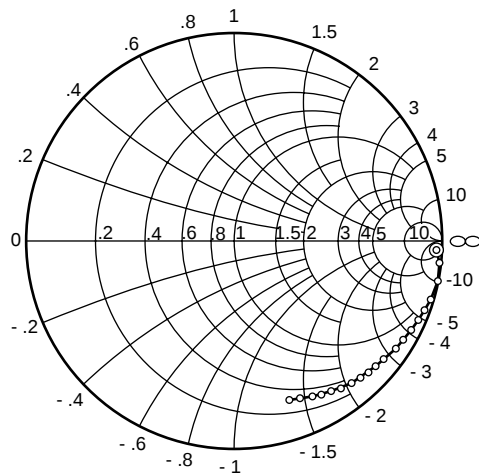
RFC : ϕ 1mm Copper wire with enamel 4turns inside dia 6mm







S11 Parameter vs. Frequency

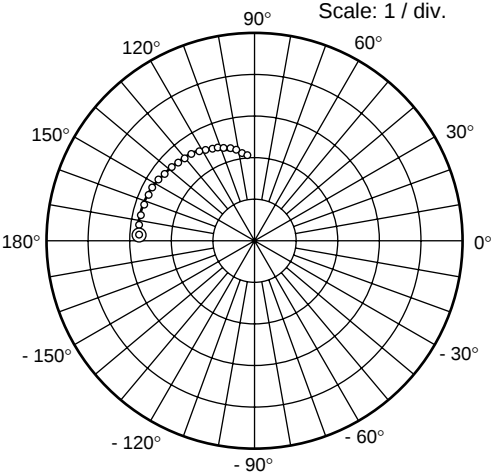


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$,
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S21 Parameter vs. Frequency

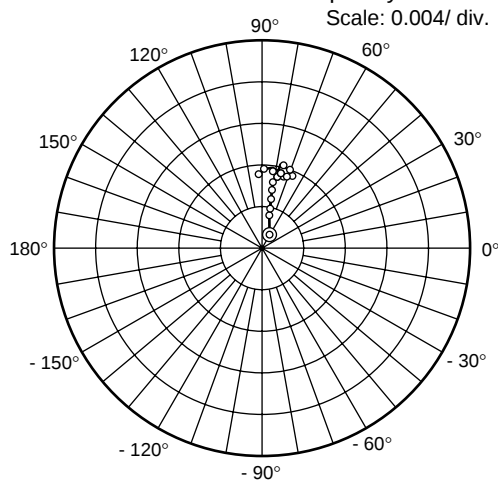


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$,
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S12 Parameter vs. Frequency

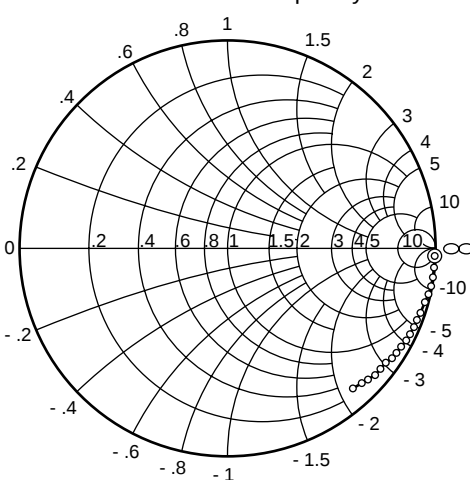


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$,
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)



S22 Parameter vs. Frequency



Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$,
 $Z_0 = 50\ \Omega$

50 to 1000 MHz (50 MHz step)

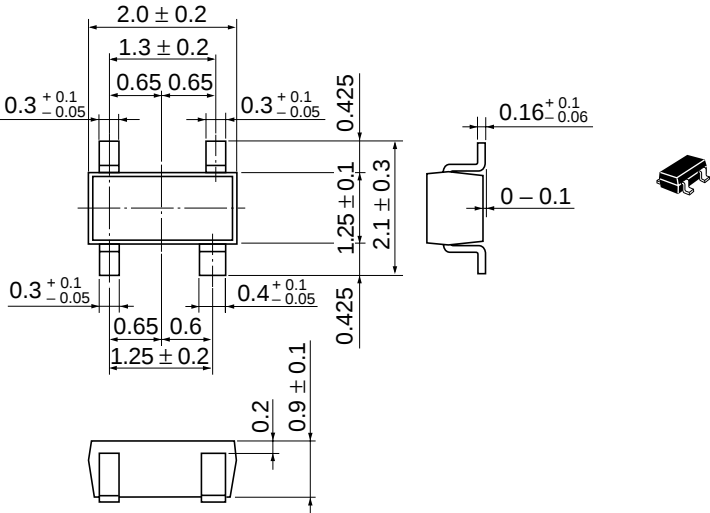


Sparameter ($V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V}$, $V_{G1} = \text{open}$, $Z_0 = 50\ \Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.998	-3.3	2.80	175.9	0.00106	58.8	0.990	-2.4
100	0.993	-7.2	2.78	170.9	0.00171	75.7	0.992	-4.7
150	0.991	-10.9	2.77	166.1	0.00253	75.1	0.991	-7.2
200	0.984	-15.0	2.74	161.2	0.00356	77.4	0.987	-9.6
250	0.978	-19.0	2.72	156.5	0.00442	78.2	0.985	-12.2
300	0.970	-22.8	2.68	151.8	0.00485	80.0	0.982	-14.7
350	0.958	-26.7	2.64	147.2	0.00576	74.7	0.978	-17.1
400	0.954	-30.3	2.60	142.7	0.00642	71.7	0.973	-19.6
450	0.945	-33.8	2.56	138.6	0.00689	73.3	0.968	-22.0
500	0.932	-37.5	2.50	134.1	0.00712	71.8	0.963	-24.2
550	0.920	-40.6	2.46	129.8	0.00765	70.7	0.958	-26.7
600	0.910	-44.3	2.41	125.7	0.00804	69.9	0.952	-28.9
650	0.900	-47.5	2.37	121.6	0.00798	69.1	0.947	-31.3
700	0.887	-50.9	2.31	117.8	0.00787	67.8	0.942	-33.4
750	0.870	-54.4	2.27	113.6	0.00785	70.8	0.936	-35.8
800	0.863	-57.6	2.22	110.0	0.00758	73.3	0.929	-37.9
850	0.853	-60.9	2.18	105.8	0.00721	75.2	0.924	-40.3
900	0.839	-63.6	2.12	102.2	0.00694	75.8	0.917	-42.5
950	0.827	-66.5	2.07	98.6	0.00716	88.1	0.912	-44.5
1000	0.819	-70.1	2.04	94.9	0.00667	92.7	0.906	-46.7

Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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