74LVU04

Hex unbuffered inverter

Rev. 7 — 18 September 2014 **Product data sheet**

1. General description

The 74LVU04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HCU04.

The 74LVU04 is a general purpose hex inverter. Each of the six inverters is a single stage with unbuffered outputs.

2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Linear amplifier
- Crystal oscillator
- Astable multivibrator

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVU04N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LVU04D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVU04DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVU04PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVU04BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

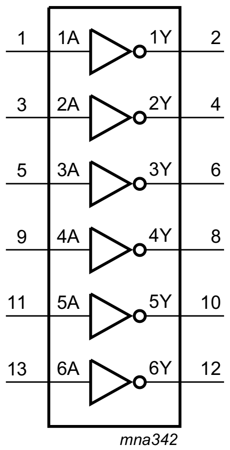

Fig 1. Logic symbol

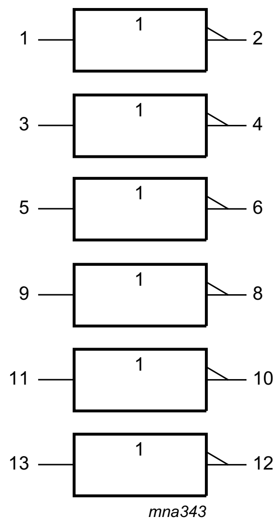

Fig 2. IEC logic symbol

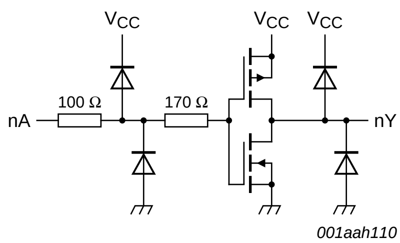

Fig 3. Circuit diagram (one inverter)

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6. Pinning information

6.1 Pinning

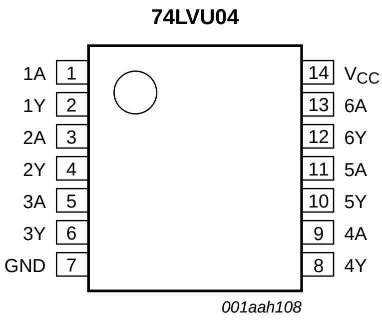
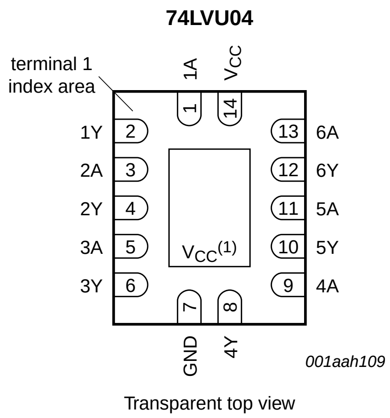


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Fig 5. Pin configuration DHVQFN14

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V_{CC}	14	supply voltage

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7. Functional description

Table 3. Function table[1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	$V_O = –0.5$ V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		DIP14 package	[2]	-	750	mW
		SO14 package	[3]	-	500	mW
		(T)SSOP14 package	[4]	-	500	mW
		DHVQFN14 package	[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

10. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.0	-	-	1.0	-	V
		V_{CC} = 2.0 V	1.6	-	-	1.6	-	V
		V_{CC} = 2.7 V to 3.6 V	2.4	-	-	2.4	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.8V_{CC}$	-	-	$0.8V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.2	-	0.2	V
		V_{CC} = 2.0 V	-	-	0.4	-	0.4	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.2V_{CC}$	-	$0.2V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = –100 µA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = –100 µA; V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.6	4.2	-	3.5	-	V

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Table 6. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100\ \mu A$; $V_{CC} = 1.2\ V$	-	0	-	-	-	V
		$I_O = 100\ \mu A$; $V_{CC} = 2.0\ V$	-	0	0.2	-	0.2	V
		$I_O = 100\ \mu A$; $V_{CC} = 2.7\ V$	-	0	0.2	-	0.2	V
		$I_O = 100\ \mu A$; $V_{CC} = 3.0\ V$	-	0	0.2	-	0.2	V
		$I_O = 100\ \mu A$; $V_{CC} = 4.5\ V$	-	0	0.2	-	0.2	V
		$I_O = 6\ mA$; $V_{CC} = 3.0\ V$	-	0.25	0.40	-	0.50	V
		$I_O = 12\ mA$; $V_{CC} = 4.5\ V$	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	20.0	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\ °C$.

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]						
		$V_{CC} = 1.2\ V$		-	35	-	-	-	ns
		$V_{CC} = 2.0\ V$		-	12	14	-	17	ns
		$V_{CC} = 2.7\ V$		-	9	10	-	13	ns
		$V_{CC} = 3.0\ V$ to $3.6\ V$; $C_L = 15\ pF$	[3]	-	6	-	-	-	ns
		$V_{CC} = 3.0\ V$ to $3.6\ V$	[3]	-	7	8	-	10	ns
		$V_{CC} = 4.5\ V$ to $5.5\ V$		-	-	7	-	9	ns
C_{PD}	power dissipation capacitance	$C_L = 50\ pF$; $f_i = 1\ MHz$; $V_I = GND$ to V_{CC}	[4]	-	18	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25\ °C$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\ V$).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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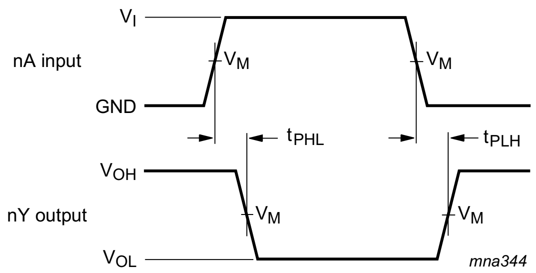
12. Waveforms



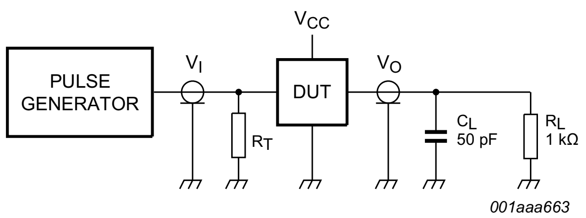
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input	
V_{CC}	V_I	t_r, t_f
< 2.7 V	V_{CC}	≤ 2.5 ns
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns
≥ 4.5 V	V_{CC}	≤ 2.5 ns

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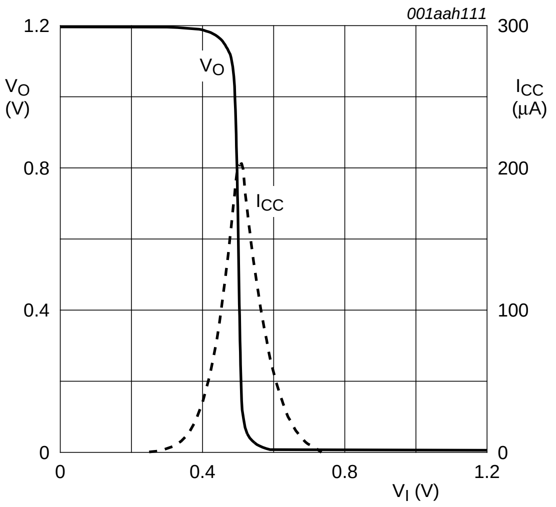
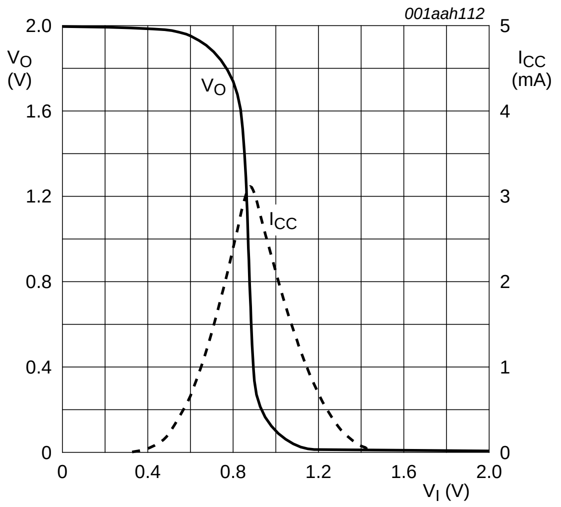
13. Transfer characteristics



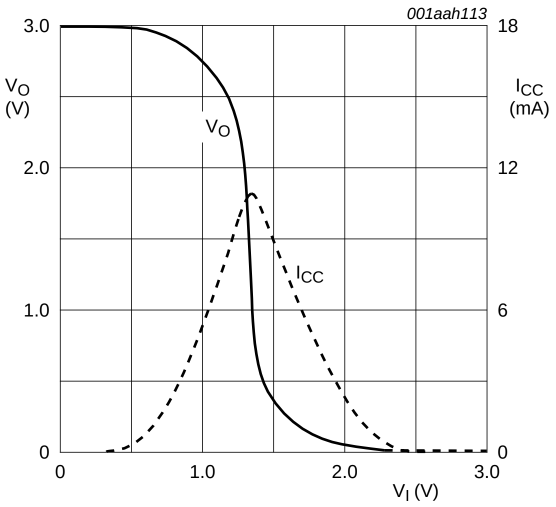
T_{amb} = 25 °C.

Fig 8. V_{CC} = 1.2 V; I_O = 0 A



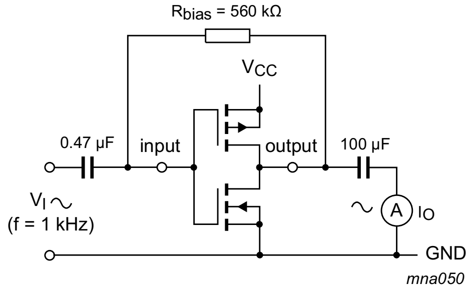
T_{amb} = 25 °C.

Fig 9. V_{CC} = 2.0 V; I_O = 0 A



T_{amb} = 25 °C.

Fig 10. V_{CC} = 3.0 V; I_O = 0 A



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz at V_O is constant

Fig 11. Test set-up for measuring forward transconductance

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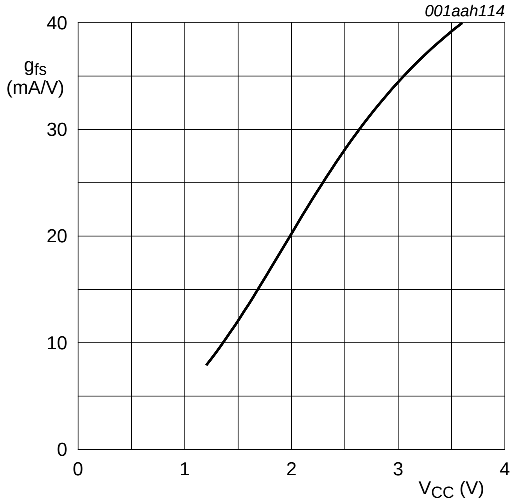

T_{amb} = 25 °C.

Fig 12. Forward transconductance as a function of the supply voltage

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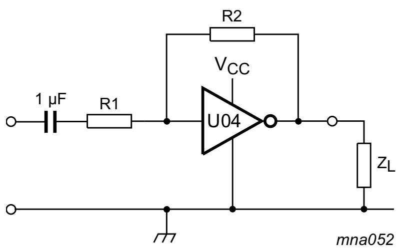
14. Application information

Some applications are:

- Linear amplifier (see Figure 13)
- In crystal oscillator design (see Figure 14)
- Astable multivibrator (see Figure 15)

Remark: All values given are typical unless otherwise specified.



Maximum $V_{o(p-p)} = V_{CC} - 1.5$ V centered at $0.5V_{CC}$.

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain

G_v = voltage gain

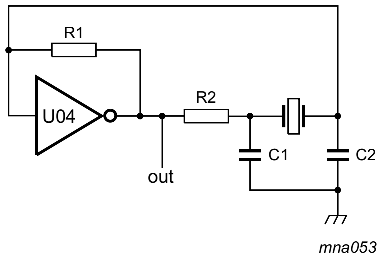
C_I, see Figure 16

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z_L > 10 kΩ; G_{ol} = 20 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Linear amplifier



C1 = 47 pF (typical)

C2 = 22 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical)

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f_i = 1 MHz).

See Table 10 and Table 11

Fig 14. Crystal oscillator

Table 10. External components for oscillator (f < 1 MHz)
All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	2.2 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	2.2 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	2.2 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	2.2 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF

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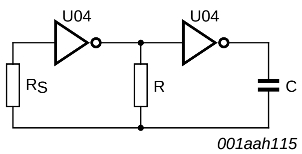
Table 11. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I_{CC}
	8.0 kΩ	minimum influence due to change in V_{CC}
6 kHz	1.0 kΩ	minimum required I_{CC}
	4.7 kΩ	minimum influence due to change in V_{CC}
10 kHz	0.5 kΩ	minimum required I_{CC}
	2.0 kΩ	minimum influence due to change in V_{CC}
14 kHz	0.5 kΩ	minimum required I_{CC}
	1.0 kΩ	minimum influence due to change in V_{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

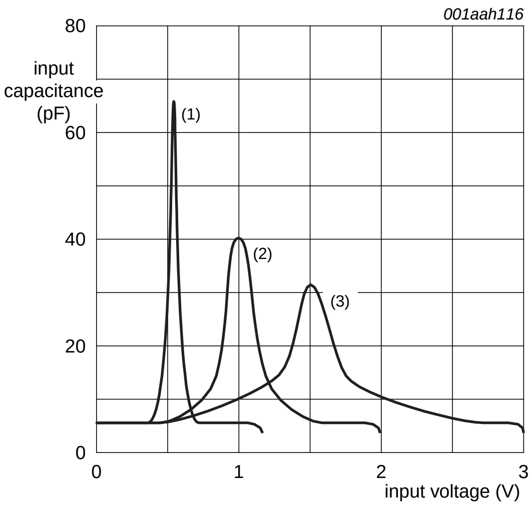


$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

$$R_S \approx 2 \times R$$

The average I_{CC} (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V_{CC} = 3.0 V.

Fig 15. Astable multivibrator



(1) V_{CC} = 1.2 V
(2) V_{CC} = 2.0 V
(3) V_{CC} = 3.0 V
T_{amb} = 25 °C.

Fig 16. Input capacitance as function of input voltage

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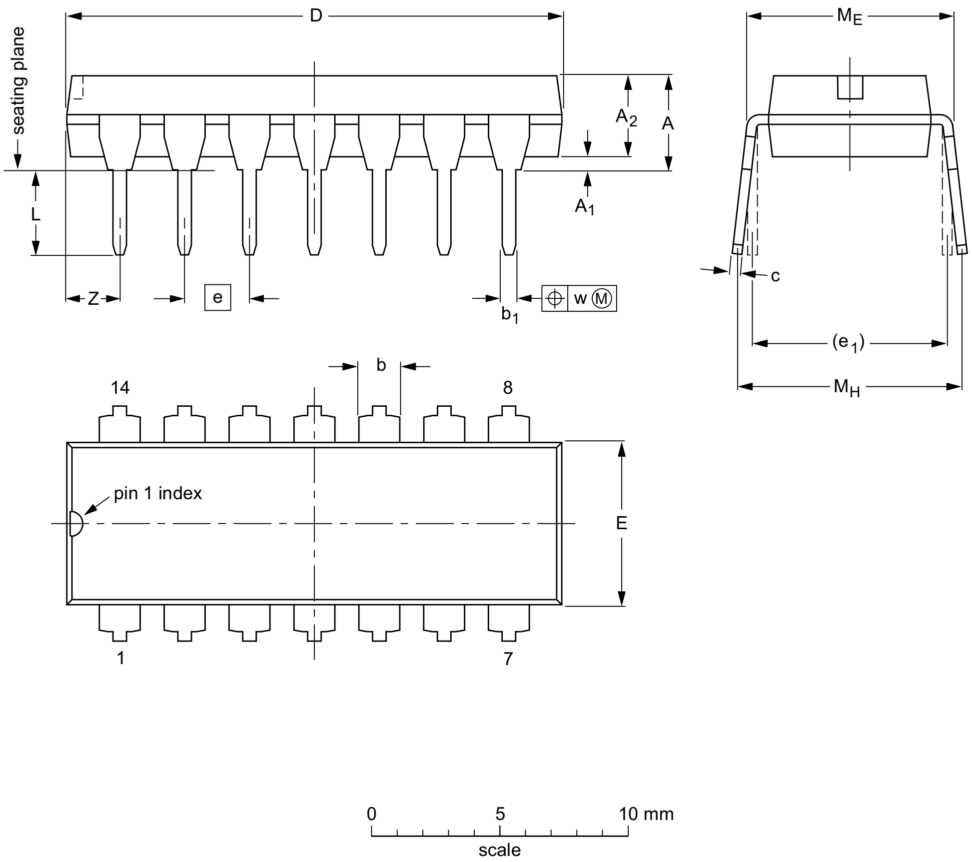
15. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 17. Package outline SOT27-1 (DIP14)

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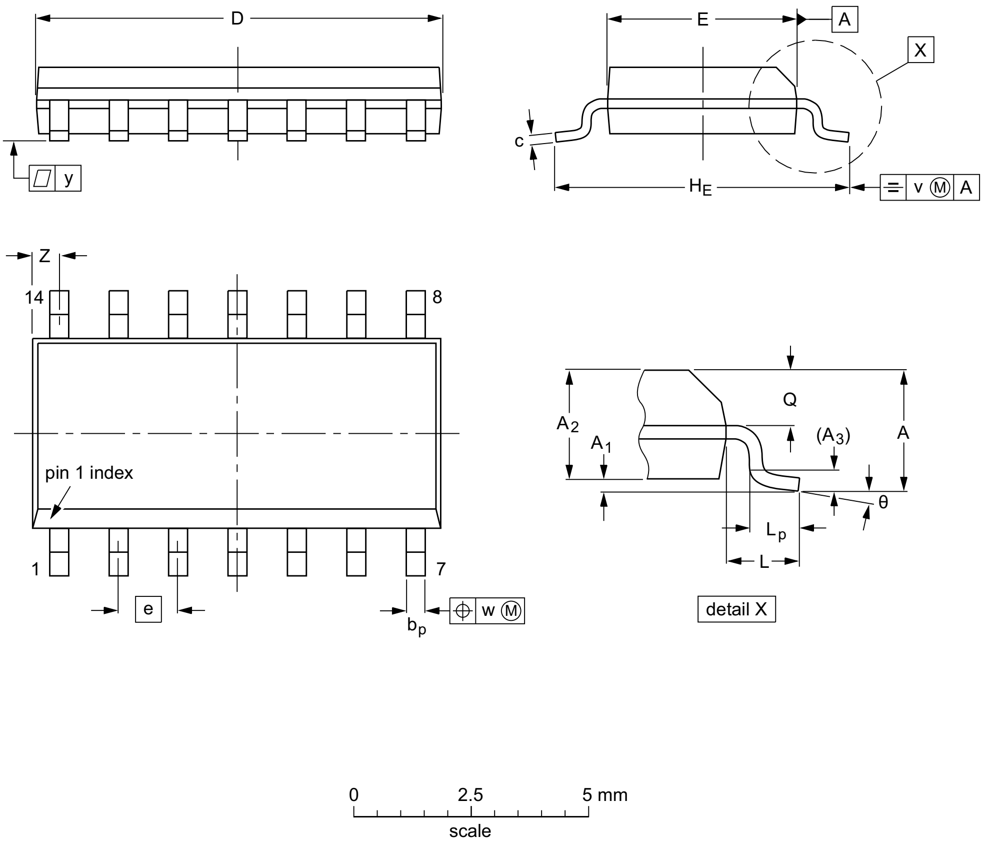
SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT108-1 (SO14)

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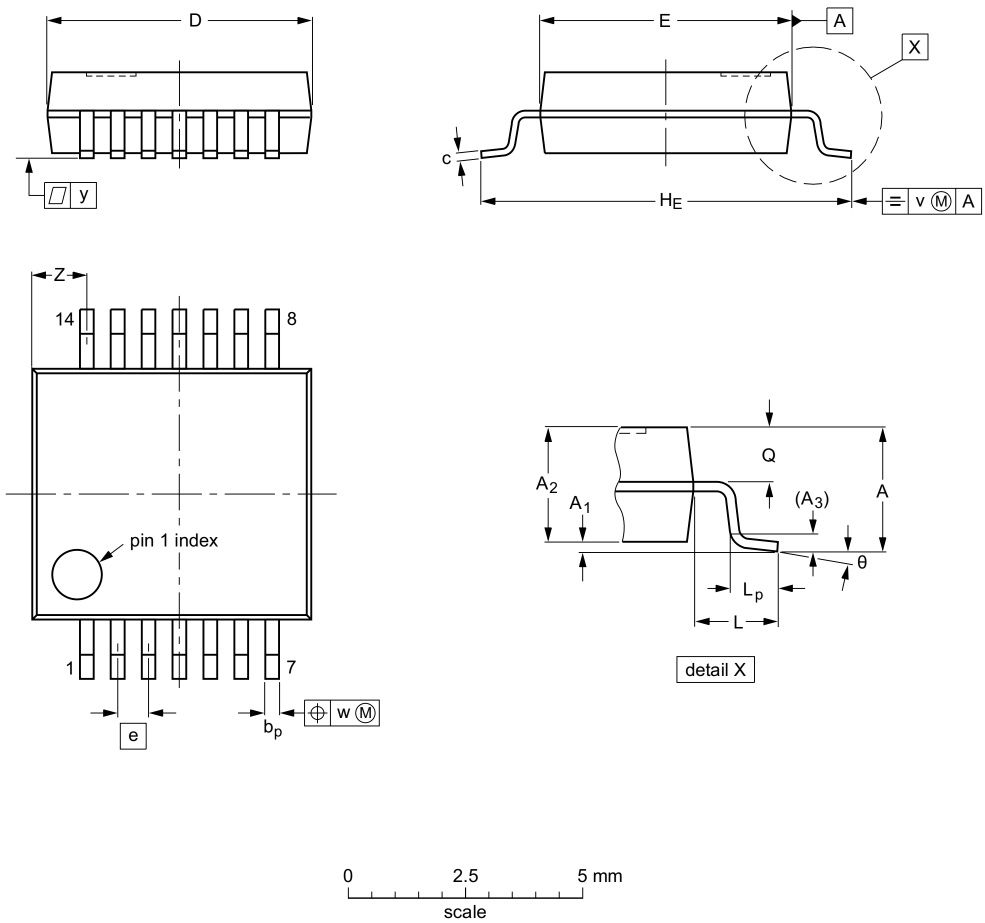
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

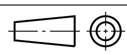
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT337-1 (SSOP14)

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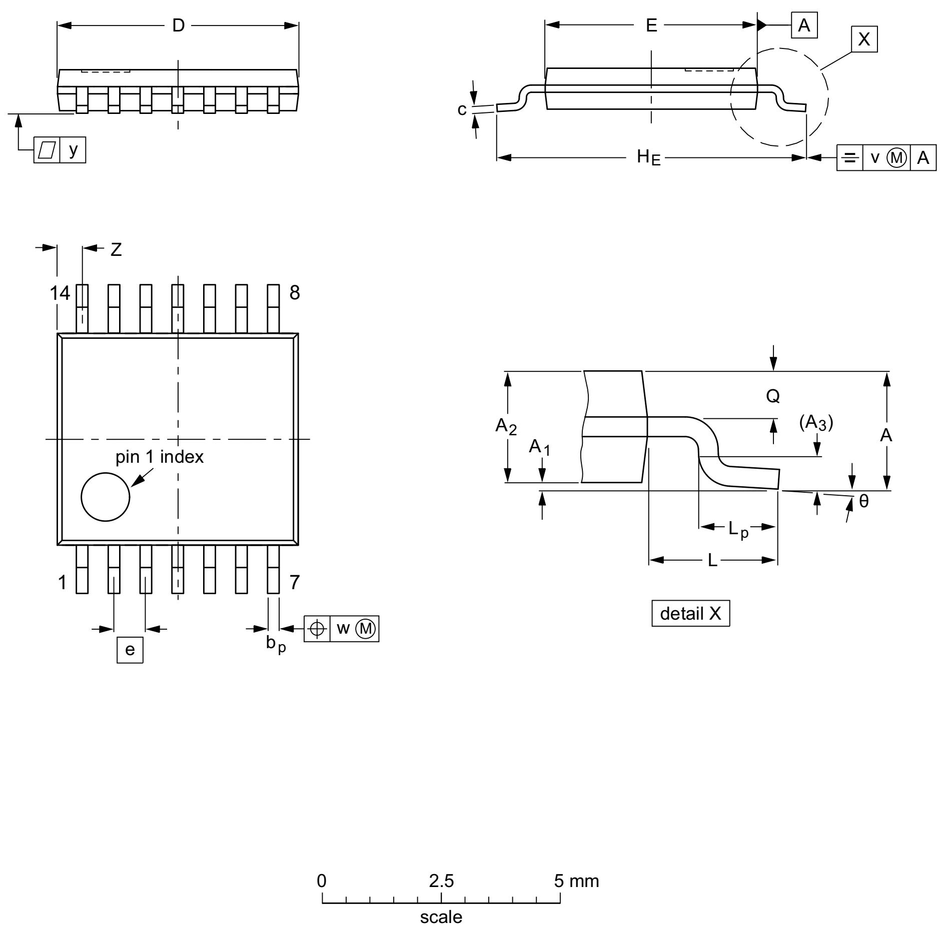
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 20. Package outline SOT402-1 (TSSOP14)

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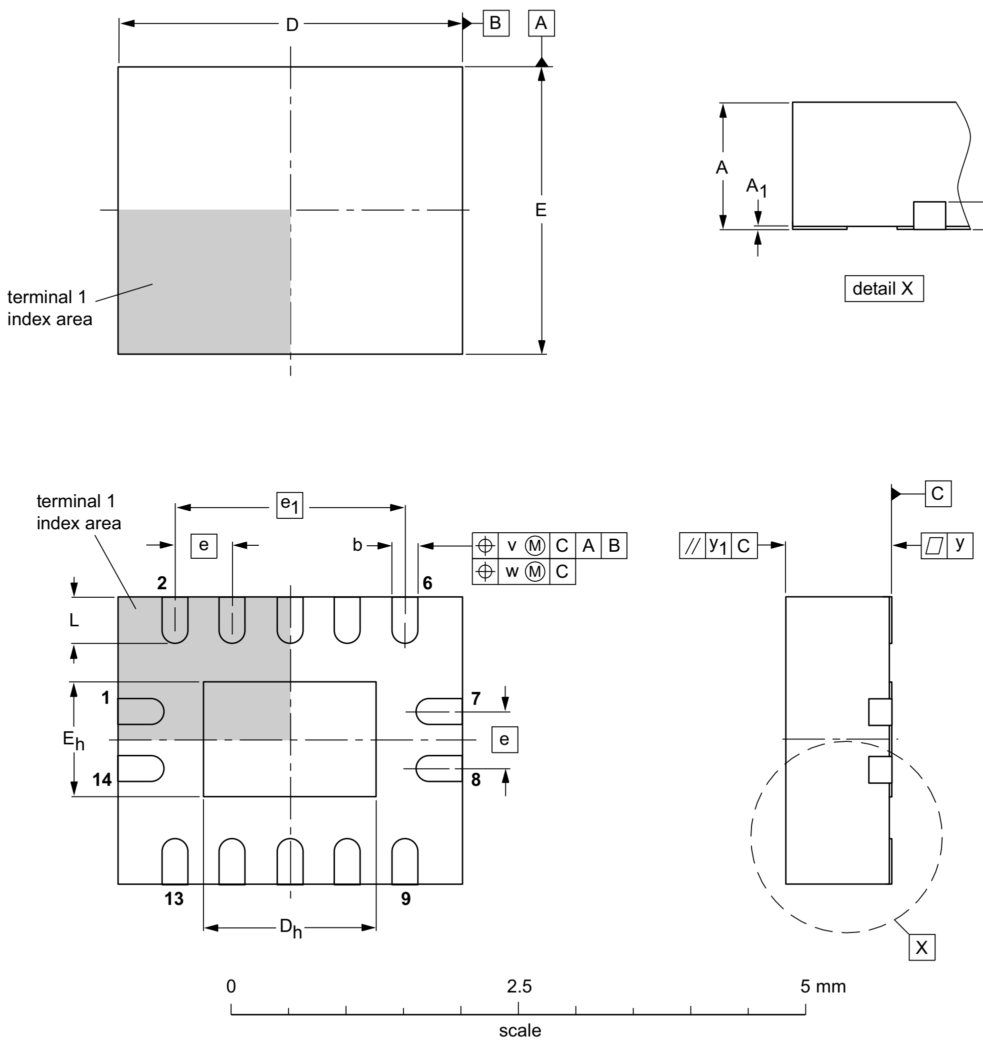
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 21. Package outline SOT762-1 (DHVQFN14)

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16. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVU04 v.7	20140918	Product data sheet	-	74LVU04 v.6
Modifications:	• Descriptive title changed to Hex unbuffered inverter.			
74LVU04 v.6	20071220	Product data sheet	-	74LVU04 v.5
74LVU04 v.5	20010111	Product specification	-	74LVU04 v.4
74LVU04 v.4	20001218	Product specification	-	74LVU04 v.3
74LVU04 v.3	19980420	Product specification	-	74LVU04 v.1
74LVU04 v.1	19970212	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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