

SN54F621, SN74F621 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDFS004B – D2932, MARCH 1987 – REVISED OCTOBER 1993

- Local Bus-Latch Capability
- Noninverting Logic
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

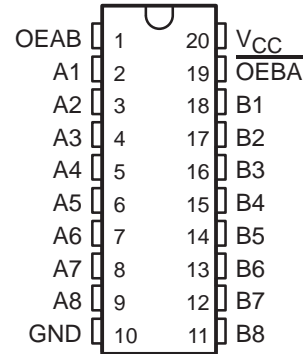
These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output enable (OEAB and $\overline{\text{OEBA}}$) inputs.

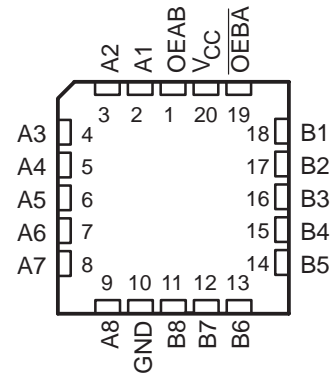
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54F621 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F621 is characterized for operation from 0°C to 70°C .

SN54F621 . . . J PACKAGE
SN74F621 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F621 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

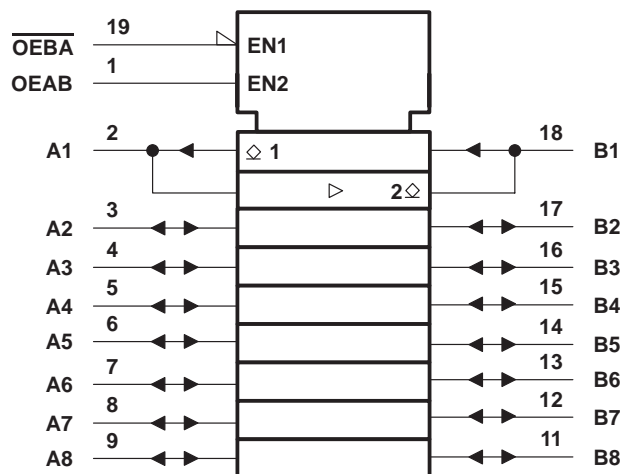
SN54F621, SN74F621

OCTAL BUS TRANSCEIVERS

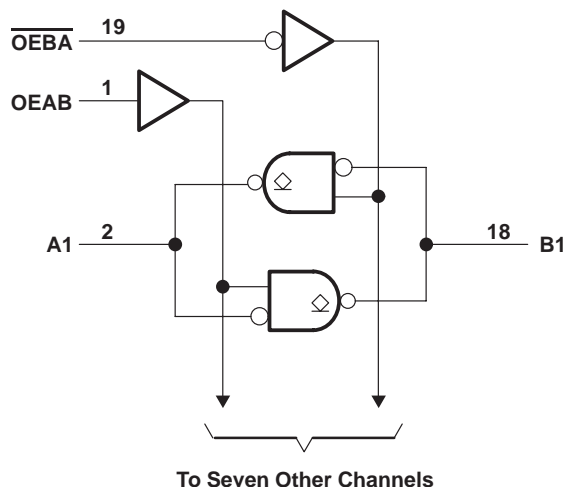
WITH OPEN-COLLECTOR OUTPUTS

SDFS004B – D2932, MARCH 1987 – REVISED OCTOBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1)	–1.2 V to 7 V
Input current range, I_{IK}	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to 5.5 V
Current into any output in the low state: SN54F621 (A1–A8)	40 mA
SN54F621 (B1–B8)	96 mA
SN74F621 (A1–A8)	48 mA
SN74F621 (B1–B8)	128 mA
Operating free-air temperature range: SN54F621	–55°C to 125°C
SN74F621	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		SN54F621			SN74F621			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{OH}	High-level output voltage			5.5			5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			– 18			– 18	mA
I_{OL}	Low-level output current	A1–A8		20	A1–A8		24	mA
		B1–B8		48	B1–B8		64	
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F621		SN74F621		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V,	I _I = − 18 mA	− 1.2		− 1.2		V
I _{OH}		V _{CC} = 4.5 V,	V _{OH} = 5.5 V	250		250		μA
V _{OL}	A1–A8	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.3	0.5			V
	I _{OL} = 24 mA				0.35	0.5		
	B1–B8		I _{OL} = 48 mA	0.38	0.55			
			I _{OL} = 64 mA			0.42	0.55	
I _I	A and B ports	V _{CC} = 5.5 V	V _I = 5.5 V	1		1		mA
	OEAB or $\overline{\text{OEBA}}$		V _I = 7 V	0.1		0.1		
I _{IH} ‡	A and B ports	V _{CC} = 5.5 V,	V _I = 2.7 V	70		70		μA
	OEAB or $\overline{\text{OEBA}}$			20		20		
I _{IL} ‡	A and B ports	V _{CC} = 5.5 V,	V _I = 0.5 V	− 0.65		− 0.65		mA
	OEAB or $\overline{\text{OEBA}}$			− 0.6		− 0.6		
I _{CCH}		V _{CC} = 5.5 V		105	140	105	140	mA
I _{CCL}		V _{CC} = 5.5 V		105	140	105	140	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			‘F621			SN54F621		SN74F621		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	6	9.5	12	5.5	13	5.5	13	ns
t _{PHL}			2.5	3.8	8	2	8.5	2	8.5	
t _{PLH}	B	A	6	9	12	5.5	12.5	5.5	12.5	ns
t _{PHL}			2.5	4	7.5	2	8	2	8	
t _{PLH}	OEBA	A	6	10	13.5	5.5	14	5.5	14	ns
t _{PHL}			3.5	6.5	10.5	2.5	11	2.5	11	
t _{PLH}	OEAB	B	7	12	15	6	17	6	17	ns
t _{PHL}			3.5	6.5	9.5	3	10	3	10	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54F621J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74F621DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74F621DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74F621N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SNJ54F621FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54F621J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SNJ54F621W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

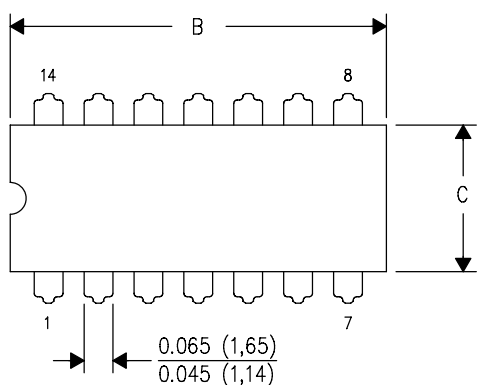
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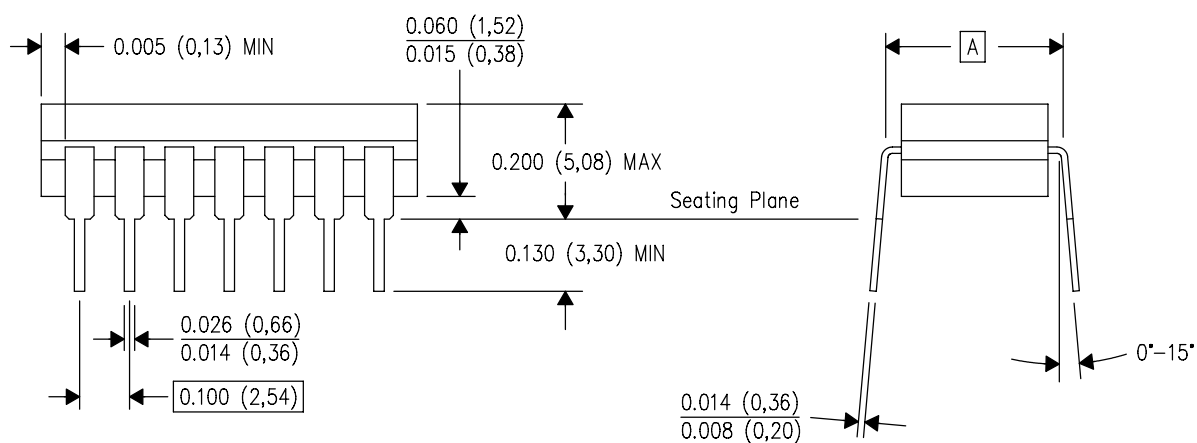
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



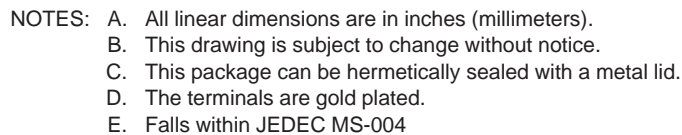
PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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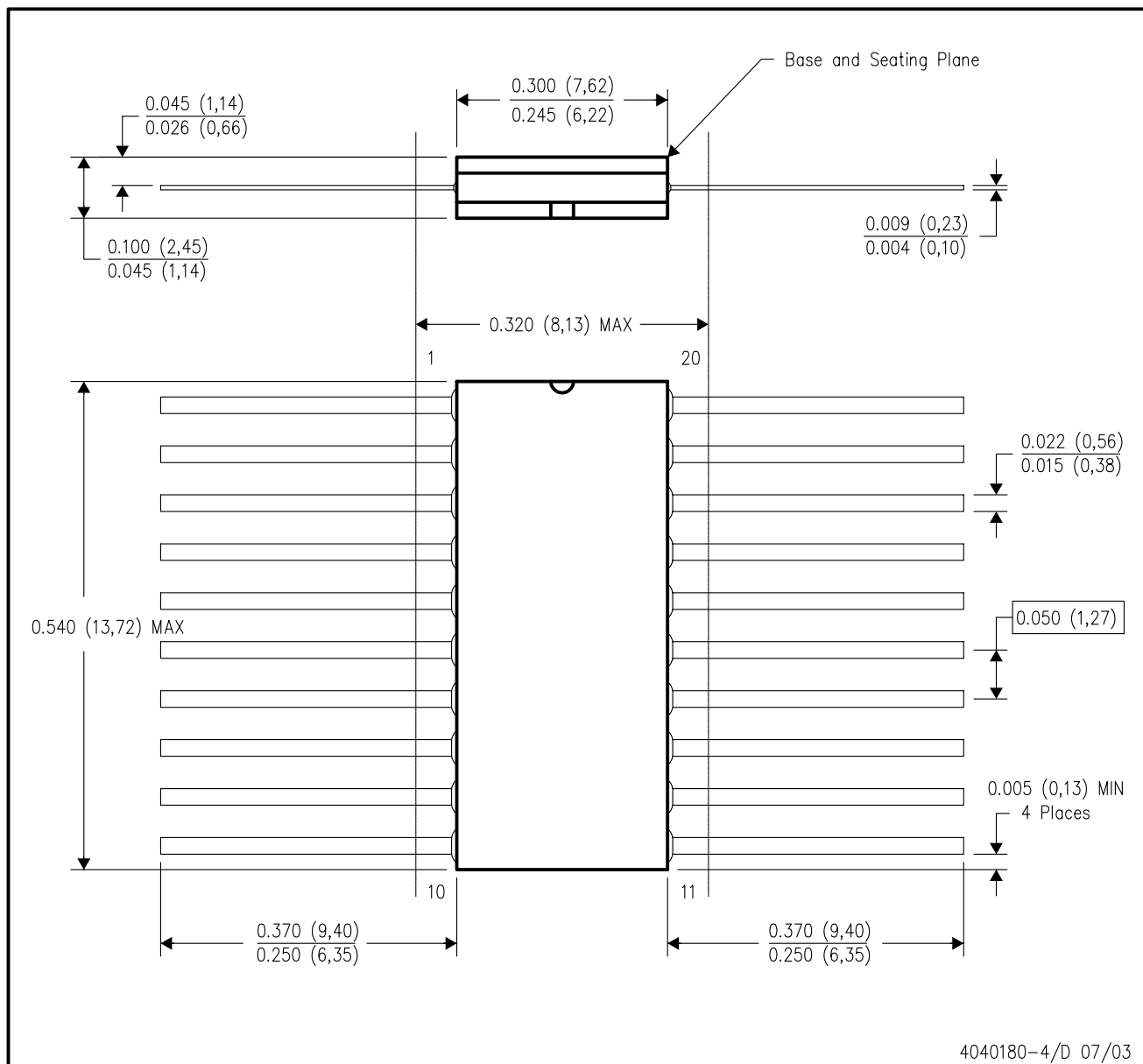
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

28 TERMINAL SHOWN



W (R-GDFP-F20)

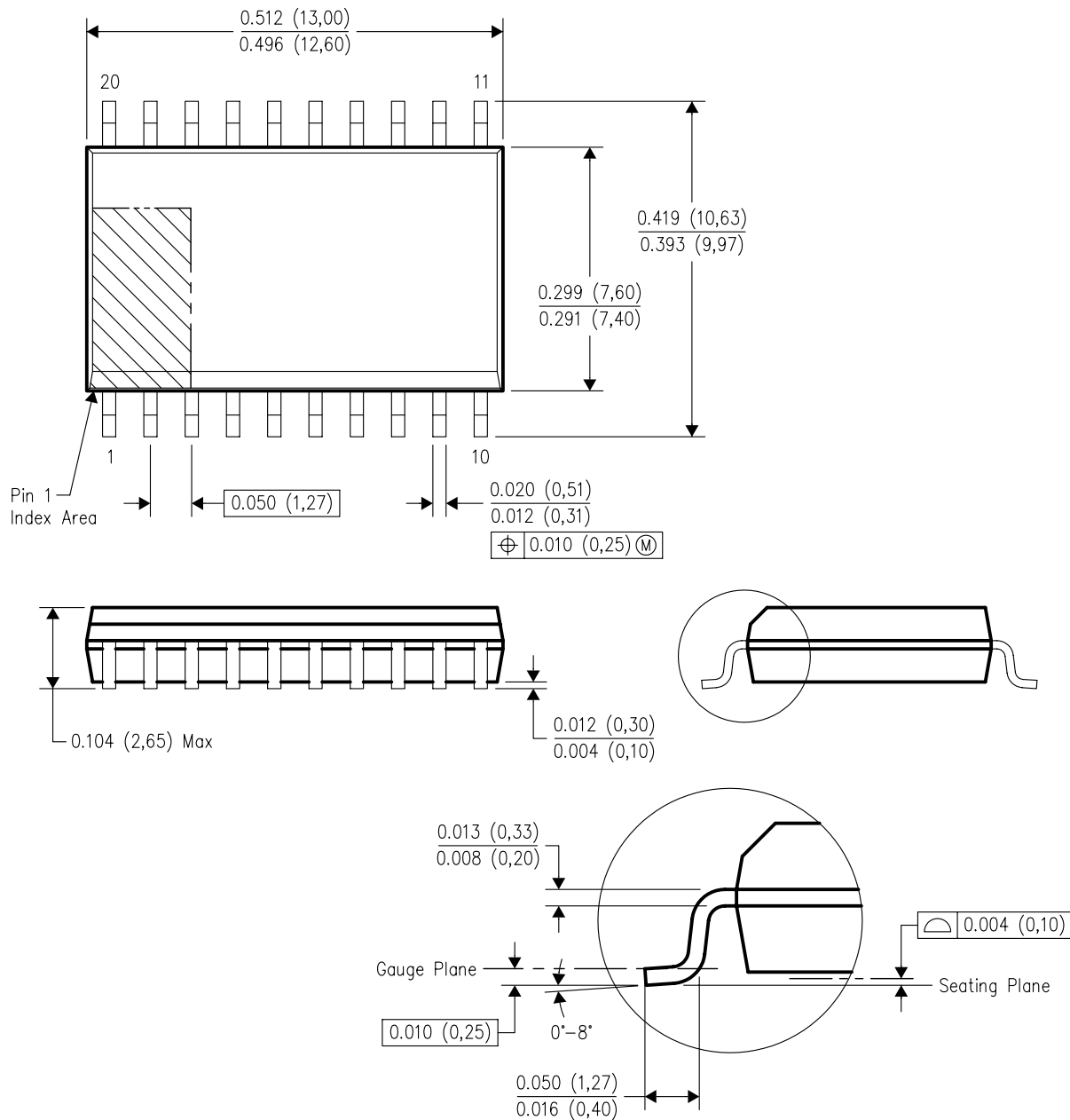
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



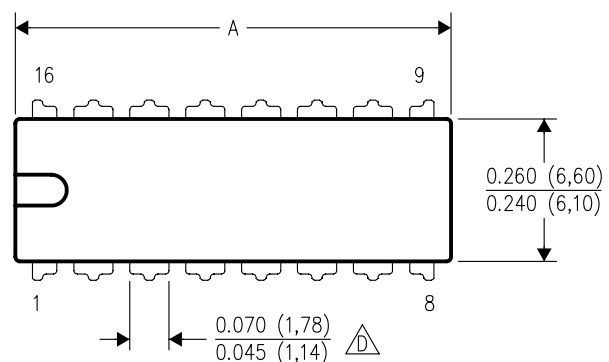
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- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

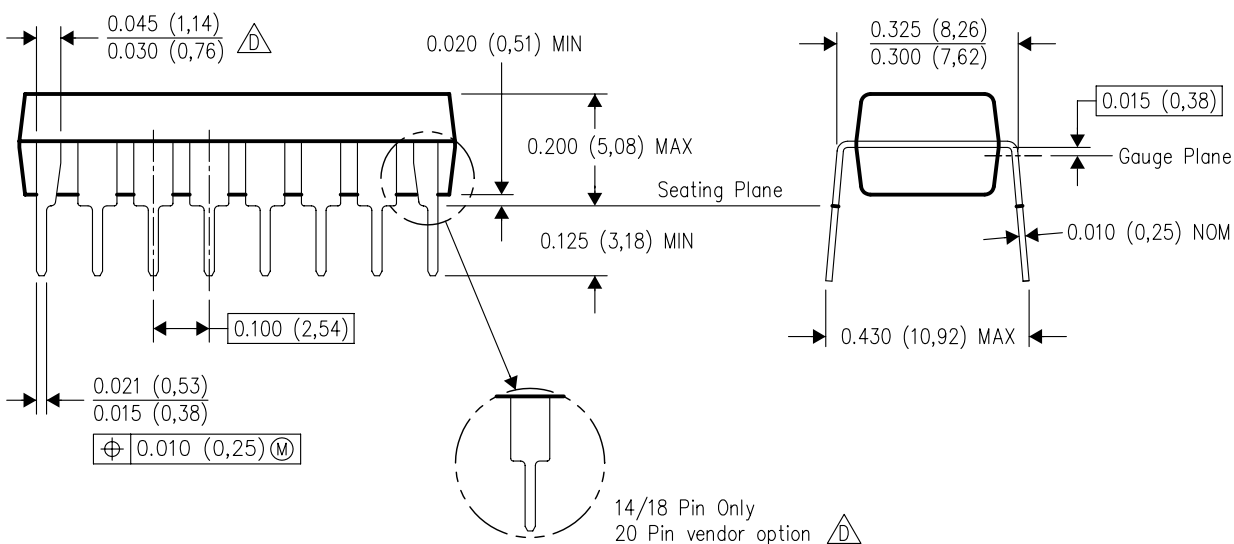
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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