

DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

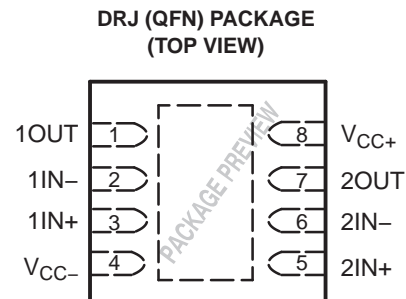
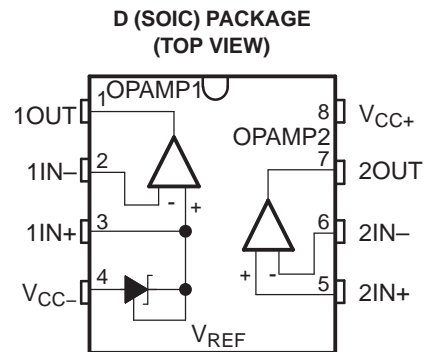
Check for Samples: [TL103W](#), [TL103WA](#)

FEATURES

- **OPERATIONAL AMPLIFIER**
 - Low Offset Voltage Max of:
 - TL103WA...3 mV (25°C) and 5 mV (Full Temperature)
 - TL103W...4 mV (25°C) and 5 mV (Full Temperature)
 - Low Supply Current...350 μ A/Channel (Typ)
 - Unity Gain Bandwidth...0.9 MHz (Typ)
 - Input Common-Mode Range Includes GND
 - Large Output-Voltage Swing... 0 V to $V_{CC} - 1.5$ V
 - Wide Supply-Voltage Range...3 V to 32 V
 - 2-kV ESD Protection (HBM)
- **VOLTAGE REFERENCE**
 - Fixed 2.5-V Reference
 - Tight Tolerance Max of:
 - TL103WA...0.4% (25°C) and 0.8% (Full Temperature)
 - TL103W . . . 0.7% (25°C) and 1.4% (Full Temperature)
 - Low Temperature Drift...7 mV (Typ) Over Operating Temperature Range
 - Wide Sink-Current Range . . . 0.5 mA (Typ) to 100 mA
 - Output Impedance...0.2 Ω (Typ)

TYPICAL APPLICATIONS

- Battery Chargers
- Switch-Mode Power Supplies
- Linear Voltage Regulation
- Data-Acquisition Systems



NOTE: Exposed thermal pad is connected internally to V_{CC-} via die attach.

DESCRIPTION/ORDERING INFORMATION

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OPAMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OPAMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from -40°C to 105°C .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T_A	MAX V_{IO} AND V_{REF} TOLERANCE (25°C)	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	A grade 3 mV, 0.4%	QFN (DRJ)	Reel of 1000	TL103WAIDRJ	PREVIEW
		SOIC (D)	Tube of 75	TL103WAID	Z103WA
			Reel of 2500	TL103WAIDR	
	Standard grade 4 mV, 0.7%	QFN (DRJ)	Reel of 1000	TL103WIDRJ	PREVIEW
		SOIC (D)	Tube of 75	TL103WID	Z103W
			Reel of 2500	TL103WIDR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

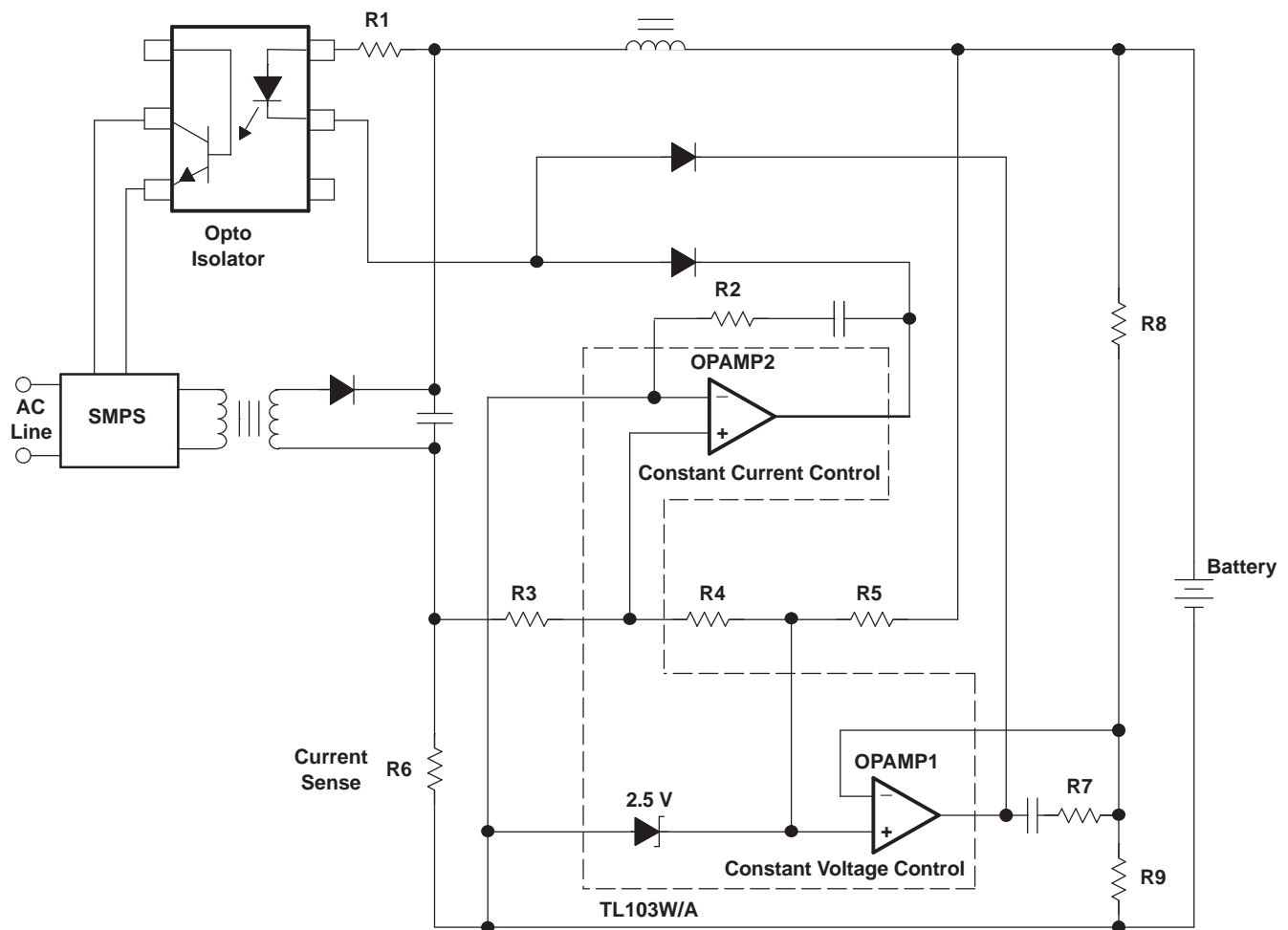
Typical Application Circuit

Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage		36	V
V _{ID}	Operational amplifier input differential voltage		36	V
V _I	Operational amplifier input voltage range	–0.3	36	V
I _{KA}	Voltage reference cathode current		100	mA
θ _{JA}	Package thermal impedance	D package ^{(2) (3)}		97
		DRJ package ^{(2) (4)}		TBD
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/θ_{JA}. Selecting the maximum of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Supply voltage	3	32	V
I _K	Cathode current	1	100	mA
T _A	Operating free-air temperature	–40	105	°C

OPAMP1, Operational Amplifier With Noninverting Input Connected to the Internal V_{REF}

Electrical Characteristics

$V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{icm} = 0\text{ V}$	25°C		1	4	mV
			Full range			5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C		0.5	3	
			Full range			5	
αV_{IO}	Input offset-voltage drift		25°C		7		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current (negative input)		25°C		20		nA
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{icm} = 0\text{ V}$	25°C		100		V/mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V , $V_{icm} = 0\text{ V}$	25°C	65	100		dB
$I_{O(\text{source})}$	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$	25°C	20	40		mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
$I_{O(\text{sink})}$	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$		12	50		μA
V_{OH}	High-level output voltage	$V_{CC} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 2 V , unity gain	25°C	0.2	0.4		V/ μs
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_V = 20\text{ dB}$	25°C		0.02		%

OPAMP2, Independent Operational Amplifier

Electrical Characteristics

 $V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $V_O = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{icm} = 0\text{ V}$	25°C		1	4	mV
			Full range			5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C		0.5	3	
			Full range			5	
αV_{IO}	Input offset voltage drift		25°C		7		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current		25°C		2	75	nA
			Full range			150	
I_{IB}	Input bias current		25°C		20	150	nA
			Full range			200	
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1.4\text{ V}$ to 11.4 V	25°C	50	100		V/mV
			Full range	25			
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V	25°C	65	100		dB
V_{ICR}	Input common-mode voltage range	$V_{CC+} = 30\text{ V}^{(1)}$	25°C	0		$V_{CC+} - 1.5$	V
			Full range	0		$V_{CC+} - 2$	
CMRR	Common-mode rejection ratio		25°C	70	85		dB
			Full range	60			
$I_{O(\text{source})}$	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$	25°C	20	40		mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
$I_{O(\text{sink})}$	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$		12	50		μA
V_{OH}	High-level output voltage	$V_{CC} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 3 V , unity gain	25°C	0.2	0.4		V/ μs
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_V = 20\text{ dB}$	25°C		0.02		%
V_n	Equivalent input noise voltage	$V_{CC} = 30\text{ V}$, $R_S = 100\text{ }\Omega$, $f = 1\text{ kHz}$	25°C		50		nV/ $\sqrt{\text{Hz}}$

(1) The input common-mode voltage of either input should not be allowed to go below -0.3 V . The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either input can go to $V_{CC+} + 0.3\text{ V}$ (but $\leq 36\text{ V}$) without damage.

Voltage Reference

Electrical Characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
V _{REF}	Reference voltage	I _K = 10 mA	25°C	2.482	2.5	2.518	V
			Full range	2.465		2.535	
	TL103WA	I _K = 10 mA	25°C	2.49	2.5	2.51	
			Full range	2.48		2.52	
ΔV _{REF}	Reference input voltage deviation over temperature range	V _{KA} = V _{REF} , I _K = 10 mA	Full range		7	30	mV
I _{min}	Minimum cathode current for regulation	V _{KA} = V _{REF}	25°C		0.5	1	mA
z _{ka}	Dynamic impedance ⁽¹⁾	V _{KA} = V _{REF} , ΔI _K = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω

(1) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$.

Total Device

Electrical Characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{CC}	Total supply current, excluding cathode-current reference	V _{CC+} = 5 V, No load	Full range		0.7	1.2	mA
		V _{CC+} = 30 V, No load				2	

REVISION HISTORY

Changes from Revision J (September 2010) to Revision K	Page
• Changed topside marking to fix typo Z103WQ to Z103WA	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL103WAID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL103WIDR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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