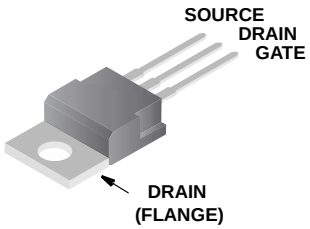
# 75A, 60V, 0.0075 Ohm, N-Channel, Logic Level UltraFET® Power MOSFET

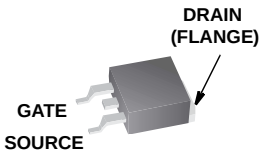
## Packaging

JEDEC TO-220AB



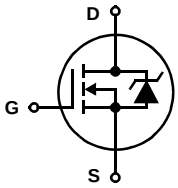

HUFA76445P3

JEDEC TO-263AB




HUFA76445S3S

## Symbol




## Features

- Ultra Low On-Resistance
  - $r_{DS(ON)}$ = 0.0065Ω, $V_{GS}$ = 10V
  - $r_{DS(ON)}$ = 0.0075Ω, $V_{GS}$ = 5V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs $R_{GS}$ Curves

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HUFA76445P3 | TO-220AB | 76445P |
| HUFA76445S3S | TO-263AB | 76445S |

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUFA76445S3ST.

## Absolute Maximum Ratings $T_C$ = 25°C, Unless Otherwise Specified

| | | HUFA76445P3, HUFA76445S3S | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DSS}$ | 60 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 60 | V |
| Gate to Source Voltage | $V_{GS}$ | ±16 | V |
| Drain Current | | | |
| Continuous ($T_C$ = 25°C, $V_{GS}$ = 5V) | $I_D$ | 75 | A |
| Continuous ($T_C$ = 25°C, $V_{GS}$ = 10V) (Figure 2) | $I_D$ | 75 | A |
| Continuous ($T_C$ = 100°C, $V_{GS}$ = 5V) | $I_D$ | 75 | A |
| Continuous ($T_C$ = 100°C, $V_{GS}$ = 4.5V) (Figure 2) | $I_D$ | 75 | A |
| Pulsed Drain Current | $I_{DM}$ | Figure 4 | |
| Pulsed Avalanche Rating | UIS | Figures 6, 17, 18 | |
| Power Dissipation | $P_D$ | 310 | W |
| Derate Above 25°C | | 2.08 | W/°C |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 175 | °C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | °C |
| Package Body for 10s, See Techbrief TB334 | $T_{pkg}$ | 260 | °C |

NOTES:

1. $T_J$ = 25°C to 150°C.

***CAUTION:*** *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/**

**Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.**

**All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.**

©2002 Fairchild Semiconductor Corporation

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **OFF STATE SPECIFICATIONS** | | | | | | | |
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250μA, $V_{GS}$ = 0V (Figure 12) | | 60 | - | - | V |
| | | $I_D$ = 250μA, $V_{GS}$ = 0V , $T_C$ = -40$^o$C (Figure 12) | | 55 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 55V, $V_{GS}$ = 0V | | - | - | 1 | μA |
| | | $V_{DS}$ = 50V, $V_{GS}$ = 0V, $T_C$ = 150$^o$C | | - | - | 250 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±16V | | - | - | ±100 | nA |
| **ON STATE SPECIFICATIONS** | | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA (Figure 11) | | 1 | - | 3 | V |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 75A, $V_{GS}$ = 10V (Figures 9, 10) | | - | 0.0054 | 0.0065 | Ω |
| | | $I_D$ = 75A, $V_{GS}$ = 5V (Figure 9) | | - | 0.0063 | 0.0075 | Ω |
| | | $I_D$ = 75A, $V_{GS}$ = 4.5V (Figure 9) | | - | 0.0066 | 0.008 | Ω |
| **THERMAL SPECIFICATIONS** | | | | | | | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | TO-220 and TO-263 | | - | - | 0.48 | $^o$C/W |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | | - | - | 62 | $^o$C/W |
| **SWITCHING SPECIFICATIONS** ($V_{GS}$ = 4.5V) | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 30V, $I_D$ = 75A<br>$V_{GS}$ = 4.5V, $R_{GS}$ = 2.2Ω<br>(Figures 15, 21, 22) | | - | - | 515 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 18 | - | ns |
| Rise Time | $t_r$ | | | - | 325 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 39 | - | ns |
| Fall Time | $t_f$ | | | - | 135 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 260 | ns |
| **SWITCHING SPECIFICATIONS** ($V_{GS}$ = 10V) | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 30V, $I_D$ = 75A<br>$V_{GS}$ = 10V,<br>$R_{GS}$ = 2.4Ω<br>(Figures 16, 21, 22) | | - | - | 205 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 12 | - | ns |
| Rise Time | $t_r$ | | | - | 126 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 62 | - | ns |
| Fall Time | $t_f$ | | | - | 135 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | 295 | - | ns |
| **GATE CHARGE SPECIFICATIONS** | | | | | | | |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 10V | $V_{DD}$ = 30V,<br>$I_D$ = 75A,<br>$I_{g(REF)}$ = 1.0mA<br>(Figures 14, 19, 20) | - | 124 | 150 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0V to 5V | | - | 68 | 81 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 1V | | - | 5 | 6 | nC |
| Gate to Source Gate Charge | $Q_{gs}$ | | | - | 14 | - | nC |
| Gate to Drain “Miller” Charge | $Q_{gd}$ | | | - | 30 | - | nC |
| **CAPACITANCE SPECIFICATIONS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V,<br>f = 1MHz<br>(Figure 13) | | - | 4965 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 1250 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 150 | - | pF |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 75A | - | - | 1.25 | V |
| | | $I_{SD}$ = 35A | - | - | 1.00 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 75A, $dI_{SD}/dt$ = 100A/μs | - | - | 100 | ns |
| Reverse Recovered Charge | $Q_{RR}$ | $I_{SD}$ = 75A, $dI_{SD}/dt$ = 100A/μs | - | - | 260 | nC |

©2002 Fairchild Semiconductor Corporation

## Typical Performance Curves

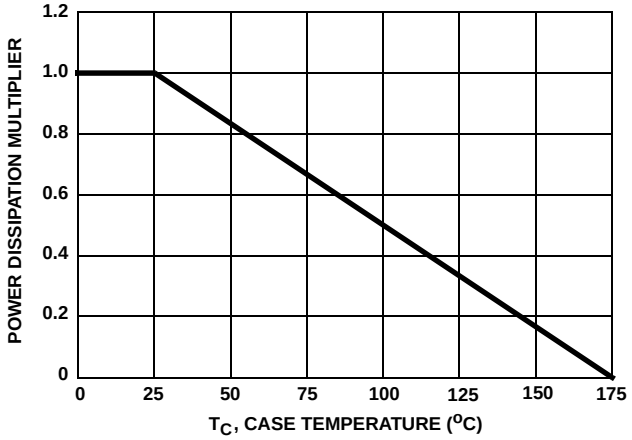



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

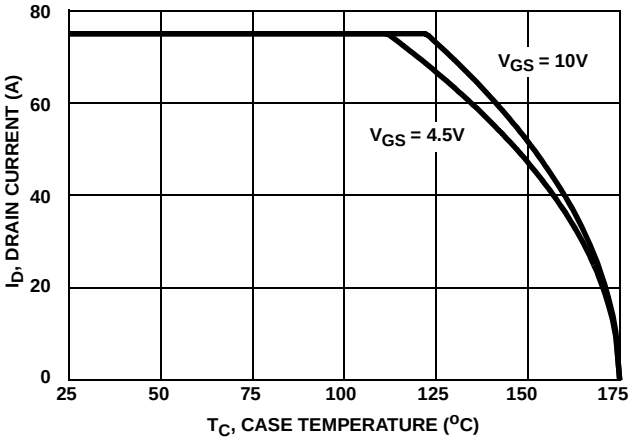



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

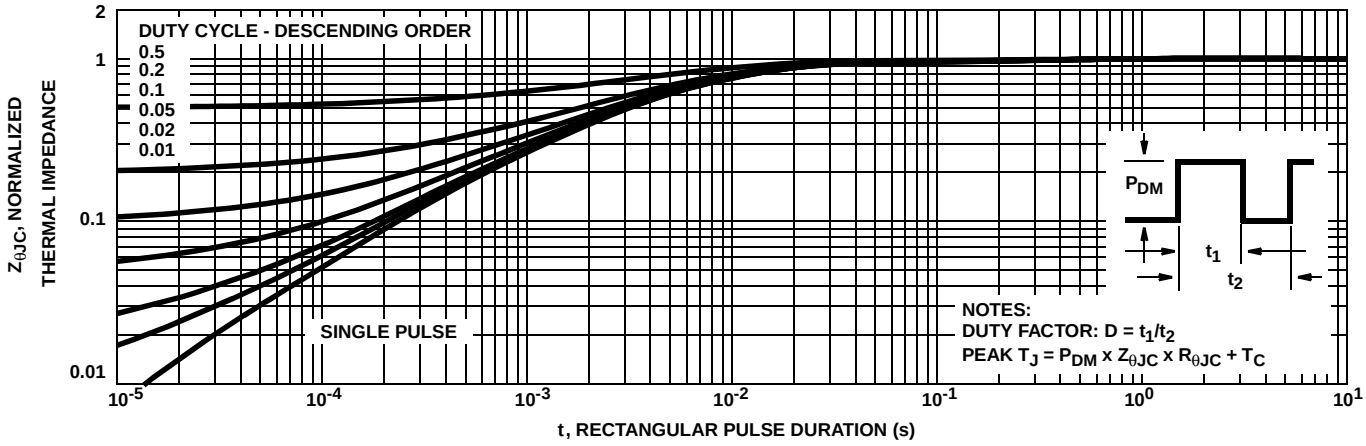



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

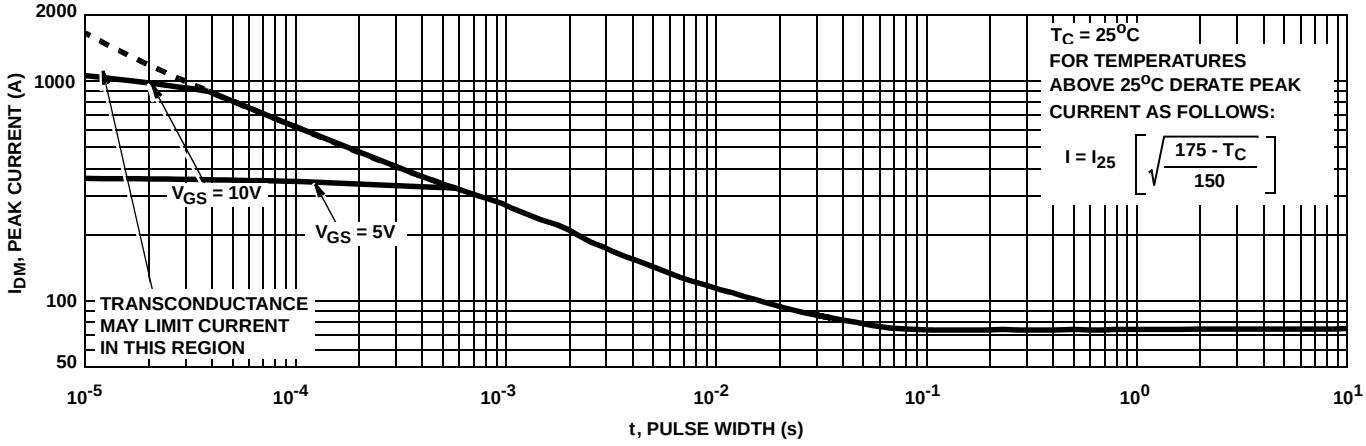



FIGURE 4. PEAK CURRENT CAPABILITY

©2002 Fairchild Semiconductor Corporation

## Typical Performance Curves (Continued)

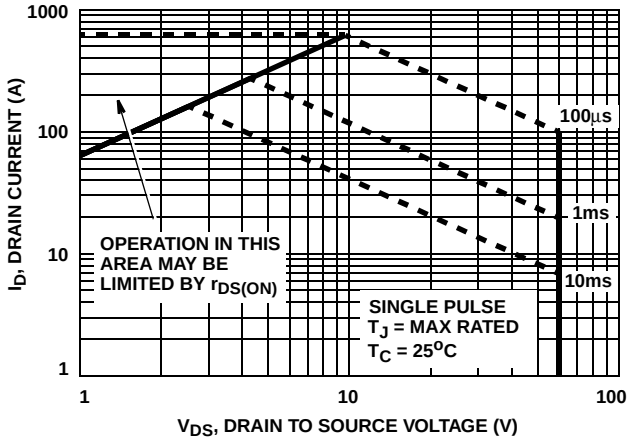
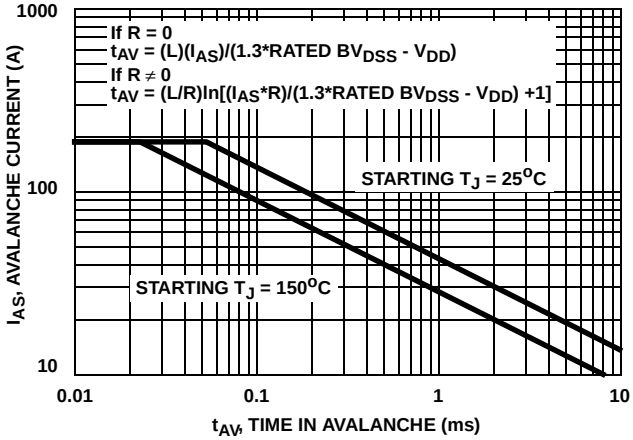



FIGURE 5. FORWARD BIAS SAFE OPERATING AREA




NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

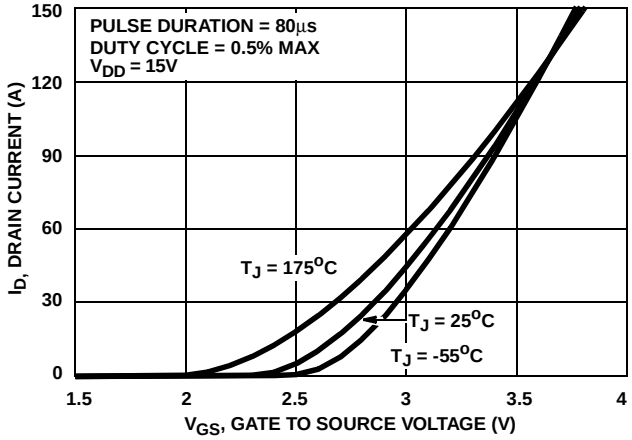



FIGURE 7. TRANSFER CHARACTERISTICS

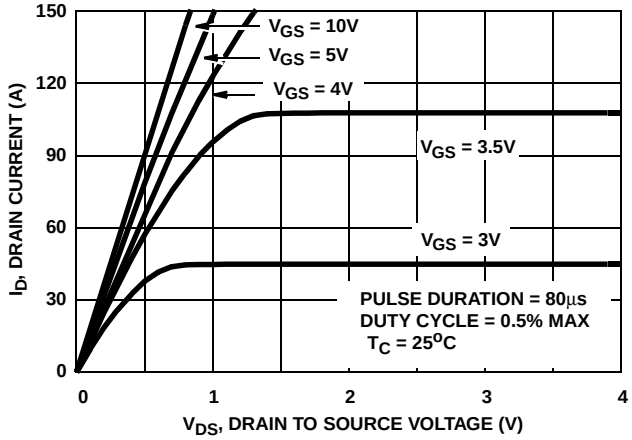



FIGURE 8. SATURATION CHARACTERISTICS

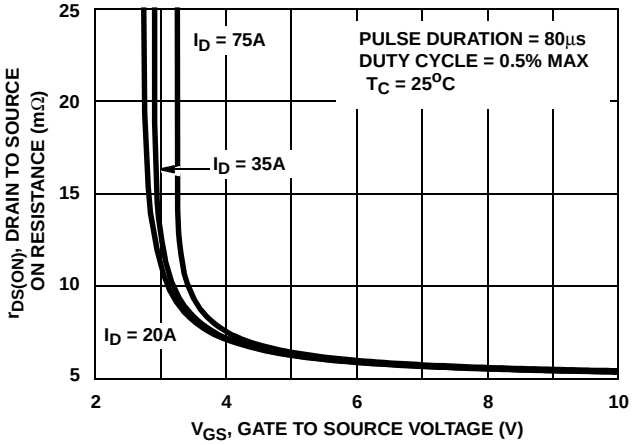



FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

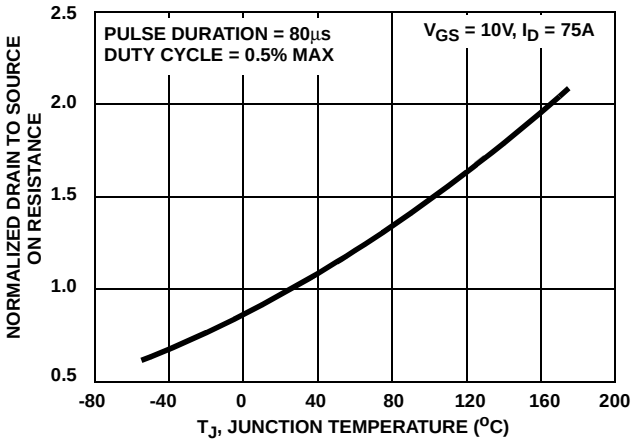



FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

©2002 Fairchild Semiconductor Corporation

## Typical Performance Curves (Continued)

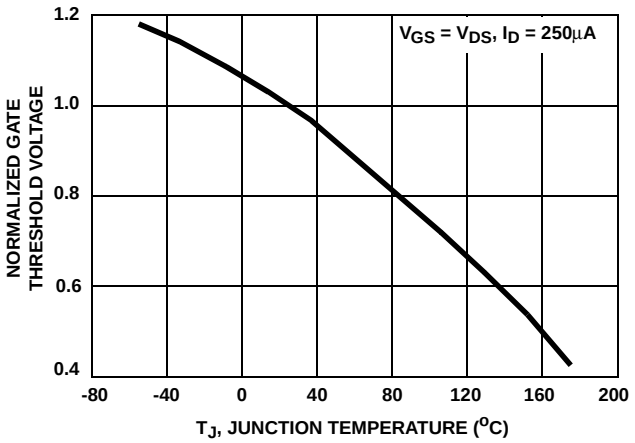



FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

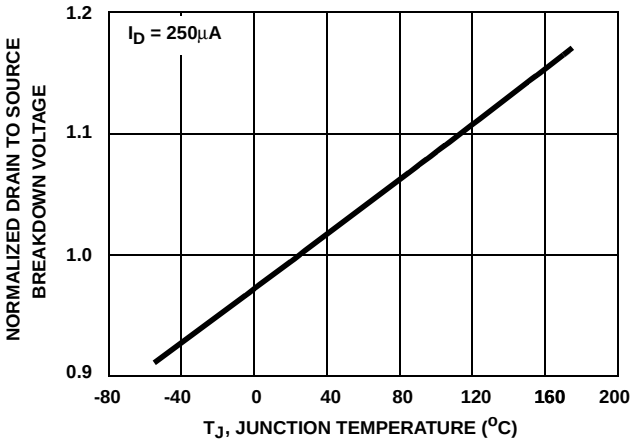



FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

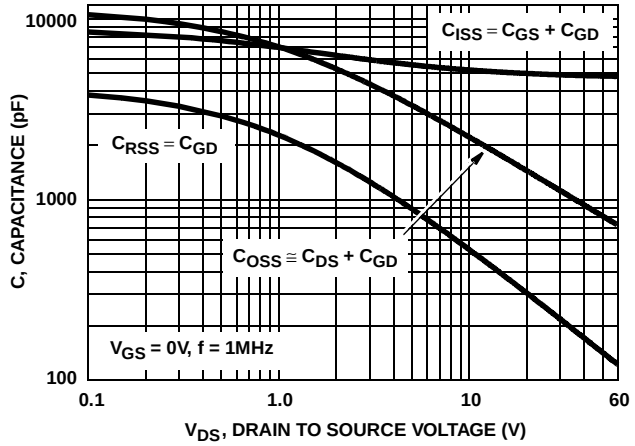
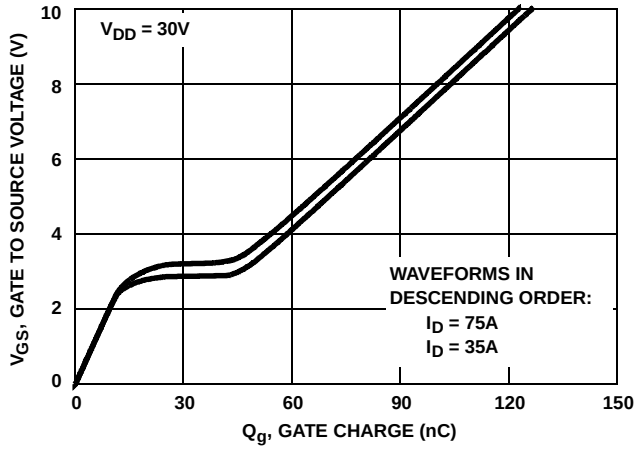



FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

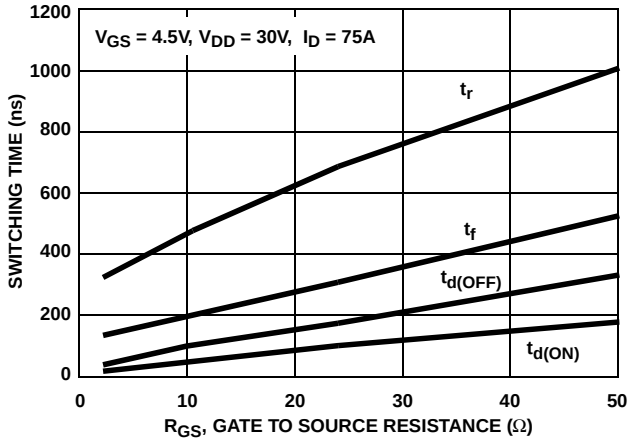



FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

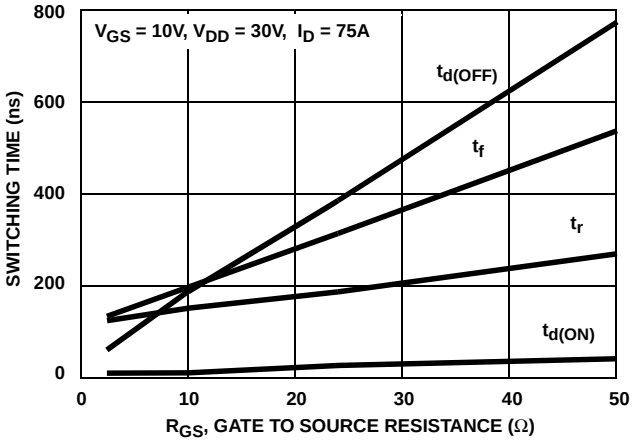



FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

©2002 Fairchild Semiconductor Corporation

## Test Circuits and Waveforms

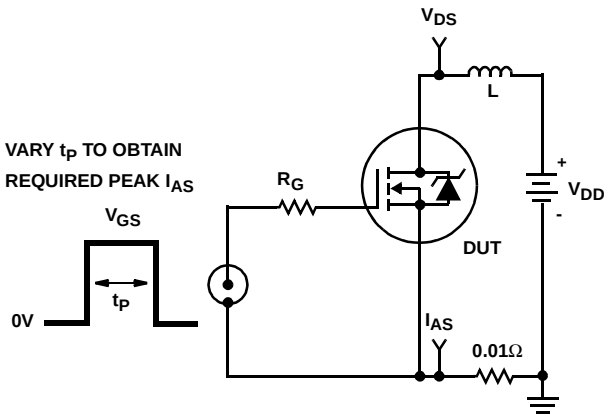



FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

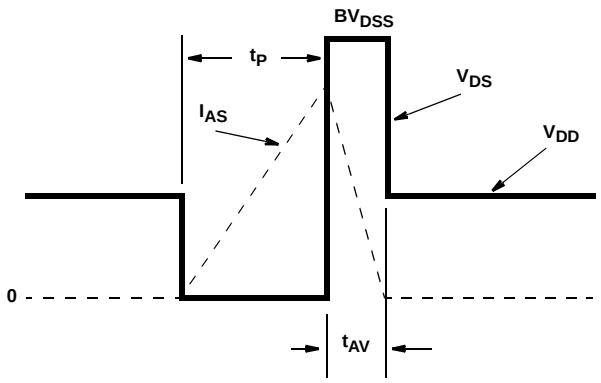



FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

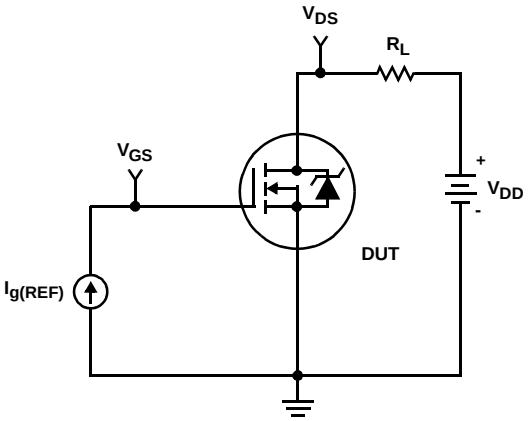



FIGURE 19. GATE CHARGE TEST CIRCUIT

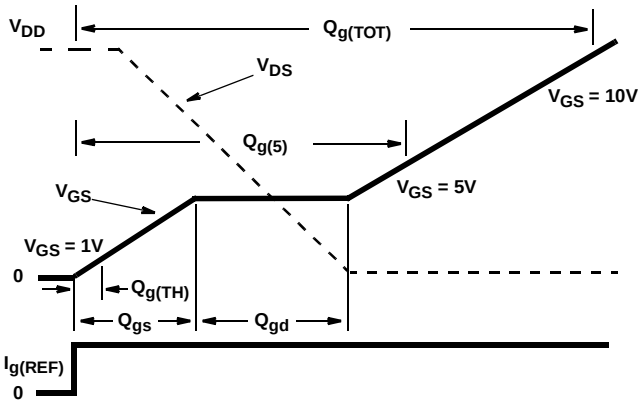



FIGURE 20. GATE CHARGE WAVEFORMS

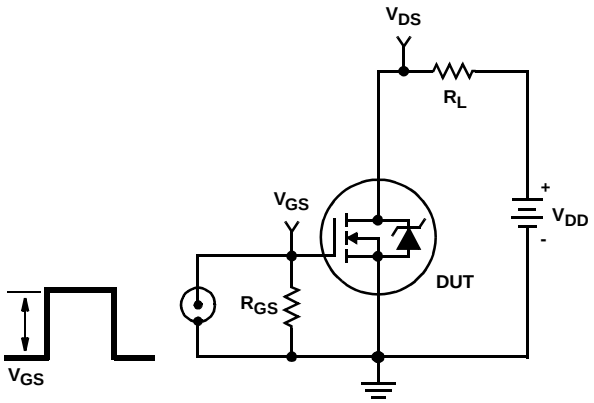



FIGURE 21. SWITCHING TIME TEST CIRCUIT

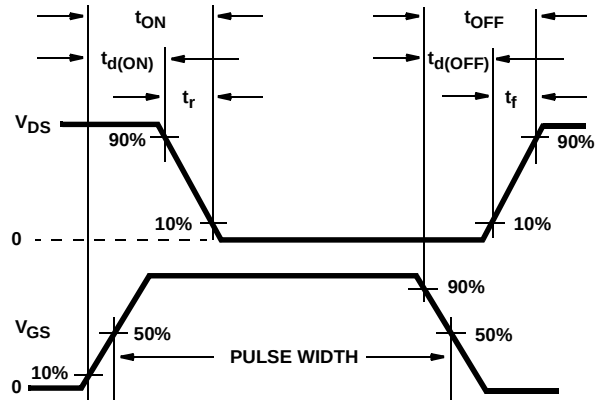



FIGURE 22. SWITCHING TIME WAVEFORM

©2002 Fairchild Semiconductor Corporation

## *PSPICE Electrical Model*

.SUBCKT HUFA76445 2 1 3 ;  rev 23 April1999

CA 12 8 6.50e-9
CB 15 14 6.50e-9
CIN 6 8 4.71e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.30
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

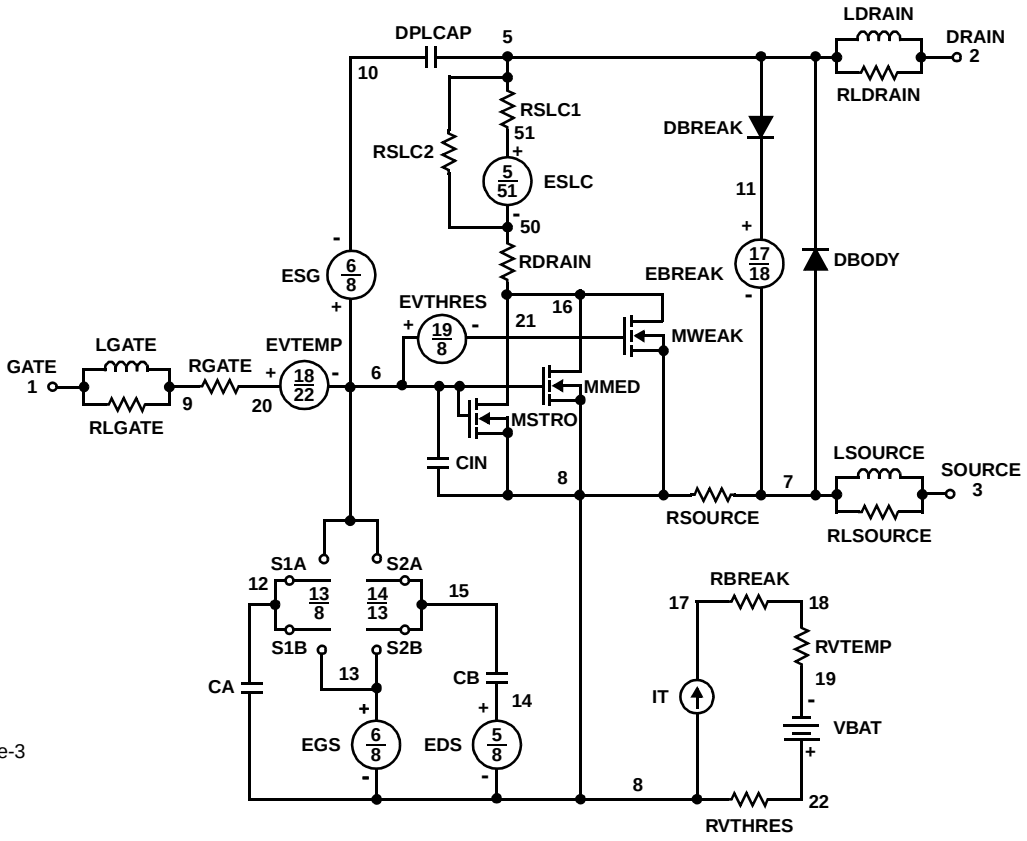
LDRAIN 2 5 1e-9
LGATE 1 9 5.05e-9
LSOURCE 3 7 2.64e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1.90e-3
RGATE 9 20 0.87
RLDRAIN 2 5 10
RLGATE 1 9 50.5
RLSOURCE 3 7 26.4
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.0e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1




ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*453),3))}

.MODEL DBODYMOD D (IS = 4.45e-12 RS = 2.08e-3 TRS1 = 1.75e-3 TRS2 = 1.03e-6 CJO = 7.22e-9 TT = 7.21e-8 M = 0.60)
.MODEL DBREAKMOD D (RS = 1.23e- 1TRS1 = 0TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 4.13e- 9IS = 1e-3 0Vj = 1.0 M = 0.85)
.MODEL MMEDMOD NMOS (VTO = 1.90 KP = 5.0 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.87)
.MODEL MSTROMOD NMOS (VTO = 2.31 KP = 275 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.65 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.7 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.16e- 3TC2 = 1.17e-7)
.MODEL RDRAINMOD RES (TC1 = 1.48e-2 TC2 = 2.93e-5)
.MODEL RSLCMOD RES (TC1 = 1.53e-3 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.87e-3 TC2 = -1.02e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.42e- 3TC2 = 9.21e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.7 VOFF= -2.7)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.7 VOFF= -5.7)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -1.0)

.ENDS

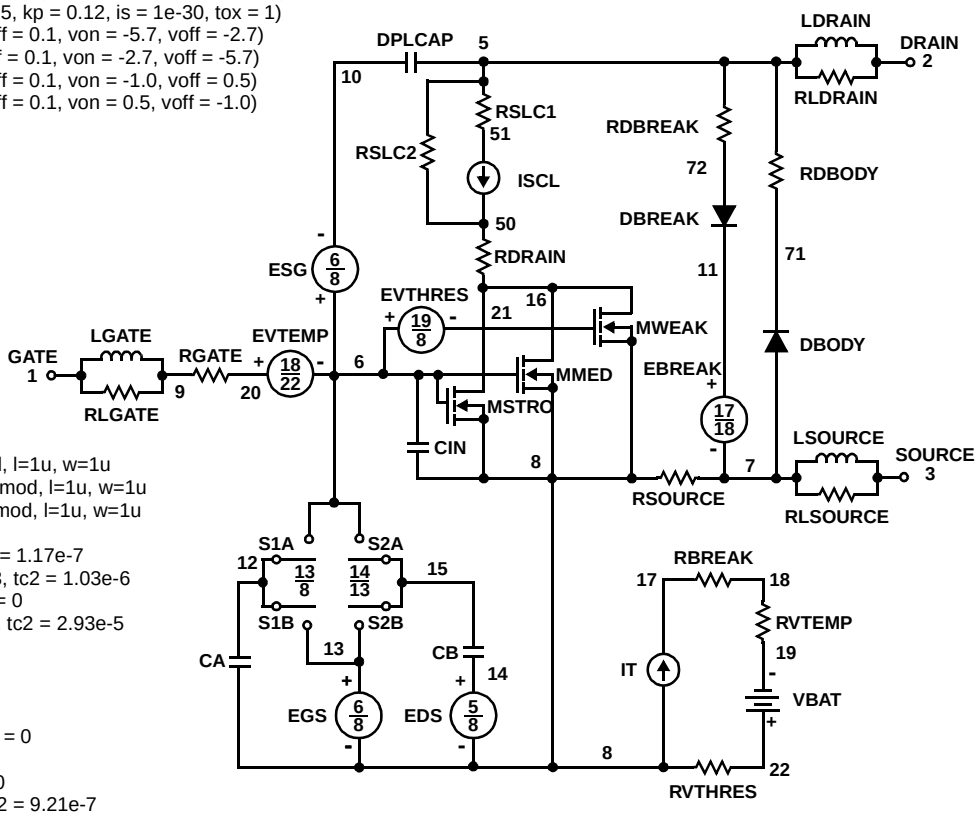
NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

©2002 Fairchild Semiconductor Corporation

## SABER Electrical Model

REV 23 April 1999

```
template ta76445 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 4.45e-12, cjo = 7.22e-9, tt = 7.21e-8, xti = 4.5, m = 0.60)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 4.13e-9, is = 1e-30, vj=1.0, m = 0.85 )
m..model mmedmod = (type=_n, vto = 1.90, kp = 5, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.31, kp = 275, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.65, kp = 0.12, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -5.7, voff = -2.7)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -2.7, voff = -5.7)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.0)

c.ca n12 n8 = 6.50e-9
c.cb n15 n14 = 6.50e-9
c.cin n6 n8 = 4.71e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 5.05e-9
l.lsource n3 n7 = 2.64e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.16e-3, tc2 = 1.17e-7
res.rdbody n71 n5 = 2.08e-3, tc1 = 1.75e-3, tc2 = 1.03e-6
res.rdbreak n72 n5 = 1.23e-1, tc1 = 0, tc2 = 0
res.rdrain n50 n16  = 1.9e-3, tc1 = 1.48e-2, tc2 = 2.93e-5
res.rgate n9 n20 = 0.87
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 50.5
res.rlsource n3 n7 = 26.4
res.rslc1 n5 n51  = 1e-6, tc1 = 1.53e-3, tc2 = 0
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 3.0e-3, tc1 = 0, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -1.42e-3, tc2 = 9.21e-7
res.rvthres n22 n8  = 1, tc1 = -2.87e-3, tc2 = -1.02e-5

spe.ebreak n11 n7 n17 n18 = 66.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/453))** 3))
}
}
```




©2002 Fairchild Semiconductor Corporation

## *SPICE Thermal Model*

REV 8 April 1999

HUFA76445T

CTHERM1 th 6 6.45e-3
CTHERM2 6 5 3.00e-2
CTHERM3 5 4 1.40e-2
CTHERM4 4 3 1.65e-2
CTHERM5 3 2 4.85e-2
CTHERM6 2 tl 12.55

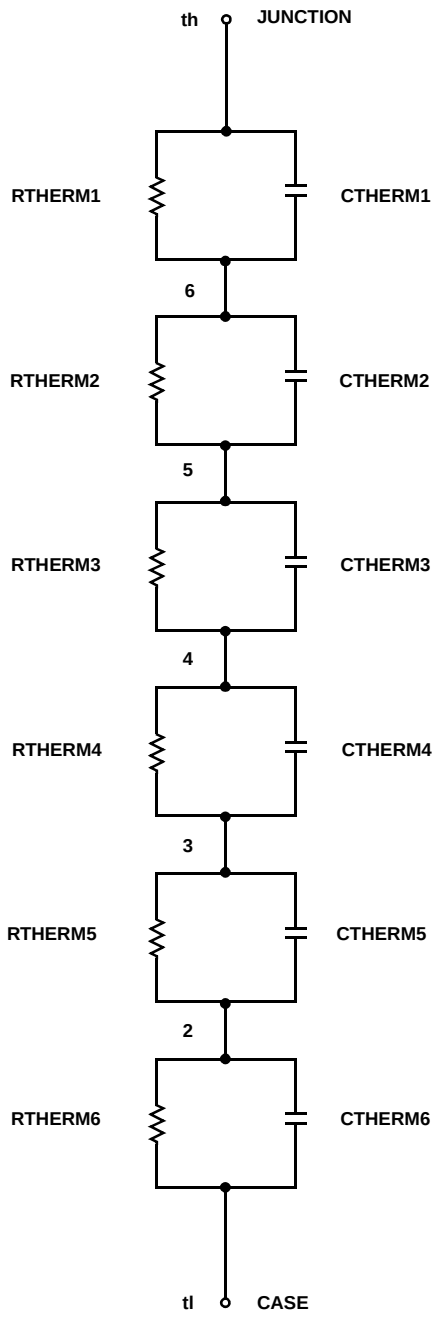
RTHERM1 th 6 3.24e-3
RTHERM2 6 5 8.08e-3
RTHERM3 5 4 2.28e-2
RTHERM4 4 3 1.28e-1
RTHERM5 3 2 1.93e-1
RTHERM6 2 tl 2.56e-2

## *SABER Thermal Model*

SABER thermal model HUFA76445T

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 6.45e-3
ctherm.ctherm2 6 5 = 3.00e-2
ctherm.ctherm3 5 4 = 1.40e-2
ctherm.ctherm4 4 3 = 1.65e-2
ctherm.ctherm5 3 2 = 4.85e-2
ctherm.ctherm6 2 tl = 12.55

rtherm.rtherm1 th 6 = 3.24e-3
rtherm.rtherm2 6 5 = 8.08e-3
rtherm.rtherm3 5 4 = 2.28e-2
rtherm.rtherm4 4 3 = 1.28e-1
rtherm.rtherm5 3 2 = 1.93e-1
rtherm.rtherm6 2 tl = 2.56e-2
}




©2002 Fairchild Semiconductor Corporation

**TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

| | | | | |
|---|---|---|---|---|
| ACEx™ | FAST ® | OPTOLOGIC™ | SMART START™ | VCX™ |
| Bottomless™ | FASTr™ | OPTOPLANAR™ | STAR*POWER™ | |
| CoolFET™ | FRFET™ | PACMAN™ | Stealth™ | |
| *CROSSVOLT*™ | GlobalOptoisolator™ | POP™ | SuperSOT™-3 | |
| DenseTrench™ | GTO™ | Power247™ | SuperSOT™-6 | |
| DOME™ | HiSeC™ | PowerTrench® | SuperSOT™-8 | |
| EcoSPARK™ | ISOPLANAR™ | QFET™ | SyncFET™ | |
| $E^2$CMOS™ | LittleFET™ | QS™ | TinyLogic™ | |
| EnSigna™ | MicroFET™ | QT Optoelectronics™ | TruTranslation™ | |
| FACT™ | MicroPak™ | Quiet Series™ | UHC™ | |
| FACT Quiet Series™ | MICROWIRE™ | SILENT SWITCHER® | UltraFET® | |

STAR*POWER is used under license

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |