GTL2002

2-bit bidirectional low voltage translator

Rev. 8 — 19 August 2013 Product data sheet

1. General description

The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2002 provides 2 NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

When the Sn or Dn port is LOW the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to V_{CC} by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other two matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

2. Features and benefits

- 2-bit bidirectional low voltage translator
- Allows voltage level translation between 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V buses, which allows direct interface with GTL, GTL+, LVTTL/TTL and 5 V CMOS levels
- Provides bidirectional voltage translation with no direction pin
- Low 6.5 Ω ON-state resistance (R_{on}) between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required; will not latch up
- 5 V tolerant inputs
- Low standby current
- Flow-through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Packages offered: SO8, TSSOP8 (MSOP8), VSSOP8, XQFN8

3. Applications

- Any application that requires bidirectional or unidirectional voltage level translation from any voltage between 1.0 V and 5.0 V to any voltage between 1.0 V and 5.0 V
- The open-drain construction with no direction pin is ideal for bidirectional low voltage (e.g., 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I^2C-bus port translation to the normal 3.3 V or 5.0 V I^2C-bus signal levels or GTL/GTL+ translation to LVTTL/TTL signal levels.

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
GTL2002D	GTL2002	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
GTL2002DP	2002	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
GTL2002DC	2002	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
GTL2002GM	G2X[2]	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

[1] Also known as MSOP8.

[2] 'X' will change based on date code.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
GTL2002D	GTL2002D,112	SO8	Standard marking * IC's tube - DSC bulk pack	2000	T_{amb} = –40 °C to +85 °C
GTL2002D	GTL2002D,118	SO8	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
GTL2002DP	GTL2002DP,118	TSSOP8	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
GTL2002DC	GTL2002DC,125	VSSOP8	Reel 7" Q3/T4 *Standard mark	3000	T_{amb} = –40 °C to +85 °C
GTL2002GM	GTL2002GM,125	XQFN8	Reel 7" Q3/T4 *Standard mark	4000	T_{amb} = –40 °C to +85 °C

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5. Functional diagram

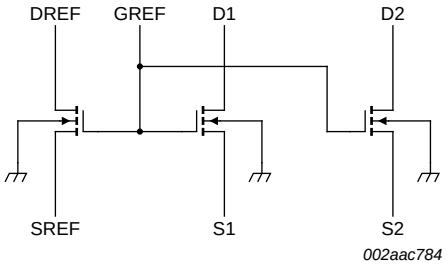

Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

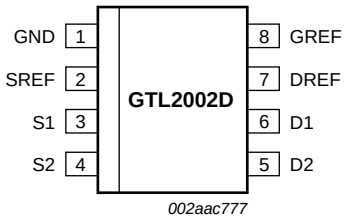

Fig 2. Pin configuration for SO8

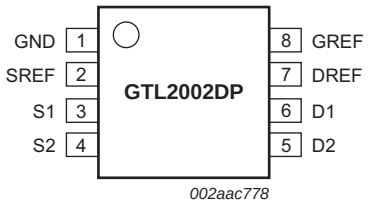

Fig 3. Pin configuration for TSSOP8 (MSOP8)

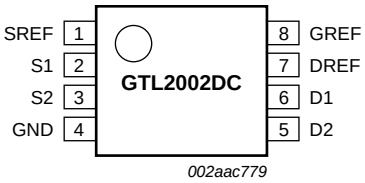

Fig 4. Pin configuration for VSSOP8

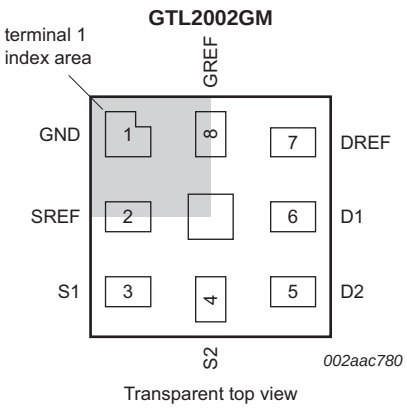

Fig 5. Pin configuration for XQFN8

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6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO8, TSSOP8, XQFN8U	VSSOP8	
GND	1	4	ground (0 V)
SREF	2	1	source of reference transistor
S1	3	2	port S1
S2	4	3	port S2
D2	5	5	port D2
D1	6	6	port D1
DREF	7	7	drain of reference transistor
GREF	8	8	gate of reference transistor

7. Functional description

Refer to Figure 1 “Functional diagram”.

7.1 Function selection

Table 4. Function selection, HIGH to LOW translation

Assuming Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don’t care.

GREF[1]	DREF	SREF	Input Dn	Output Sn	Transistor
H	H	0 V	X	X	off
H	H	V_{TT}[4]	H	V_{TT}[2][4]	on
H	H	V_{TT}[4]	L	L[3]	on
L	L	0 V – V_{TT}[4]	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2] Sn is not pulled up or pulled down.

[3] Sn follows the Dn input LOW.

[4] V_{TT} is equal to the SREF voltage.

Table 5. Function selection, LOW to HIGH translation

Assuming Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don’t care.

GREF[1]	DREF	SREF	Input Sn	Output Dn	Transistor
H	H	0 V	X	X	off
H	H	V_{TT}[4]	V_{TT}[4]	H[2]	nearly off
H	H	V_{TT}[4]	L	L[3]	on
L	L	0 V – V_{TT}[4]	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2] Dn is pulled up to V_{CC} through an external resistor.

[3] Dn follows the Sn input LOW.

[4] V_{TT} is equal to the SREF voltage.

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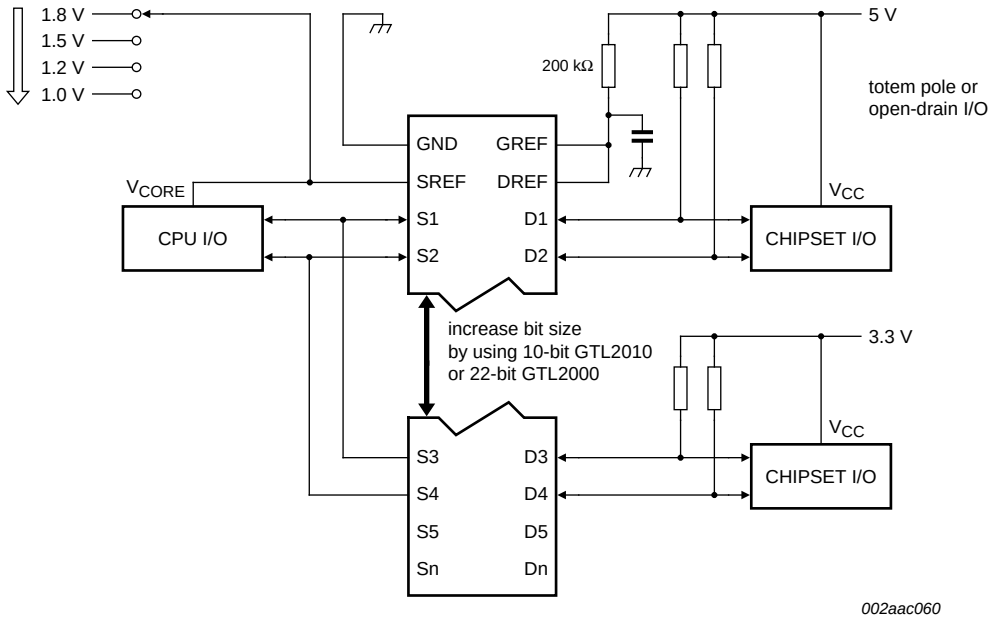
8. Application design-in information

8.1 Bidirectional translation

For the bidirectional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the GREF input must be connected to DREF and both pins pulled to HIGH side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. The processor output can be totem pole or open-drain (pull-up resistors may be required) and the chip set output can be totem pole or open-drain (pull-up resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed. The opposite side of the reference transistor (SREF) is connected to the processor core power supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and SREF is set between 1.0 V to (V_{CC} − 1.5 V), the output of each Sn has a maximum output voltage equal to SREF and the output of each Dn has a maximum output voltage equal to V_{CC}.



Typical bidirectional voltage translation.

Fig 6. Bidirectional translation to multiple higher voltage levels such as an I²C-bus application

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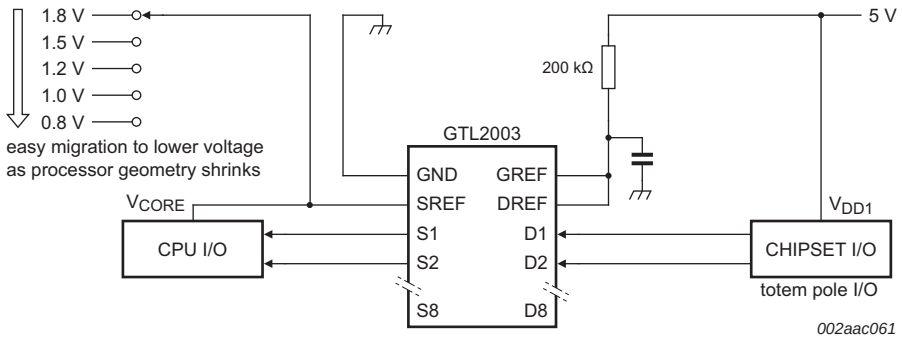
8.2 Unidirectional down translation

For unidirectional clamping, higher voltage to lower voltage, the GREF input must be connected to DREF and both pins pulled to the higher side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. Pull-up resistors are required if the chip set I/O are open-drain. The opposite side of the reference transistor (SREF) is connected to the processor core supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and SREF is set between 1.0 V to (V_{CC} − 1.5 V), the output of each Sn has a maximum output voltage equal to SREF.

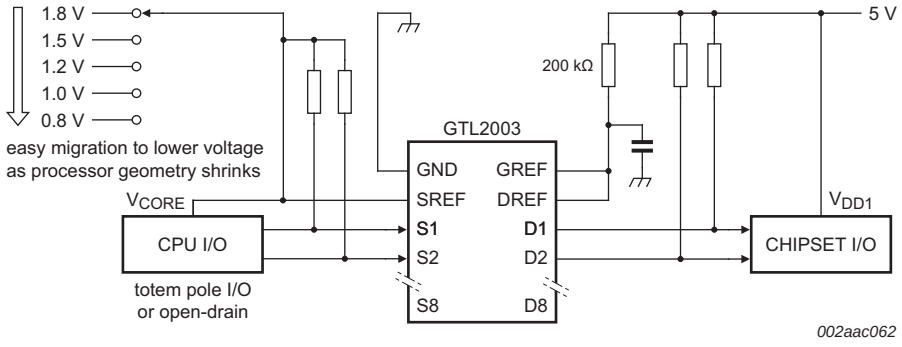


Typical unidirectional HIGH-to-LOW voltage translation.

Fig 7. Unidirectional down translation to protect low voltage processor pins

8.3 Unidirectional up translation

For unidirectional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side (Dn or Sn) to get the full HIGH level, since the GTL-TVC device will only pass the reference source (SREF) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open-drain.



Typical unidirectional LOW-to-HIGH voltage translation.

Fig 8. Unidirectional up translation to higher voltage chip sets

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8.4 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This will guarantee a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as shown in Equation 1:

$$resistor\ value\ (\Omega) = \frac{pull\text{-}up\ voltage\ (V) - 0.35\ V}{0.015\ A} \quad (1)$$

Table 6 summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA. The resistor value shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device. See application note *AN10145, "Bidirectional low voltage translators"* for more information.

Table 6. Pull-up resistor values

Pull-up resistor value (Ω)[1]						
Voltage	**15 mA[2]**		**10 mA[2]**		**3 mA[2]**	
	Nominal	**+ 10 %[3]**	**Nominal**	**+ 10 %[3]**	**Nominal**	**+ 10 %[3]**
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

[1] Calculated for V_{OL} = 0.35 V.

[2] Assumes output driver V_{OL} = 0.175 V at stated current.

[3] + 10 % to compensate for V_{DD} range and resistor tolerance.

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9. Limiting values

Table 7. Limiting values[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{SREF}	voltage on pin SREF		[2]	−0.5	+7.0	V
V_{DREF}	voltage on pin DREF		[2]	−0.5	+7.0	V
V_{GREF}	voltage on pin GREF		[2]	−0.5	+7.0	V
V_{Sn}	voltage on port Sn		[2]	−0.5	+7.0	V
V_{Dn}	voltage on port Dn		[2]	−0.5	+7.0	V
I_{REFK}	diode current on reference pins	$V_I < 0$ V		-	−50	mA
I_{SK}	diode current port Sn	$V_I < 0$ V		-	−50	mA
I_{DK}	diode current port Dn	$V_I < 0$ V		-	−50	mA
I_{max}	clamp current per channel	channel in ON state		-	±128	mA
T_{stg}	storage temperature			−65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperature which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

10. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{I/O}$	voltage on an input/output pin	Sn, Dn		0	5.5	V
V_{SREF}	voltage on pin SREF		[1]	0	5.5	V
V_{DREF}	voltage on pin DREF			0	5.5	V
V_{GREF}	voltage on pin GREF			0	5.5	V
I_{PASS}	pass transistor current			-	64	mA
T_{amb}	ambient temperature	operating in free air		−40	+85	°C

[1] $V_{SREF} \leq V_{DREF} - 1.5$ V for best results in level shifting applications.

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11. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	V_{DD} = 3.0 V; V_{SREF} = 1.365 V; V_{Sn} or V_{Dn} = 0.175 V; I_{clamp} = 15.2 mA		-	260	350	mV
V_{IK}	input clamping voltage	I_I = −18 mA; V_{GREF} = 0 V		-	-	−1.2	V
$I_{LI(gate)}$	gate input leakage current	V_I = 5 V; V_{GREF} = 0 V		-	-	5	μA
C_{ig}	input capacitance at gate	pin GREF; V_I = 3 V or 0 V		-	19.4	-	pF
$C_{io(off)}$	off-state input/output capacitance	V_O = 3 V or 0 V; V_{GREF} = 0 V	[2]	-	7.4	-	pF
$C_{io(on)}$	on-state input/output capacitance	V_O = 3 V or 0 V; V_{GREF} = 3 V	[2]	-	18.6	-	pF
R_{on}	ON-state resistance	V_I = 0 V; I_O = 64 mA	[3]				
		V_{GREF} = 4.5 V		-	3.5	5	Ω
		V_{GREF} = 3 V		-	4.4	7	Ω
		V_{GREF} = 2.3 V		-	5.5	9	Ω
		V_{GREF} = 1.5 V		-	67	105	Ω
		V_I = 0 V; I_O = 30 mA; V_{GREF} = 1.5 V	[3]	-	9	15	Ω
		V_I = 2.4 V; I_O = 15 mA; V_{GREF} = 4.5 V	[3]	-	7	10	Ω
		V_I = 2.4 V; I_O = 15 mA; V_{GREF} = 3 V	[3]	-	58	80	Ω
		V_I = 1.7 V; I_O = 15 mA; V_{GREF} = 2.3 V	[3]	-	50	70	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

[2] $C_{io(on)}$ maximum of 30 pF and $C_{io(off)}$ maximum of 15 pF is guaranteed by design.

[3] Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

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12. Dynamic characteristics

12.1 Dynamic characteristics for translator-type application

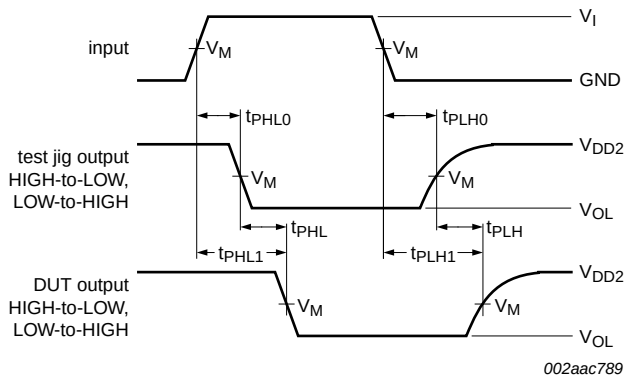
Table 10. Dynamic characteristics for translator-type application

T_{amb} = −40 °C to +85 °C; V_{ref} = 1.365 V to 1.635 V; V_{DD1} = 3.0 V to 3.6 V; V_{DD2} = 2.36 V to 2.64 V; GND = 0 V; $t_r = t_f \leq 3.0$ ns. Refer to Figure 11.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	Sn to Dn; Dn to Sn	[2]	0.5	1.5	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	Sn to Dn; Dn to Sn	[2]	0.5	1.5	5.5	ns

[1] All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V; V_{ref} = 1.5 V and T_{amb} = 25 °C.

[2] Propagation delay guaranteed by characterization.



V_M = 1.5 V; V_I = GND to 3.0 V.

Fig 9. The input (Sn) to output (Dn) propagation delays

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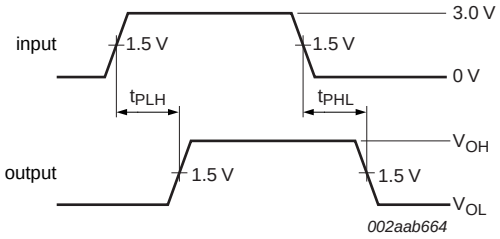
12.2 Dynamic characteristics for CBT-type application

Table 11. Dynamic characteristics for CBT-type application

T_{amb} = −40 °C to +85 °C; V_{GREF} = 5 V ± 0.5 V; GND = 0 V; $t_r = t_f \leq 3.0$ ns; C_L = 50 pF.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay		[1]	-	-	250	ps

[1] This parameter is warranted by the ON-state resistance at GREF = 4.5 V, but is not directly production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



t_{PD} = the maximum of t_{PLH} or t_{PHL}.

V_M = 1.5 V; V_I = GND to 3.0 V.

Fig 10. Input (Sn) to output (Dn) propagation delays

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13. Test information

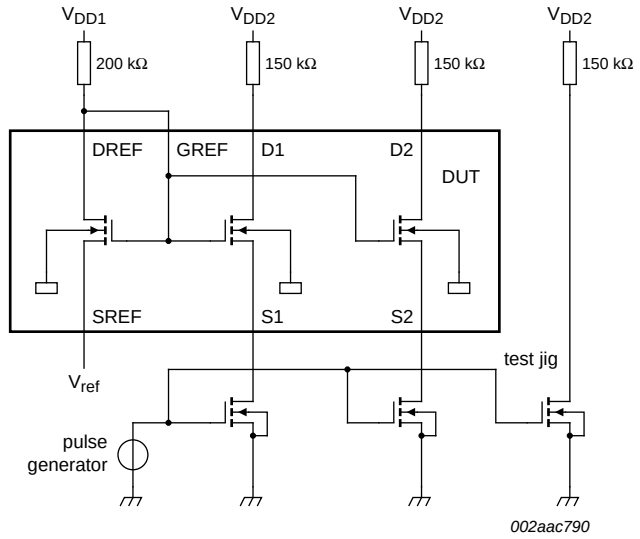
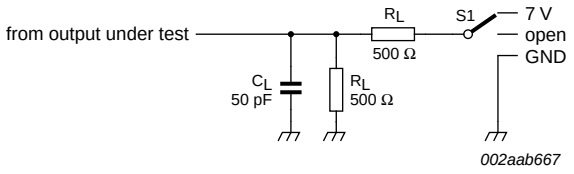


Fig 11. Load circuit for translator-type applications



Test data are given in Table 12.

C_L = load capacitance; includes jig and probe capacitance.

R_L = load resistance.

Fig 12. Load circuit for CBT-type application

Table 12. Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open

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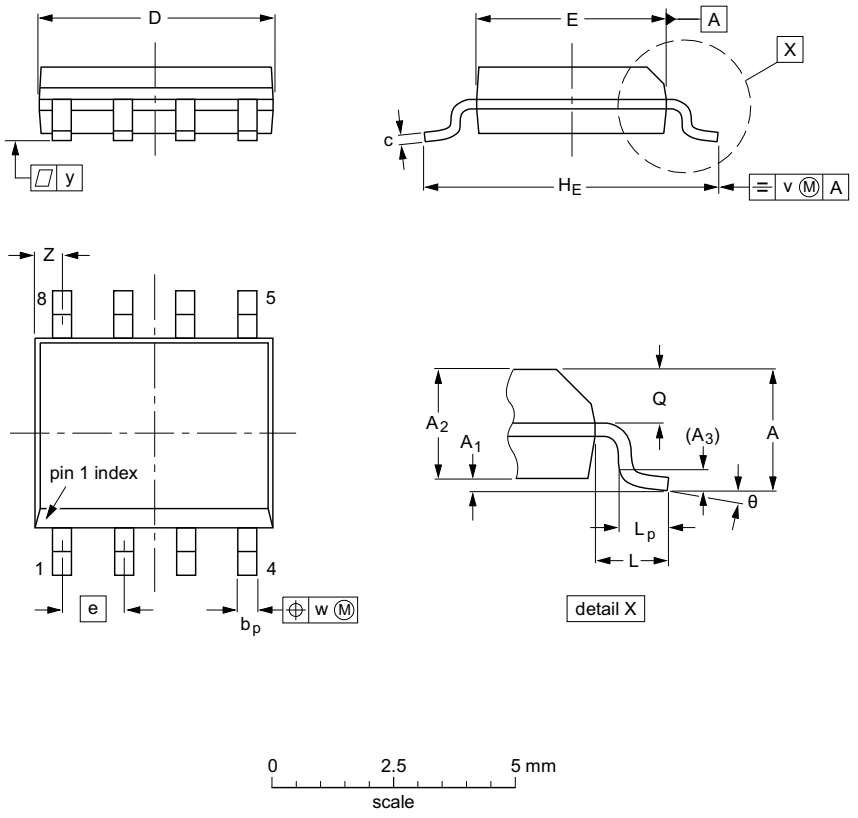
14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT96-1 (SO8)

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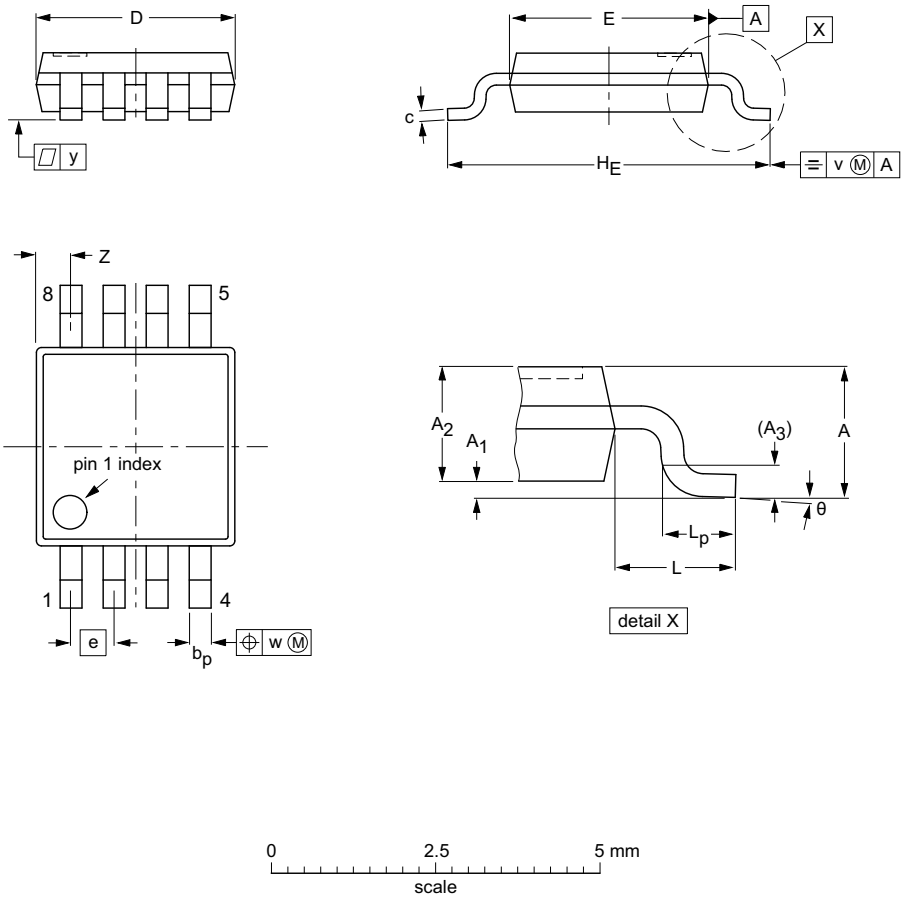
TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 14. Package outline SOT505-1 (TSSOP8)

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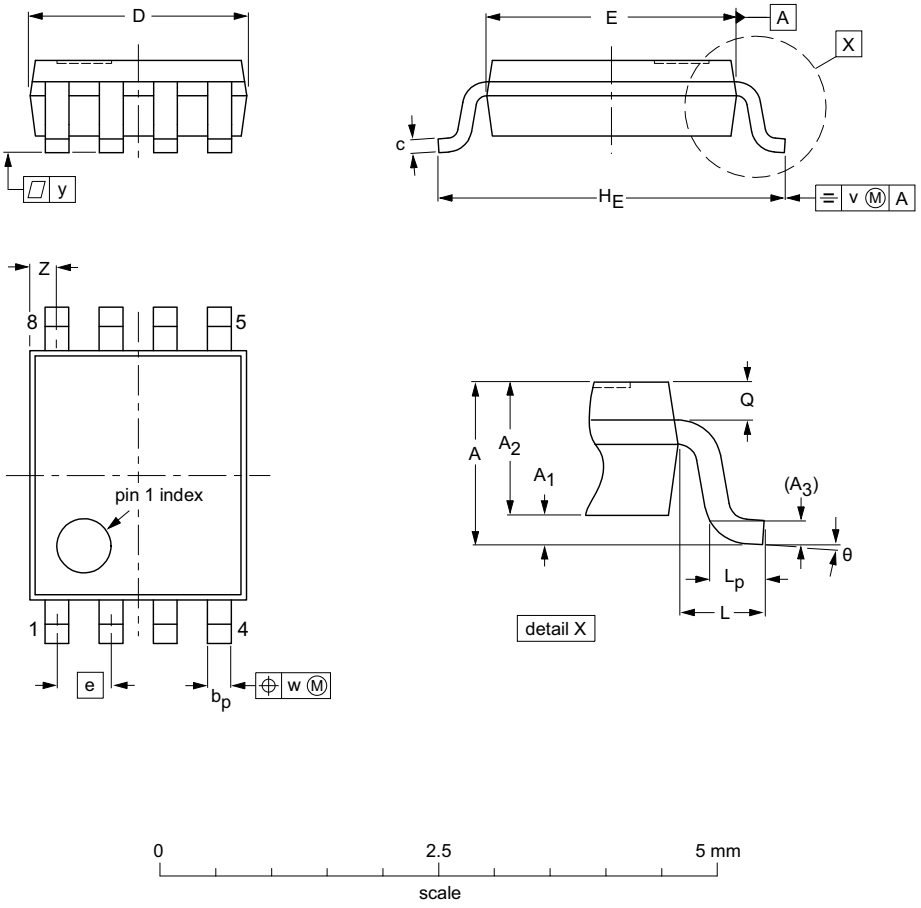
VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 15. Package outline SOT765-1 (VSSOP8)

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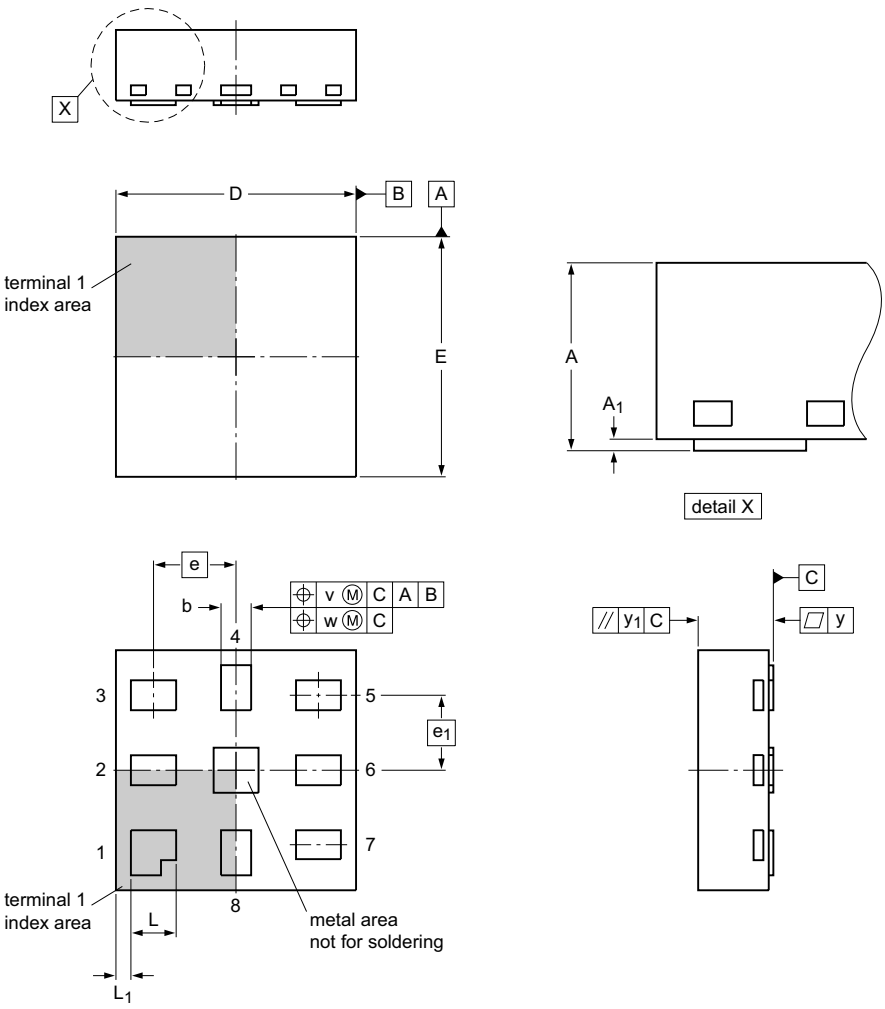
XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65	0.55	0.5	0.35	0.15	0.1	0.05	0.05	0.05
	nom			0.20	1.60	1.60			0.30	0.10				
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 16. Package outline SOT902-2 (XQFN8)

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15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.

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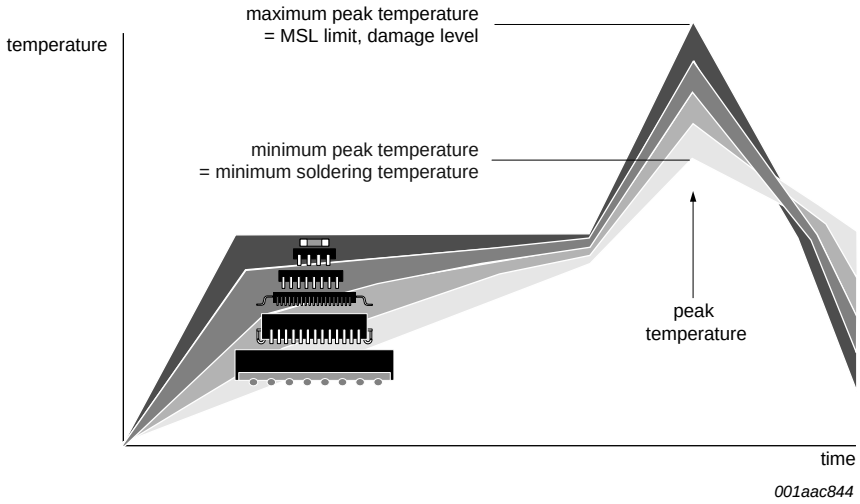

MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Soldering: PCB footprints

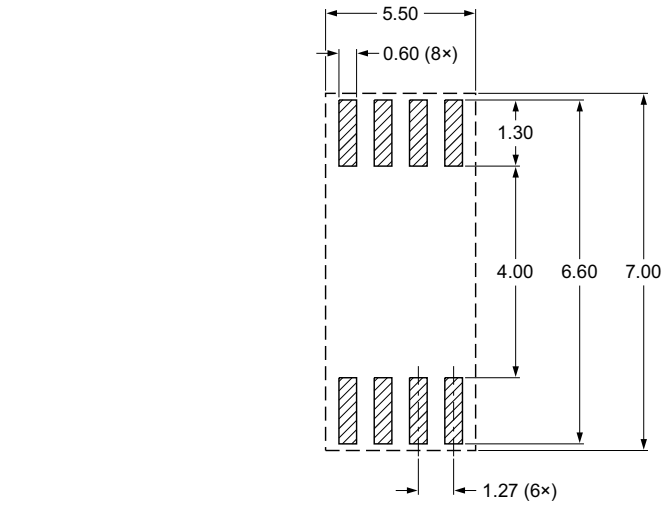

Fig 18. PCB footprint for SOT96-1 (SO8); reflow soldering

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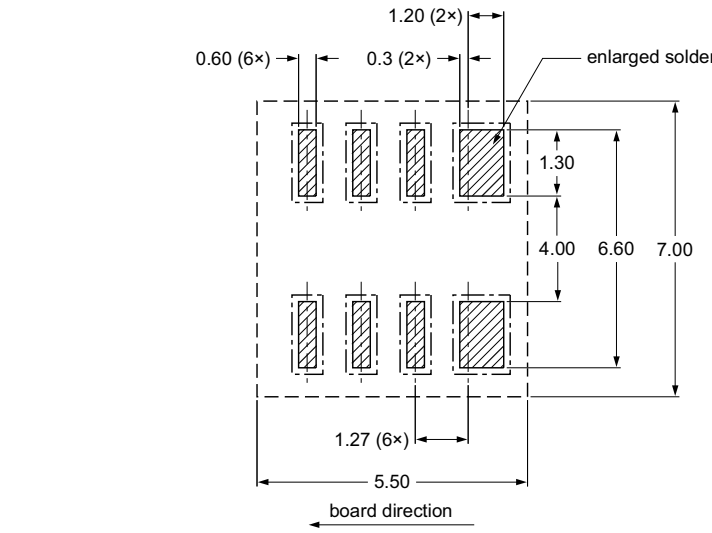

Fig 19. PCB footprint for SOT96-1 (SO8); wave soldering

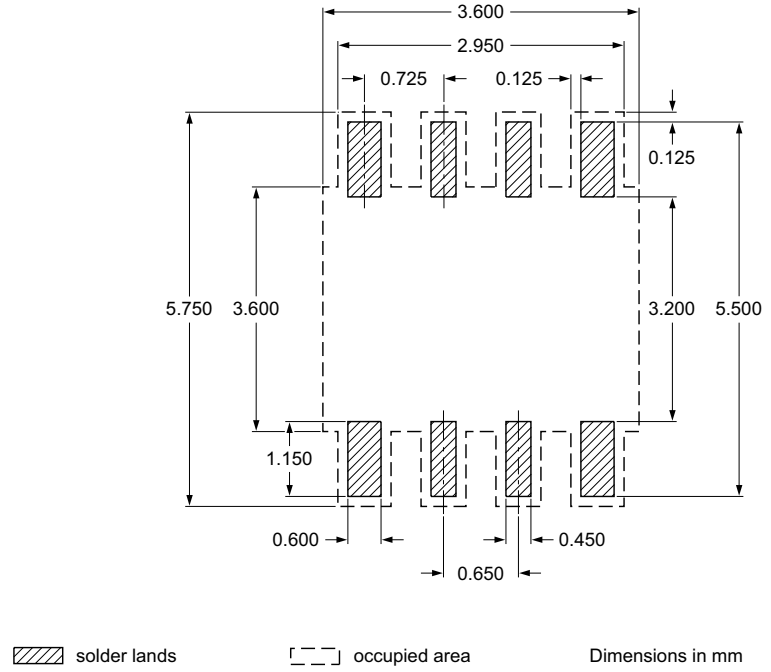

Fig 20. PCB footprint for SOT505-1 (TSSOP8); reflow soldering

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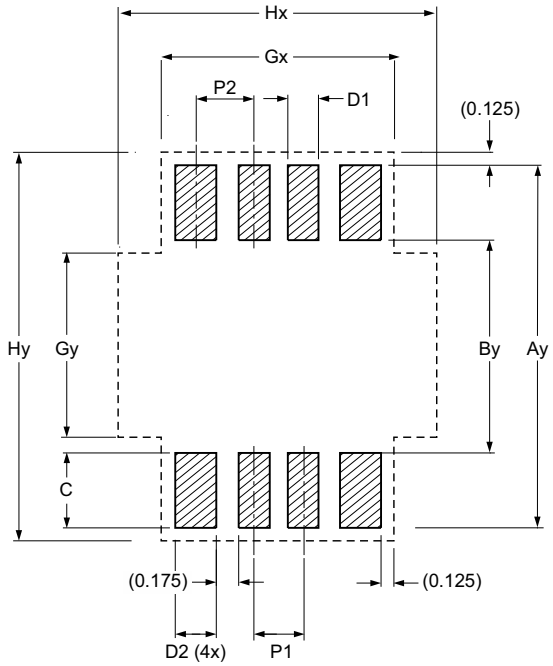
Footprint information for reflow soldering of VSSOP8 package **SOT765-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.550	3.500	2.000	0.750	0.300	0.400	2.250	1.750	3.075	3.750

sot765-1_fr

Fig 21. PCB footprint for SOT765-1 (VSSOP8); reflow soldering

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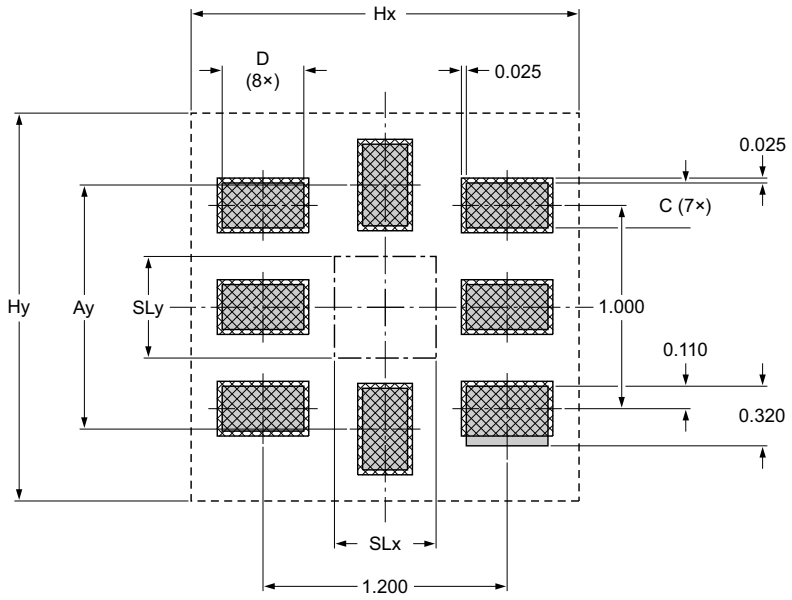
Footprint information for reflow soldering of XQFN8 package **SOT902-2**



solder land

solder paste deposit

solder land plus solder paste

occupied area

DIMENSIONS in mm

Ay	C	D	SLx	SLy	Hx	Hy
1.2	0.22	0.4	0.5	0.5	1.9	1.9

Issue date ~~12-02-23~~ 12-12-18

sot902-2_fr

Fig 22. PCB footprint for SOT902-2 (XQFN8); reflow soldering

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17. Abbreviations

Table 15. Abbreviations

Acronym	Description
CBT	Cross Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I/O	Input/Output
I^2C-bus	Inter-Integrated Circuit bus
LVTTL	Low Voltage Transistor-Transistor Logic
NMOS	Negative-channel Metal-Oxide Semiconductor
RC	Resistor Capacitor network
TTL	Transistor-Transistor Logic
TVC	Transceiver Voltage Clamps

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18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2002 v.8	20130819	Product data sheet	-	GTL2002 v.7
Modifications:	• Section 2 “Features and benefits”: – 10th bullet item: deleted phrase “150 V MM per JESD22-A115” – 11th bullet item changed from “XQFN8U” to “XQFN8” • Table 1 “Ordering information”: – removed type number “GTL2002DP/Q900” – added column “Topside marking” – GTL2002GM package name, description, and version changed per PCN #201108001F01: from “XQFN8U, plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm (SOT902-1)” to “XQFN8, plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm (SOT902-2)” • Table 2 “Ordering options”: – Added columns “Orderable part number”, “Package”, “Packing method”, and “Minimum order quantity” – Column “Topside mark” is moved to Table 1 • Figure 3 “Pin configuration for TSSOP8 (MSOP8)” updated: removed type number “GTL2002DP/Q900” • Figure 5 changed from “XQFN8U” (SOT902-1) to “XQFN8” (SOT902-2), (per PCN #201108001F01) • Table 3 “Pin description” modified: column heading changed from “XQFN8U” to “XQFN8” • Figure 16 changed from “SOT902-1 (XQFN8U)” to “SOT902-2 (XQFN8)”, per PCN #201108001F01 • Section 15 “Soldering of SMD packages” updated • Added Section 16 “Soldering: PCB footprints”			
GTL2002 v.7	20090702	Product data sheet	-	GTL2002 v.6
GTL2002 v.6	20071221	Product data sheet	-	GTL2002 v.5
GTL2002 v.5	20070813	Product data sheet	-	GTL2002 v.4
GTL2002 v.4	20060829	Product data sheet	-	GTL2002 v.3
GTL2002 v.3 (9397 750 13058)	20040929	Product data sheet	-	GTL2002 v.2
GTL2002 v.2 (9397 750 11349)	20030401	Product data	ECN 853-2214 29603 dated 2003 Feb 28	GTL2002 v.1
GTL2002 v.1 (9397 750 07417)	20000216	Product specification	ECN 853-2214 24367 dated 2000 Aug 16	-

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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