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TECHNICAL DATA

MC9S12K-Family

Product Preview

16-Bit Microcontroller

Targeted for ultra high reliability systems, members of the MC9S12K-Family of 16-bit Flash-based microcontrollers have an increased performance in reliability over the life of the product. The improvement is due to a built-in Error Checking and Correction code (ECC) in the Flash memory. The program and erase operations automatically generate six parity bits per word making ECC transparent to the end user. The ECC logic implements a modified Hamming code capable of correcting single bit faults and detecting double bit faults in each word. The MC9S12K-Family members are composed of standard on-chip peripherals and maintain pin compatibility with the MC9S12D-Family.

Features

- **16-bit CPU12**
  - — Upward compatible with M68HC11 instruction set
  - — Interrupt stacking and programmer's model identical to M68HC11
  - — Instruction queue
  - — Enhanced indexed addressing
- **System Integration Module (SIM)**
  - — Multiplexed External Bus Interface (MEBI)
    - Single chip or expanded
    - 16 address/16 data wide or 16 address/8 data narrow modes
  - — Memory Map and Interface (MMC)
  - — Interrupt Controller (INT)
  - — Development support
    - Single-wire Background Debug Mode™ (BDM)
    - Debugger with on-chip trace buffer and flexible triggers (DBG)
    - On-chip hardware Breakpoints (BKP)
- **Oscillator (OSC)**
  - — 2Mhz to 16Mhz frequency range
  - — Pierce with amplitude loop control
  - — Clock monitor
- **Clock and Reset Generator (CRG)**
  - — Phase-locked loop clock frequency multiplier
  - — Self Clock mode in absence of external clock
  - — COP watchdog
  - — Real Time interrupt (RTI)
- **Memory options**
  - — 32K, 64K, 128K, 256K Byte Flash EEPROM
    - Internal program/erase voltage generation
    - Security and Block Protect bits
    - Built-in Error Checking and Correction code (ECC)
  - — 1K, 2K, 4K Byte EEPROM
  - — 2K, 4K, 8K, 12K Byte static RAM

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- **Analog-to-Digital Converter(s) (ADC)**
  - — Two 8-channel modules with 10-bit resolution for MC9S12KT256
  - — One 16-channel module with 10-bit resolution for MC9S12KG128, MC9S12K64 and MC9S12K32
  - — External conversion trigger capability
- **8-channel Timer (TIM)**
  - — Programmable input capture or output compare channels
  - — Simple PWM mode
  - — Counter Modulo Reset
  - — External Event Counting
  - — Gated Time Accumulation
- **8-channel Pulse Width Modulator (PWM)**
  - — Programmable period and duty cycle per channel
  - — 8-bit 8-channel or 16-bit 4-channel
  - — Edge and center aligned PWM signals
  - — Emergency shutdown input
- **Up to three 1M bit per second, CAN 2.0 A, B software compatible modules**
  - — Five receive and three transmit buffers
  - — Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - — Four separate interrupt channels for Rx, Tx, error and wake-up
  - — Low-pass filter wake-up function
  - — Loop-back for self test operation
- **Serial interfaces**
  - — Up to two asynchronous serial communication interface (SCI)
  - — Up to three synchronous serial peripheral interface (SPI)
  - — Inter-IC Bus (IIC)
- **Internal 2.5V Regulator**
  - — Input voltage range from 3.15V to 5.5V
  - — Low power mode capability
  - — Low Voltage Reset (LVR) and Low Voltage Interrupt (LVI)
- **20 key wake up inputs**
  - — Rising or falling edge triggered interrupt capability
  - — Digital filter to prevent short pulses from triggering interrupts
  - — Programmable pull ups and pull downs
- **Operating frequency for ambient temperatures (T_A -40°C to 125°C)**
  - — 50MHz equivalent to 25MHz Bus Speed
- **112-Pin LQFP or 80-Pin QFP package**
  - — I/O lines with 3.3V/5V input and drive capability
  - — 3.3V/5V A/D converter inputs

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Table 1 List of MC9S12K-Family members

Flash	RAM	EEPROM	Package	Device	CAN	SCI	SPI	IIC	A/D	PWM	I/O
256K	12K	4K	112LQFP	KT256	3	2	3	1	16	8	91
				KG256	2	2	3	1	16	8	91
			80QFP	KG256	2	2	3	1	8	7	59
128K	8K	2K	112LQFP	KG128	2	2	3	1	16	8	91
			80QFP	KG128	2	2	3	1	8	7	59
64K	4K	1K	112LQFP	K64	1	2	2	1	16	8	91
			80QFP	K64	1	2	2	1	8	7	59
32K	2K	1K	80QFP	K32	1	2	1	0	8	7	59

- **Pin out explanations:**
  - — A/D is the number of A/D channels.
  - — I/O is the sum of ports capable to act as digital input or output.
    - 112 Pin Packages:
      - Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16 input only.
      - 22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)
    - 80 Pin Packages:
      - Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8 input only.
      - 11 inputs provide Interrupt capability (P= 7, J = 2, IRQ, XIRQ)
  - — CAN0 can be routed under software control from PM1:0 to pins PM3:2 or PM5:4.
  - — CAN4 pins are shared between IIC pins.
  - — CAN4 can be routed under software control from PJ7:6 to pins PM5:4 or PM7:6.
  - — Versions with 2 CAN modules will have CAN0 and CAN4.
  - — Versions with one CAN module will have CAN0.
  - — Versions with 2 SPI modules will have SPI0 and SPI1.
  - — Versions with 1 SPI will have SPI0.
  - — SPI0 can be routed to either Ports PS7:4 or PM5:2.
  - — SPI2 pins are shared with PWM7:4.
  - — In 112 pin versions SPI2 can be routed under software control to PH7:4.
  - — In 80 pin versions $\overline{SS}$ signal of SPI2 is not bonded out!

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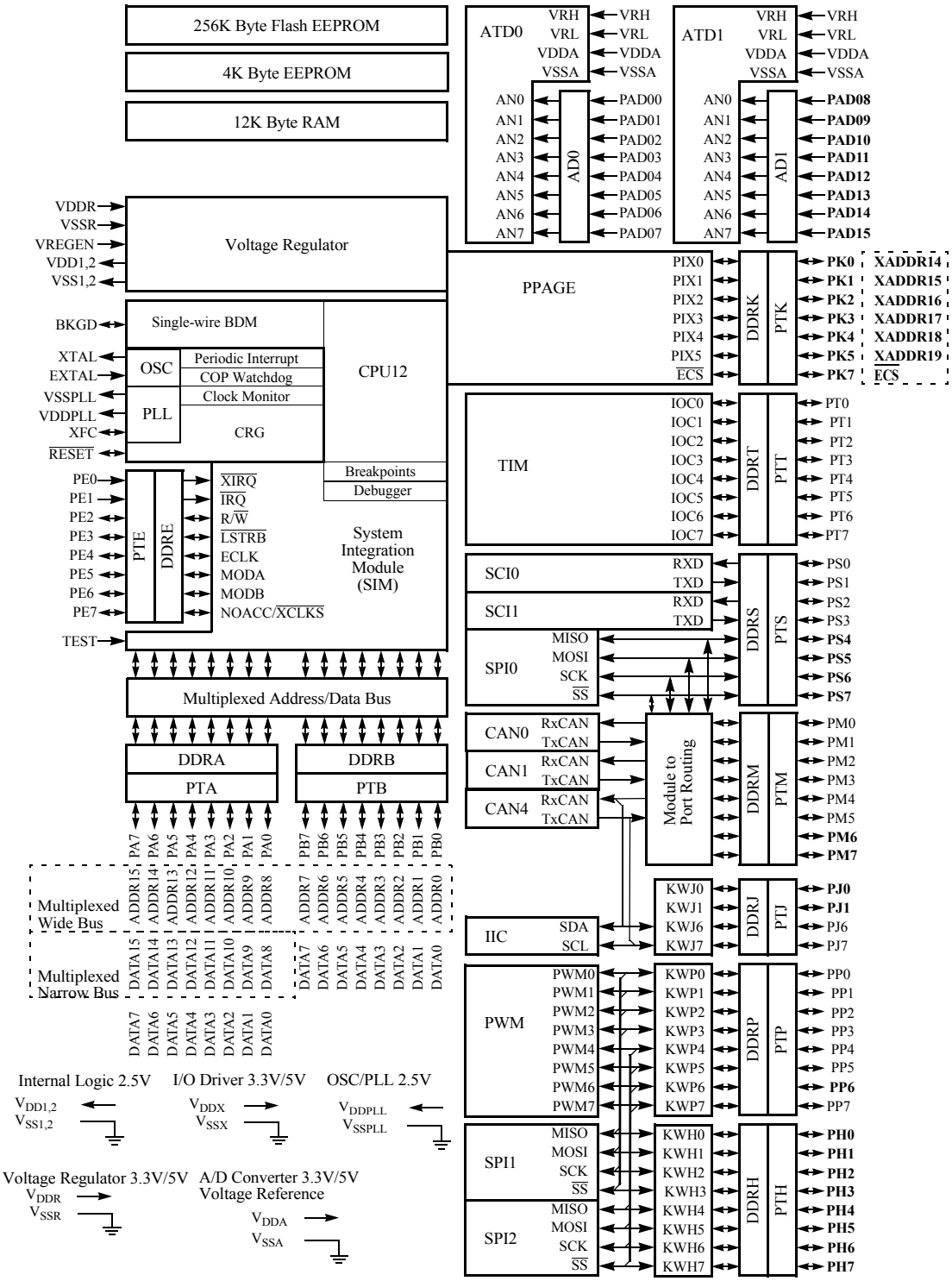
MC9S12KT256 Block Diagram



Signals shown in **Bold** are not available on the 80 Pin Package

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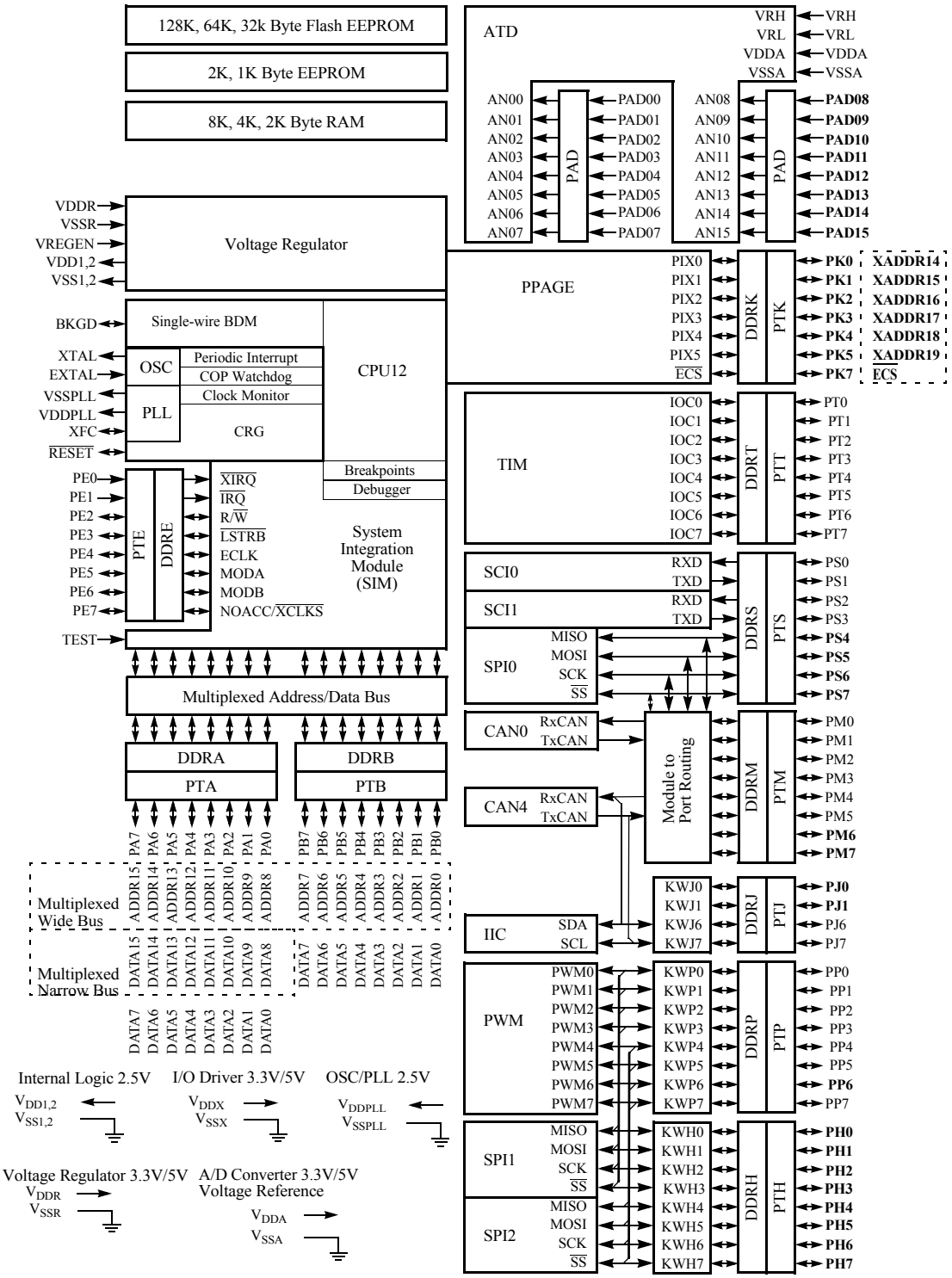
MC9S12KG128, MC9S12K64 and MC9S12K32 Block Diagram



Signals shown in **Bold** are not available on the 80 Pin Package.
CAN4 and SPI2 are only available on the MC9S12KG128.
IIC and SPI1 are not available on the MC9S12K32.

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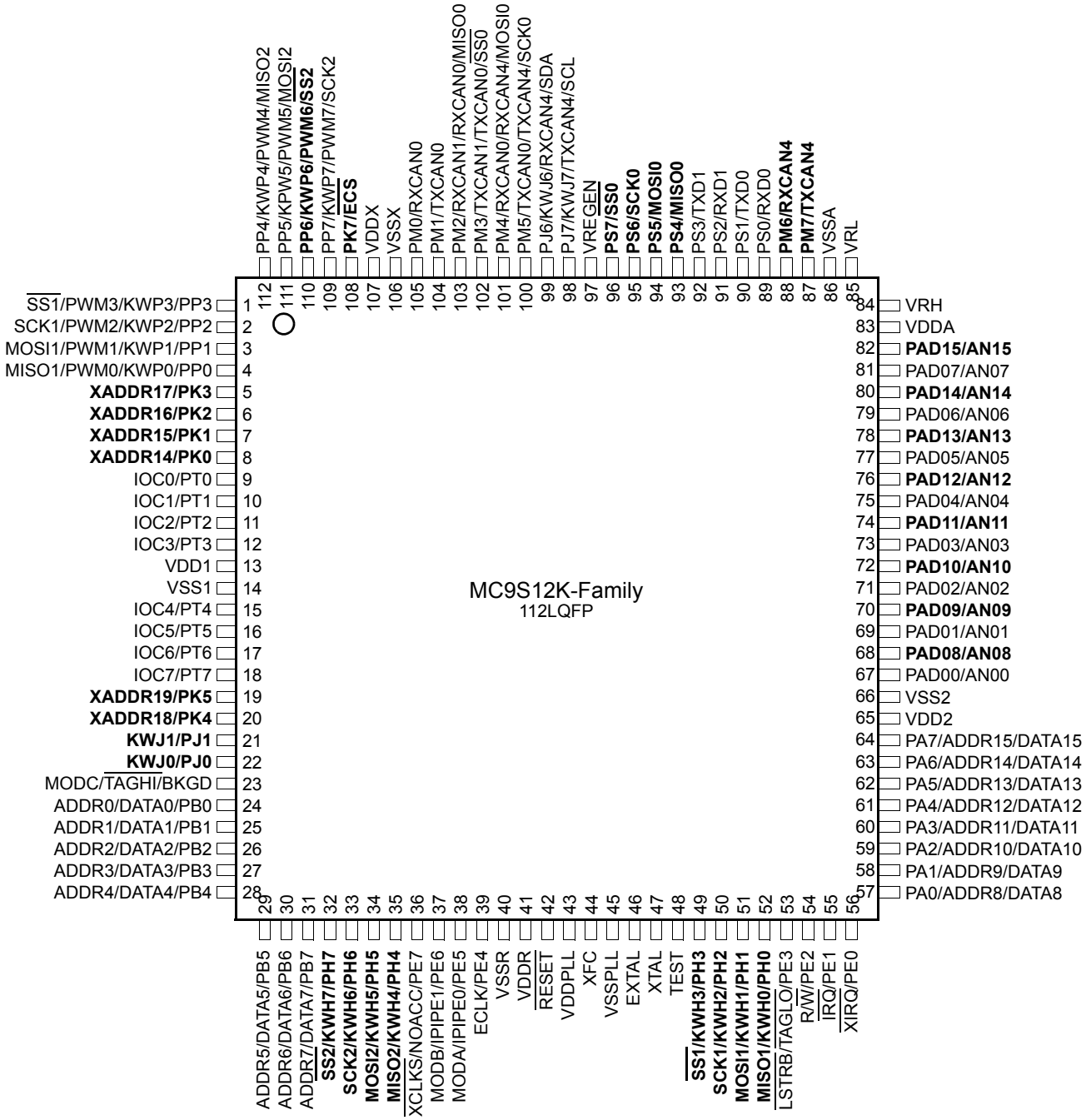
Pin assignments

Figure 1 Pin assignments 112 LQFP for MC9S12K-Family



Signals shown in **Bold** are not available on the 80 Pin Package

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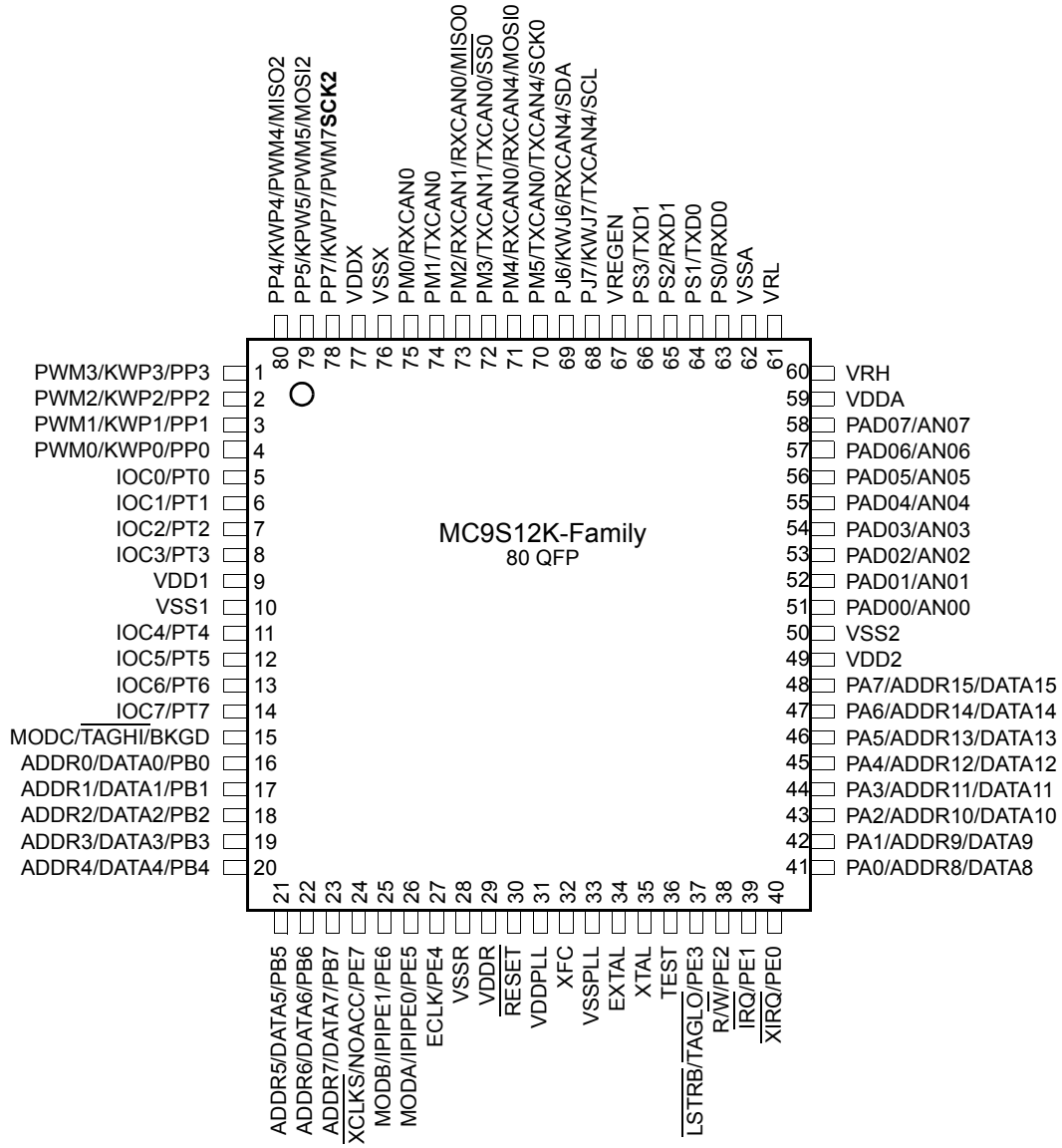
Figure 2 Pin Assignments in 80 QFP for MC9S12K-Family



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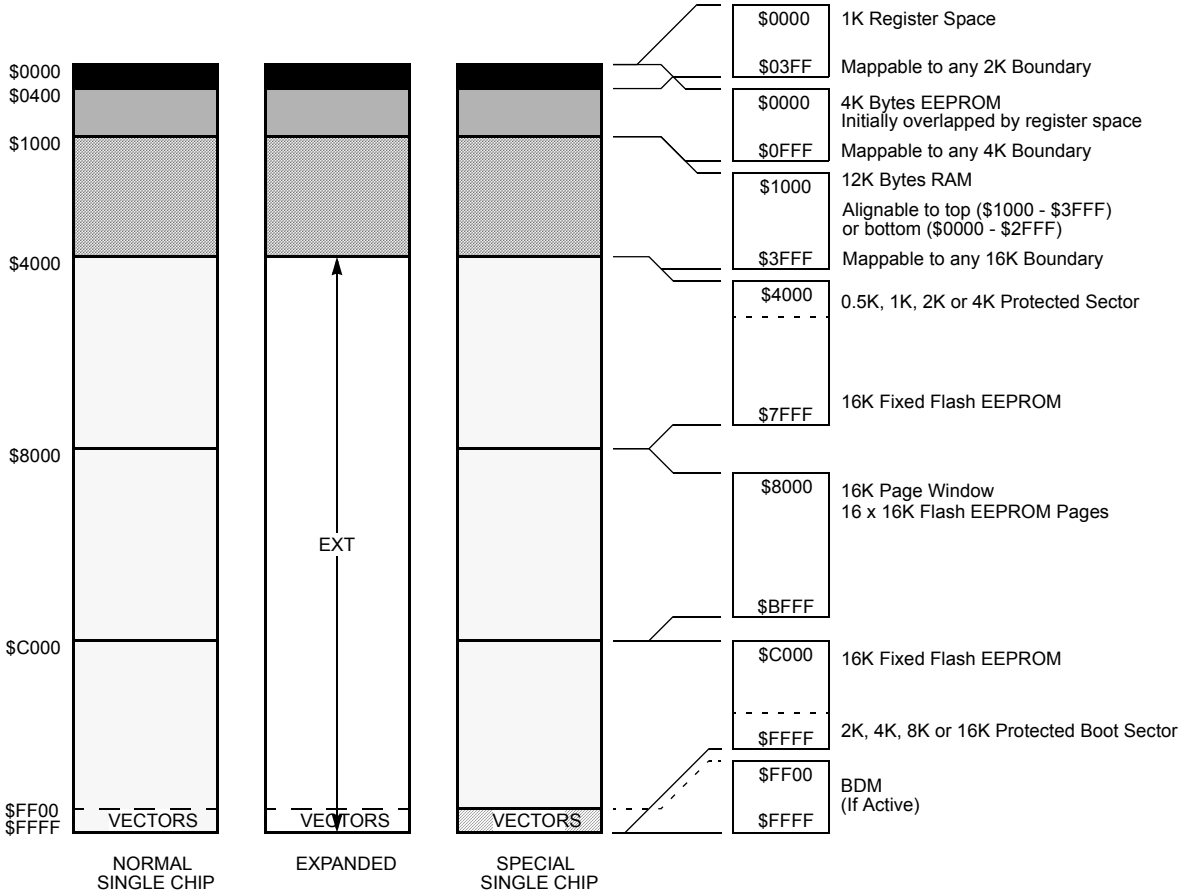
Memory Configurations

Figure 3 MC9S12Kx256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$1000 - $3FFF: 12K RAM
$0000 - $0FFF: 4K EEPROM (1K $0000 - $03FF not visible)

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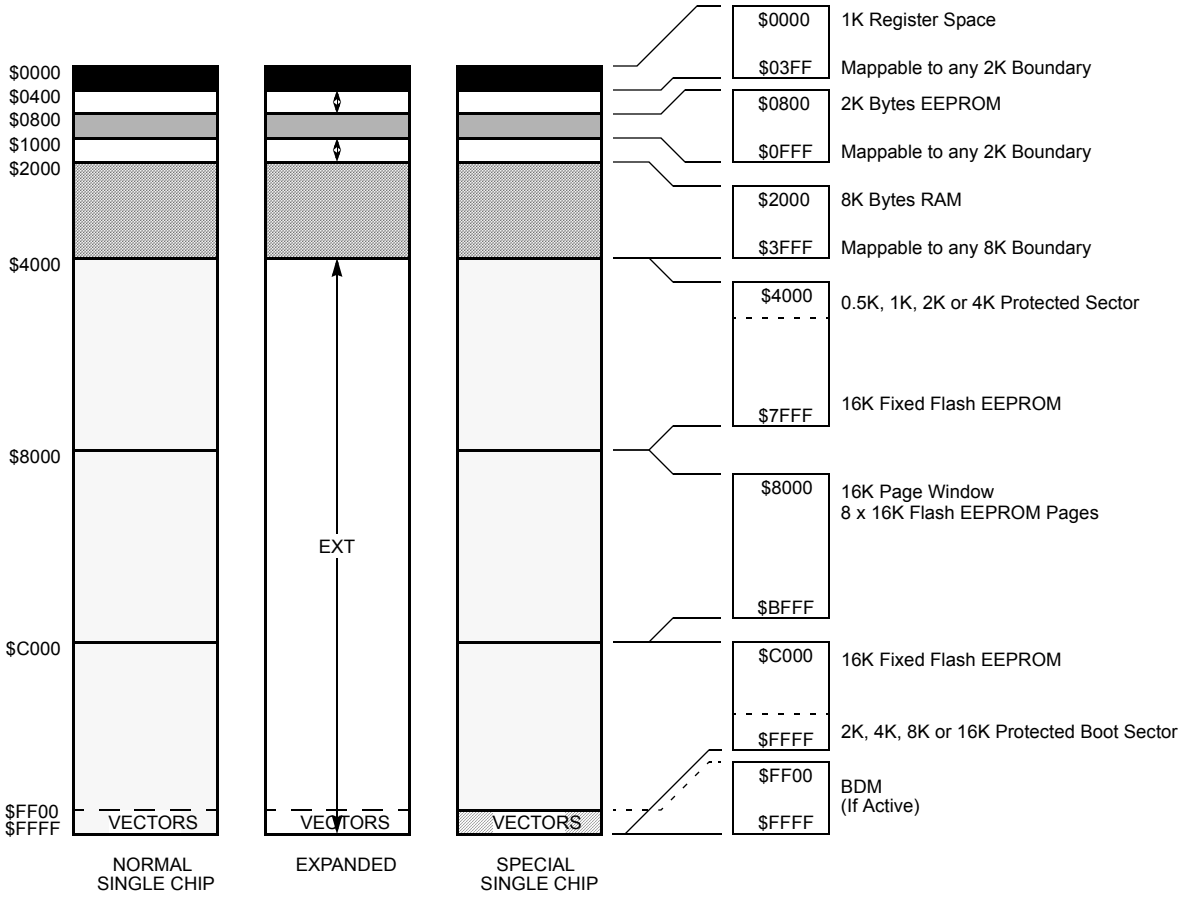
Figure 4 MC9S12KG128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM (1K $0000 - $03FF not visible)
$0000 - $07FF: 2K EEPROM (1K $0000 - $03FF not visible)

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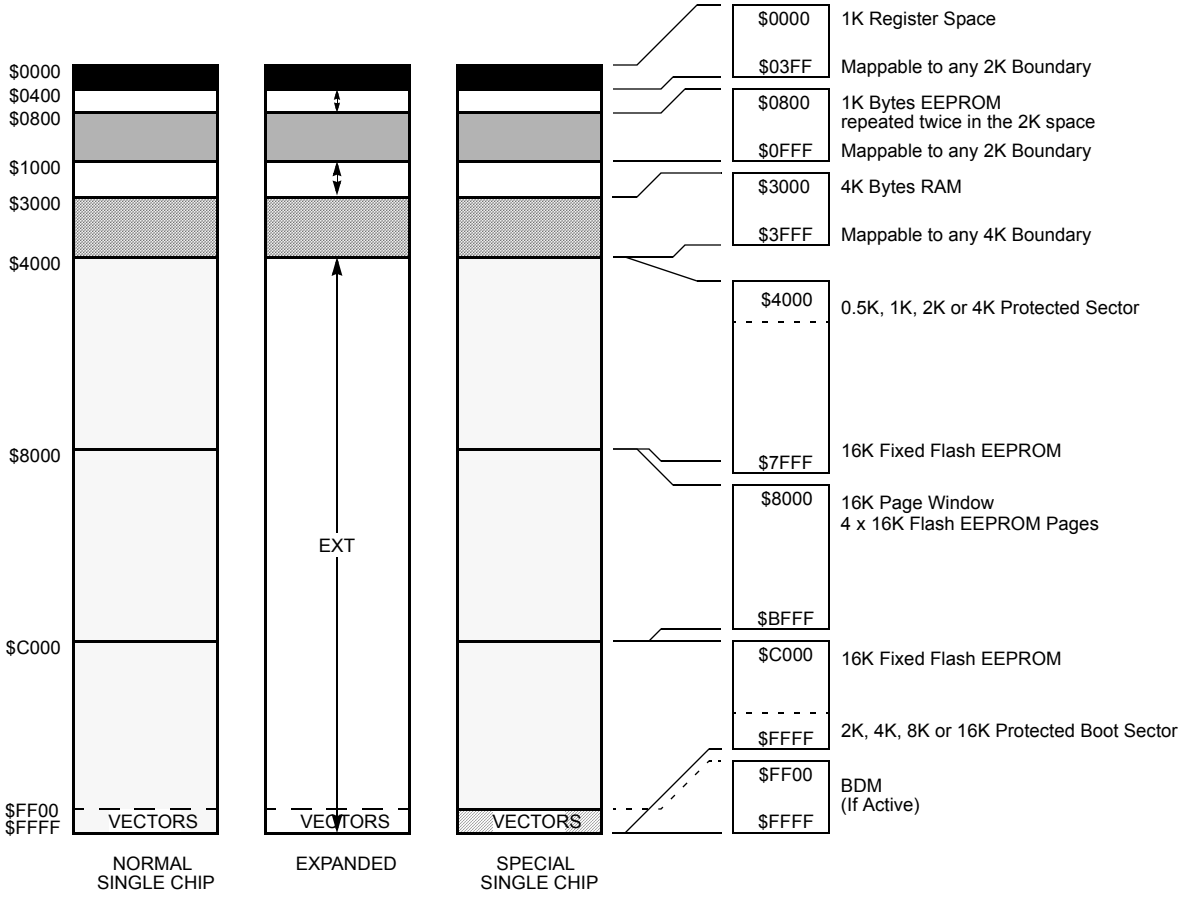
Figure 5 MC9S12K64 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $0FFF: 4K RAM (1K $0000 - $03FF not visible)
$0000 - $03FF: 1K EEPROM (not visible)

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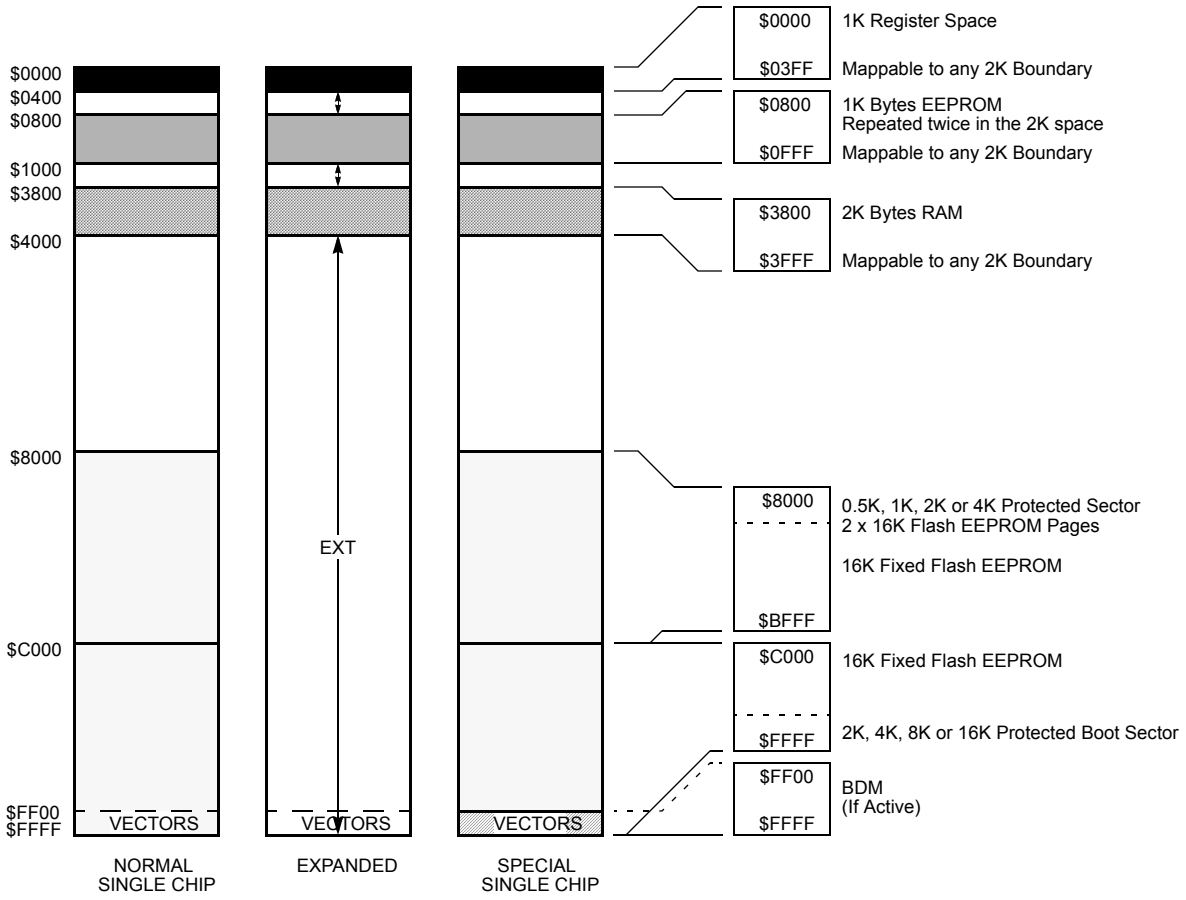
Figure 6 MC9S12K32 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0800 - $0FFF: 2K RAM
$0000 - $07FF: 1K EEPROM (not visible)

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