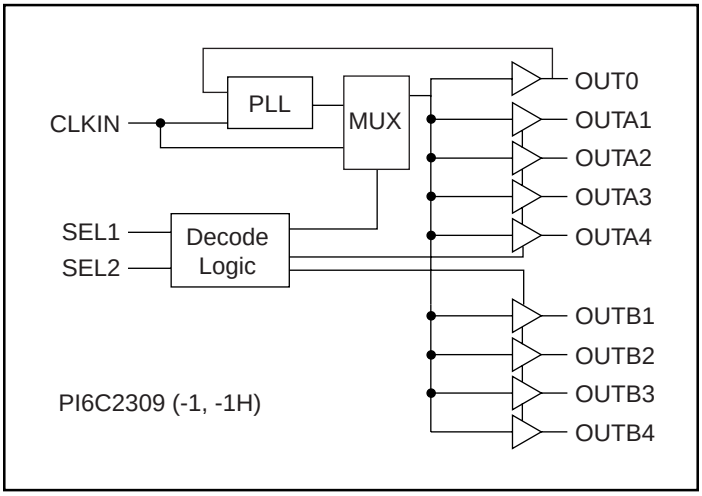
Product Features

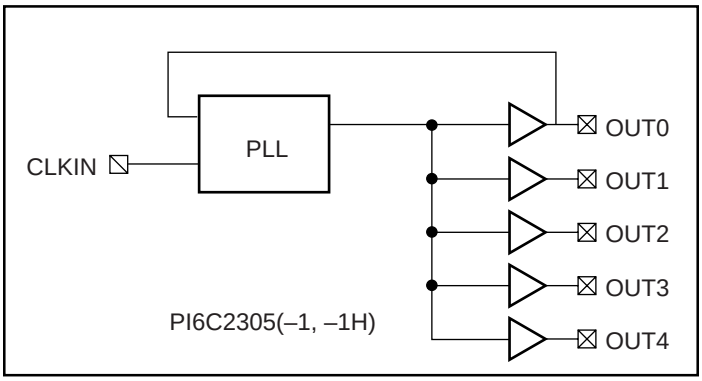
- Maximum rated frequency: 133 MHz
- Low cycle-to-cycle jitter
- Input to output delay, less than 200ps
- Internal feedback allows outputs to be synchronized to the clock input
- 5V tolerant input*
- Operates at 3.3V V_{DD}
- Space-saving Packages:
  150-mil SOIC (W)
  173-mil TSSOP (L)

* *FB_IN and CLKIN must reference the same voltage thresholds for the PLL to deliver zero delay skewing*

Block Diagram: PI6C2309



Block Diagram: PI6C2305



Functional Description

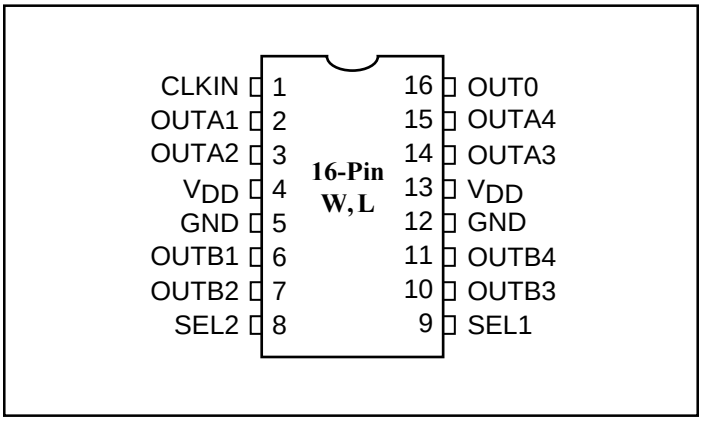
The PI6C230x is a PLL based, zero-delay buffer, with the ability to distribute five outputs on PI6C2305, nine outputs on PI6C2309 of up to 133MHz at 3.3V. All the outputs are distributed from a single clock input CLKIN and output CLK0 performs zero delay by connecting a feedback to PLL.

PI6C2309 has two banks of four outputs that can be controlled by the selection inputs, SEL1 & SEL2. It also has a powersparing feature: when input SEL1 is 0 and SEL2 is 1, PLL is turned off and all outputs are referenced from CLKIN. PI6C2305 is an 8-pin version of PI6C2309 without selection inputs. PI6C230X is available in high drive and industrial environment versions.

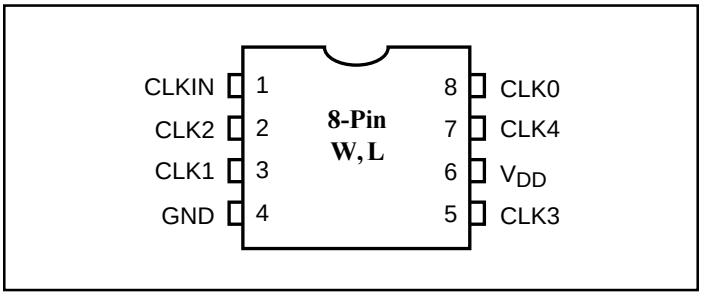
An internal feedback on OUT0 is used to synchronize the outputs to the input; the relationship between loading of this signal and the outputs determines the input-output delay. PI6C230X are characterized for both commercial and industrial operation

Notice: *This device is subject to import restriction. Please refer to the Import Restriction Notice under the Ordering Information section.*

Pin Configuration PI6C2309



Pin Configuration: PI6C2305



Input Select Decoding for PI6C2309

SEL2	SEL1	OUTA [1-4]	OUTB [1-4]	Output Source (OUT0)	PLL
0	0	3-State	3-State	PLL	ON
0	1	PLL	3-State	PLL	ON
1	0	CLKIN	CLKIN	CLKIN	OFF
1	1	PLL	PLL	PLL	ON

Pin Description for PI6C2309

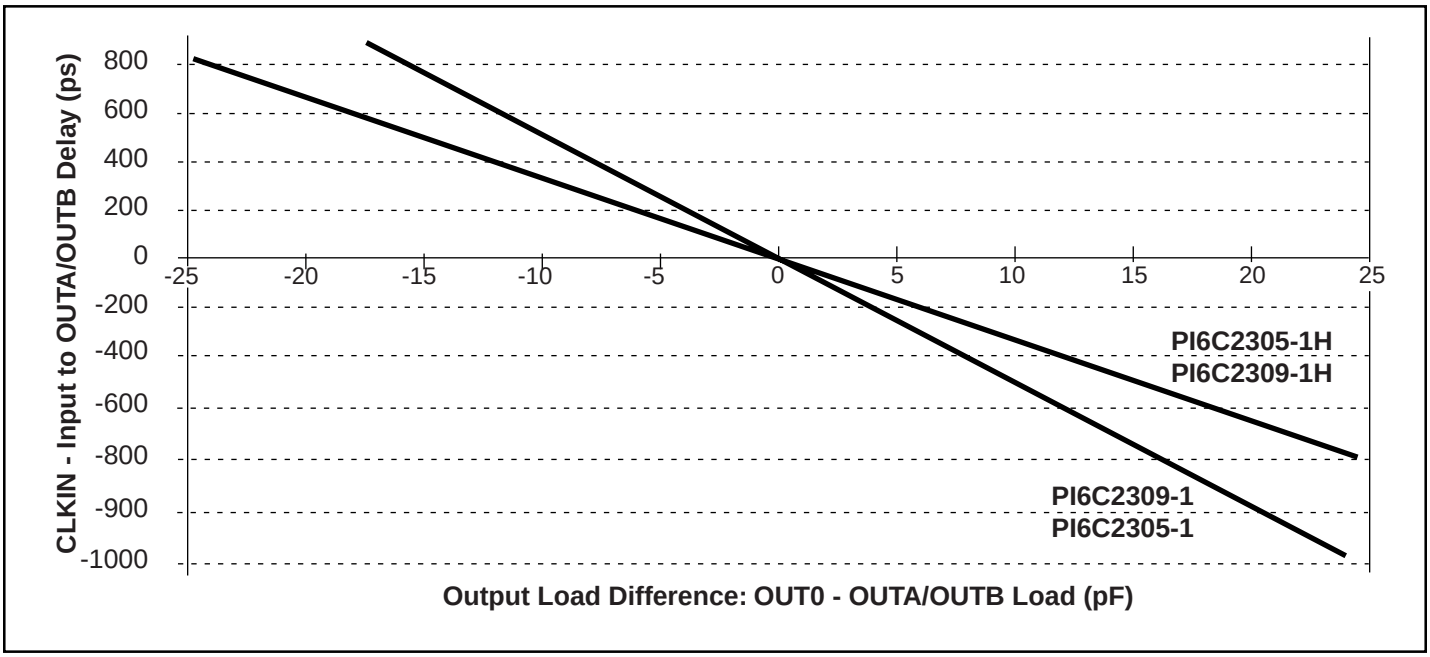
Pin	Signal	Description
1	CLKIN	Input clock reference frequency (weak pull-down)
2, 3, 14, 15	OUTA[1-4]	Clock output, Bank A (weak pull-down)
4, 13	V_{DD}	3.3V supply
5, 12	GND	Ground
6, 7, 10 ,11	OUTB[1-4]	Clock output, Bank B (weak pull-down)
8	SEL2	Select input, bit 2 (weak pull-up)
9	SEL1	Select input, bit 1 (weak pull-up)
16	OUT0	Clock Output , internal PLL feedback (weak pull-down)

Pin Description for PI6C2305

Pin	Signal	Description
1	CLKIN	Input clock reference frequency (weak pull-down)
2, 3, 5, 7	OUTA[1-4]	Clock output, Bank A (weak pull-down)
4	GND	3.3V supply
6	V_{DD}	Ground
8	OUT0	Clock output, internal PLL feedback (weak pull-down)

Zero Delay and Skew Control

CLKIN Input to OUTA/OUTB Delay vs. Difference in Loading between OUT0 pin and OUTA/OUTB pins



The relationship between loading of the FB_IN signal and other outputs determines the input-output delay. Zero delay is achieved when all outputs, including feedback, are loaded equally.

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V
DC Input Voltage (Except CLKIN) ..... –0.5V to V_{DD} +0.5V
DC Input Voltage CLKIN ..... –0.5 to 7V
Storage Temperature ..... –65°C to +150°C
Maximum Soldering Temperature (10 seconds) ..... 260°C
Junction Temperature ..... 150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions (V_{CC} = 3.3V ±0.3V)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commerical Operating Temperature	0	70	°C
	Industrial Operating Temperature	–40	85	
C_L	Load Capacitance, below 100 MHz	—	30	pF
	Load Capacitance, from 100 MHz to 133 MHz	—	15	
C_{IN}	Input Capacitance	—	7	

DC Electrical Characteristics for Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	
V_{OL}	Output LOW Voltage	I_{OL} = 8mA (–1); I_{OL} = 12mA (–1H)		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8mA (–1); I_{OH} = –12mA (–1H)	2.4		
I_{DD} (PI6C2309)	Bypass, PLL OFF	SEL1 = 0, SEL2 = 1		25.0	µA
I_{DD}	Supply Current	Unloaded outputs 100 MHz, Select inputs at V_{DD} or GND		54.0	mA
		Unloaded outputs 66 MHz, CLKIN		39.0	

AC Electrical Characteristics for Industial Temperature Devices

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F_O	Output Frequency	30pF load (–1, –1H)	10.0		100	MHz
		20pF load, (–1H)			133	
		15pF load, (–1, –1H)				
t_{DC}	Duty Cycle(1) (–1)	Measured at V_{DD}/2, F_{OUT} <66.67MHz 30pF load	40.0	50	60.0	%
		Measured at V_{DD}/2, F_{OUT} <45MHz 15pF load	45.0		55.0	
	Duty Cycle(1) (–1H)	Measured at V_{DD}/2, F_{OUT} <133MHz 15pF load	40.0		60.0	
		Measured at V_{DD}/2V, F_{OUT} <45MHz 30pF load	45.0		55.0	
t_R	Rise Time(1) (–1, –2, –3, –4,)	Measured between 0.8V and 2.0V, 30pF load			2.2	ns
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Rise Time(1) (–1H)	Measured between 0.8V and 2.0V, 30pF load			1.50	
t_F	Fall Time(1) (–1)	Measured between 0.8V and 2.0V, 30pF load			2.50	
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Fall Time(1) (–1H)	Measured between 0.8V and 2.0V, 30pF load			1.25	
$t_{SK(O)}$	Output to Output Skew (–1,–1H)(1)	All outputs equally loaded			200	ps
t_0	Delay, CLKIN Rising Edge to OUT0 Rising Edge(1)	Measured at V_{DD}/2		0	±350	
$t_{SK(D)}$	Device-to-Device Skew(1)	Measured at V_{DD}/2 on OUT0 pins of devices		0	600	
t_{SLEW}	Output Slew Rate(1)	Measured between 0.8V & 2.0V on –1H device using Test Crt #2	1			V/ns
t_{JIT}	Cycle-to-Cycle Jitter(1) (–1,–1H)	Measured at 66.67 MHz, loaded 30pF load			200	ps
		Measured at 133 MHz, loaded 15pF load			100	
t_{LOCK}	PLL Lock Time(1)	Stable power supply, valid clocks presented on CLKIN pin			1.0	ms

Notes: 1.See Switching Waveforms on page 6.

DC Electrical Characteristics for Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage	—	—	0.8	V
V_{IH}	Input HIGH Voltage	—	2.0	—	
I_{IL}	Input LOW Current	V_{IN} = 0V	—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	—	100	
V_{OL}	Output LOW Voltage	I_{OL} = 8mA (–1); I_{OL} = 12mA (–1H)	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8mA (–1); I_{OH} = –12mA (–1H)	2.4	—	
I_{DD} (PI6C2309)	Bypass, PLL off	SEL1 = 0 SEL2 = 1	—	25	µA
I_{DD}	Supply Current	Unloaded outputs, 66.67 MHz, Select inputs at V_{DD} or GND	—	39	mA
I_{DD}	Supply Current	Unloaded outputs 100 MHz Select Inputs @ V_{DD} or GND	—	54	

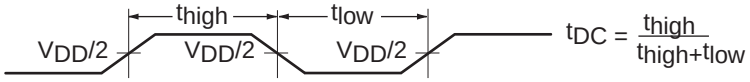
AC Electrical Characteristics for Commercial Temperature Device

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F_O	Output Frequency	30pF load (–1, –1H)	10		100	MHz
		20pF load, (–1H)			133	
		15pF load, (–1, –1H)				
t_{DC}	Duty Cycle(1) (–1H)	Measured at V_{DD}/2, F_O< 66MHz, 30pF	45	50	55	%
	Duty Cycle (–1)	Measured at V_{DD}/2, F_O< 66MHz, 30pF	40	50	60	
t_R	Rise Time(1) @30pF	Measured between 0.8V and 2.0V			2.2	ns
	Rise Time(1) @15pF				1.5	
	Rise Time(1) @30pF (–1H)				1.5	
t_F	Fall Time(1) @30pF				2.2	
	Fall Time(1) @15pF				1.5	
	Fall Time(1) @30pF (–1H)				1.25	
$t_{SK(O)}$	Output to Output Skew(1) (–1,–1H)	All outputs equally loaded, V_{DD}/2			200	ps
t_0	Input to Output Delay, CLKIN Rising Edge to OUT0 Rising Edge(1)	Measured at V_{DD}/2		0	±350	
$t_{SK(D)}$	Device to Device Skew(1)	Measured at V_{DD}/2 on OUT0 pins of devices		0	600	
t_{SLEW}	Output Slew Rate(1)	Measured between 0.8V and 2.0V on –1H device using Test Circuit #2	1			V/ns
t_{JIT}	Cycle-to-Cycle Jitter(1) (–1,–1H)	Measured at 66.67 MHz, loaded 30pF outputs			200	ps
		Measured at 133 MHz, loaded 15pF outputs			100	
t_{LOCK}	PLL Lock Time(1)	Stable power supply, valid clocks presented on CLKIN pins			1.0	ms

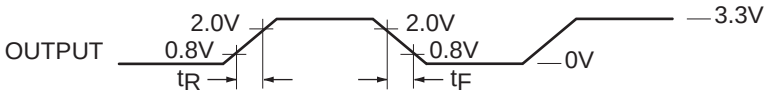
Notes:
1. See Switching Waveforms on page 6

Switching Waveforms

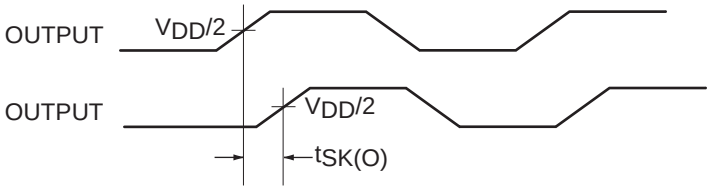
Duty Cycle Timing



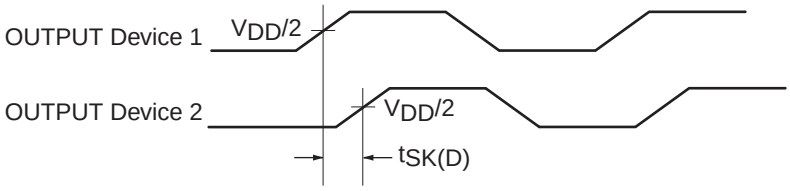
All Outputs Rise/Fall Time



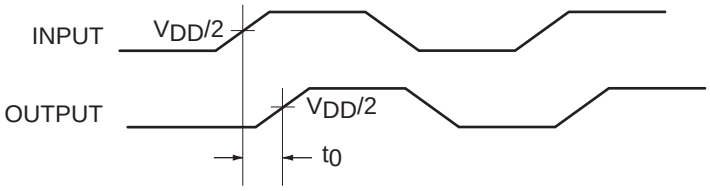
Output-Output Skew



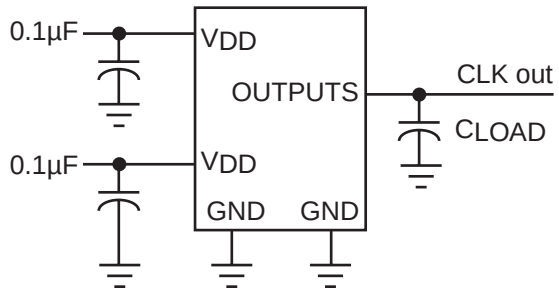
Device-Device Skew



Input-Output Propagation Delay

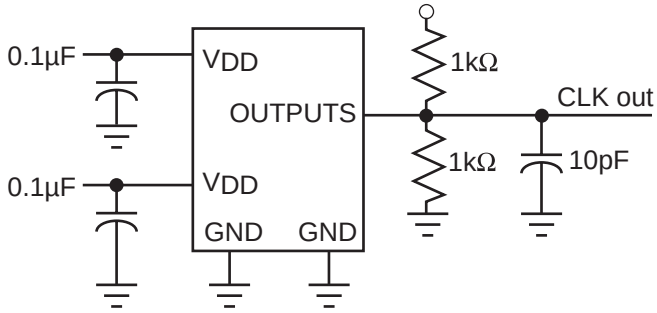


Test Circuit 1



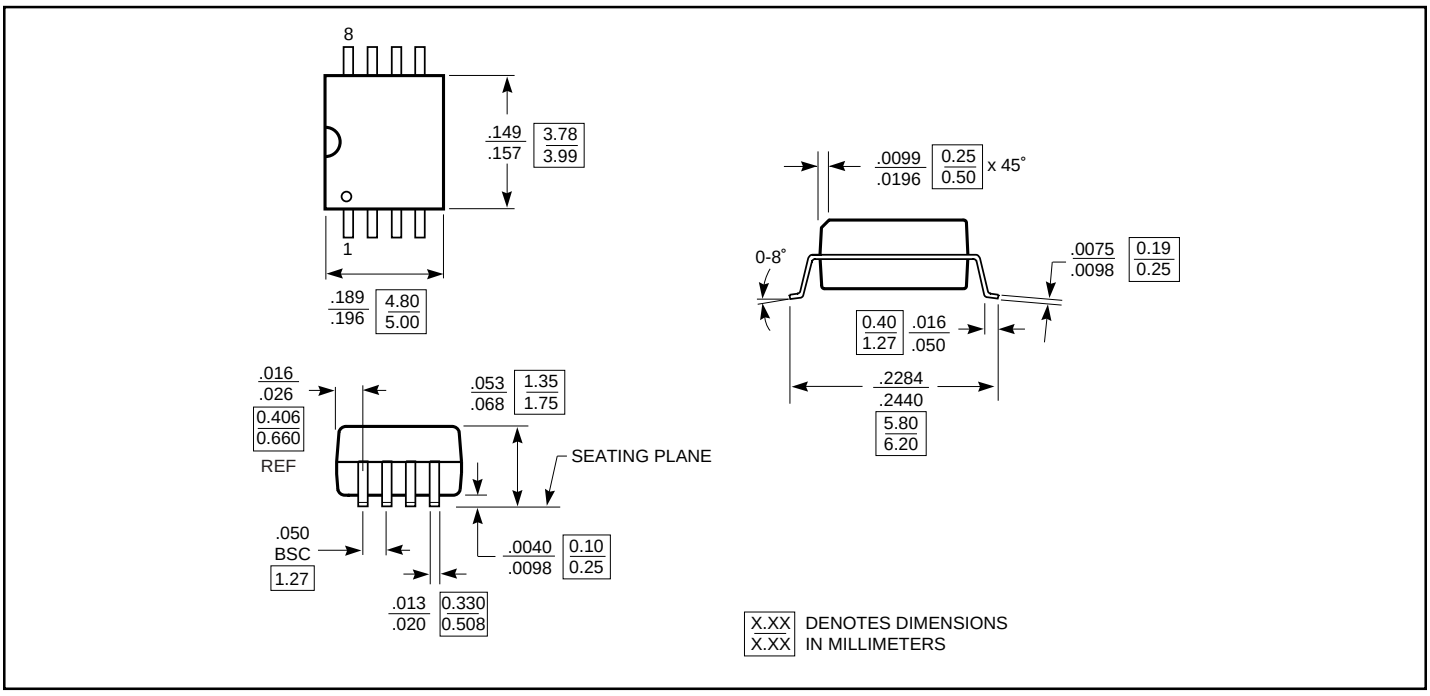
Test Circuit for all parameters except t_{SLEW}

Test Circuit 2

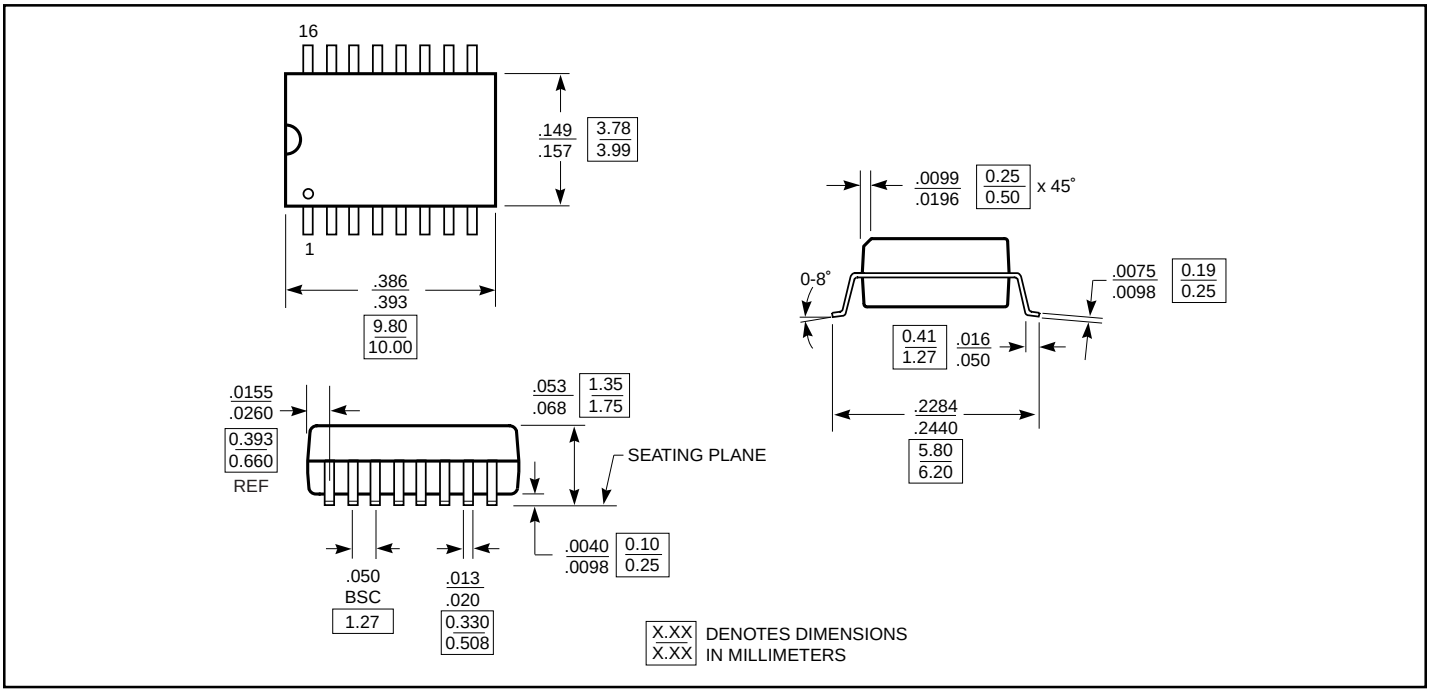


Test Circuit for t_{SLEW} ,Output slew rate on –1H device

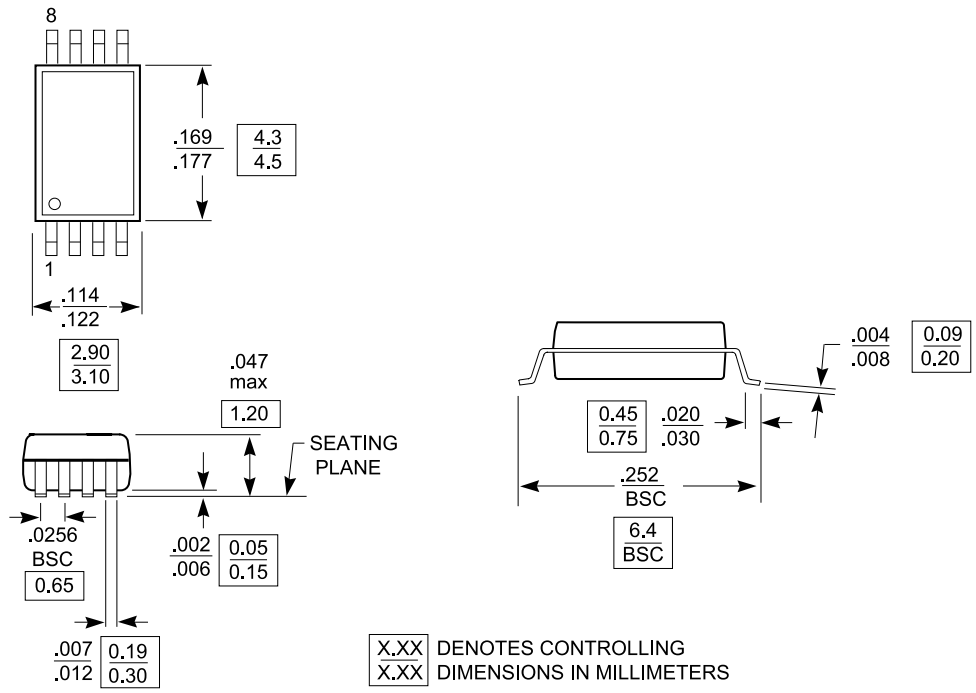
8-Pin SOIC (W) Package



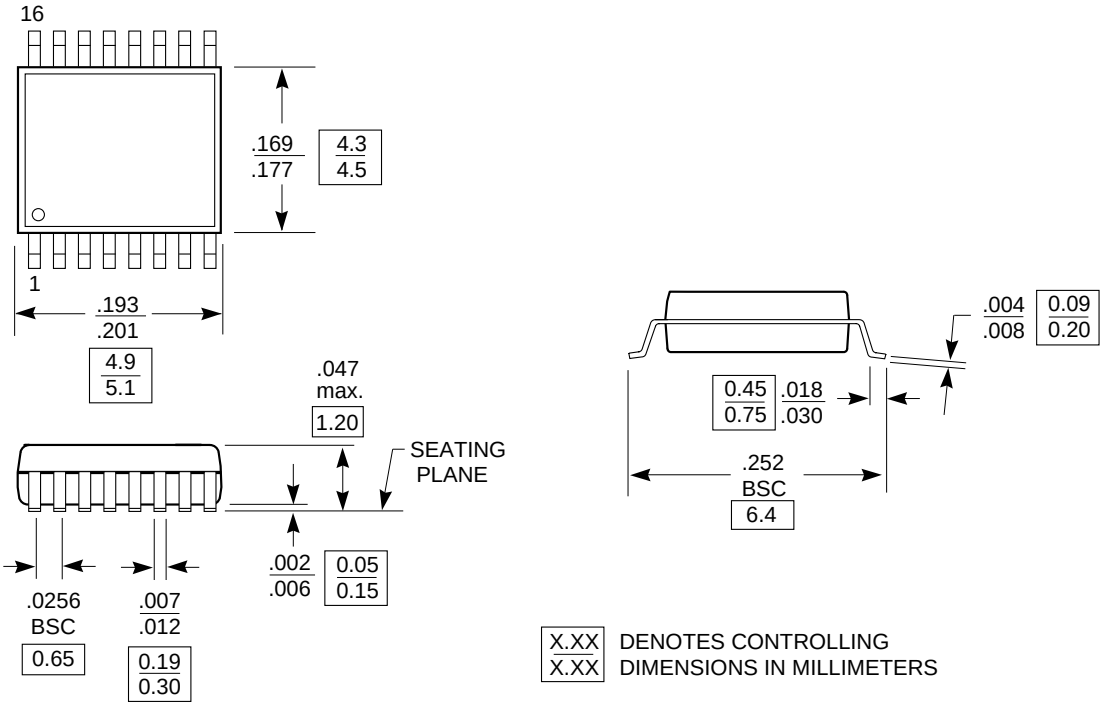
16-Pin SOIC (W) Package



8-Pin TSSOP (L) Package



16-Pin TSSOP (L) Package



Note: Controlling dimensions in millimeters. Ref: JEDEC MS - 012 AC

Ordering Information PI6C2309

Ordering Code	Package Name	Package Type	Operating Range
PI6C2309-1W	W16	16-pin 150-mil SOIC	Commercial
PI6C2309-1HW			
PI6C2309-1L	L16	16-pin TSSOP	
PI6C2309-1HL			
PI6C2309-1WI	W16	16-pin 150-mil SOIC	Industrial
PI6C2309-1HWI			
PI6C2309-1LI	L16	16-pin TSSOP	
PI6C2309-1HLI			

Ordering Information PI6C2305

Ordering Code	Package Name	Package Type	Operating Range
PI6C2305-1W	W8	8-pin 150-mil SOIC	Commercial
PI6C2305-1HW			
PI6C2305-1L	L8	8-pin TSSOP	
PI6C2305-1HL			
PI6C2305-1WI	W8	8-pin 150-mil SOIC	Industrial
PI6C2305-1HWI			
PI6C2305-1LI	L18	8-pin TSSOP	
PI6C2305-1HLI			

Import Restriction Notice:

Due to an agreement to settle a patent dispute, this device is only available for sale outside of the US and may not be subsequently re-imported into the US as an individual component or as incorporated into equipment. Any sale is expressly conditioned on the customer's agreement not to export the device or any product or equipment containing the device to the United States. Pericom disclaims any liability for indemnity or other obligation or warranty if the devices or any product or equipment containing the devices are imported in violation of this agreement.