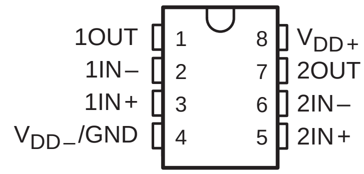
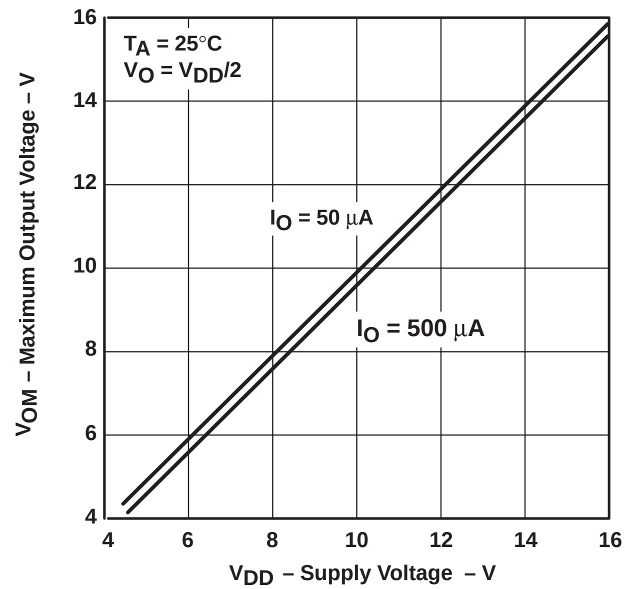
- **Free-Air Operating Temperature −40°C to 150°C**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High Unity-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage 300 μV Typ at T_A = 25°C**
- **Macromodel Included**

D OR P PACKAGE
(TOP VIEW)



MAXIMUM OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



description

The TLC2872Z is a dual rail-to-rail output operational amplifier manufactured using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance while having better noise, input offset voltage and power dissipation than existing CMOS operational amplifiers. In addition, the common-mode input voltage range is wider than typical standard CMOS type amplifiers. To take advantage of this improvement in performance, making this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. Also, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The TLC2872Z, manufactured using Texas Instruments high-temperature process flow, allows extended temperature operation up to 150°C in a plastic package. This adds extra reliability at the extended temperature and reduces the need for expensive hermetically sealed ceramic packages.

The TLC2872Z, which exhibits high input impedance and low noise, is excellent for small signal conditioning of high impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split supplies makes this device a great choice for inputs to ADCs in either the unipolar or bipolar mode of operation. This feature, combined with its temperature performance, makes the TLC2872Z ideal for sonobuoys, pressure sensors, temperature controls, active VR sensors, accelerometers, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 150°C	2.5 mV	TLC2872ZD	TLC2872ZP	TLC2872Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2872DR).

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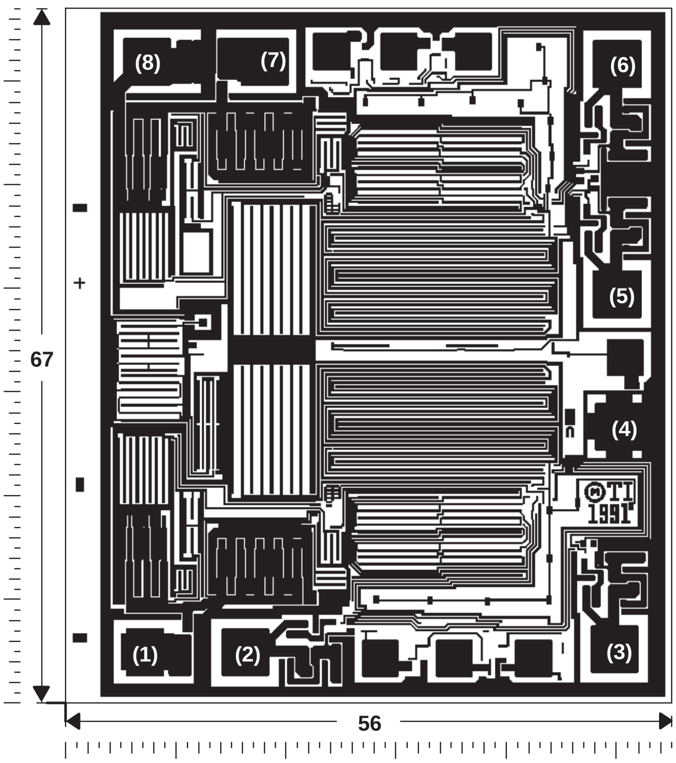
description (continued)

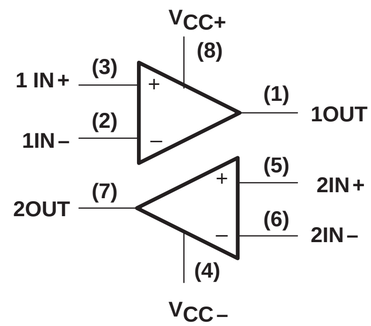
The inputs and outputs of this device are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V. The device is characterized for operation over the extended (Z) temperature range of –40°C to 150°C.

TLC2872Y chip information

This chip, when properly assembled, displays characteristics similar to TLC2872Z. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

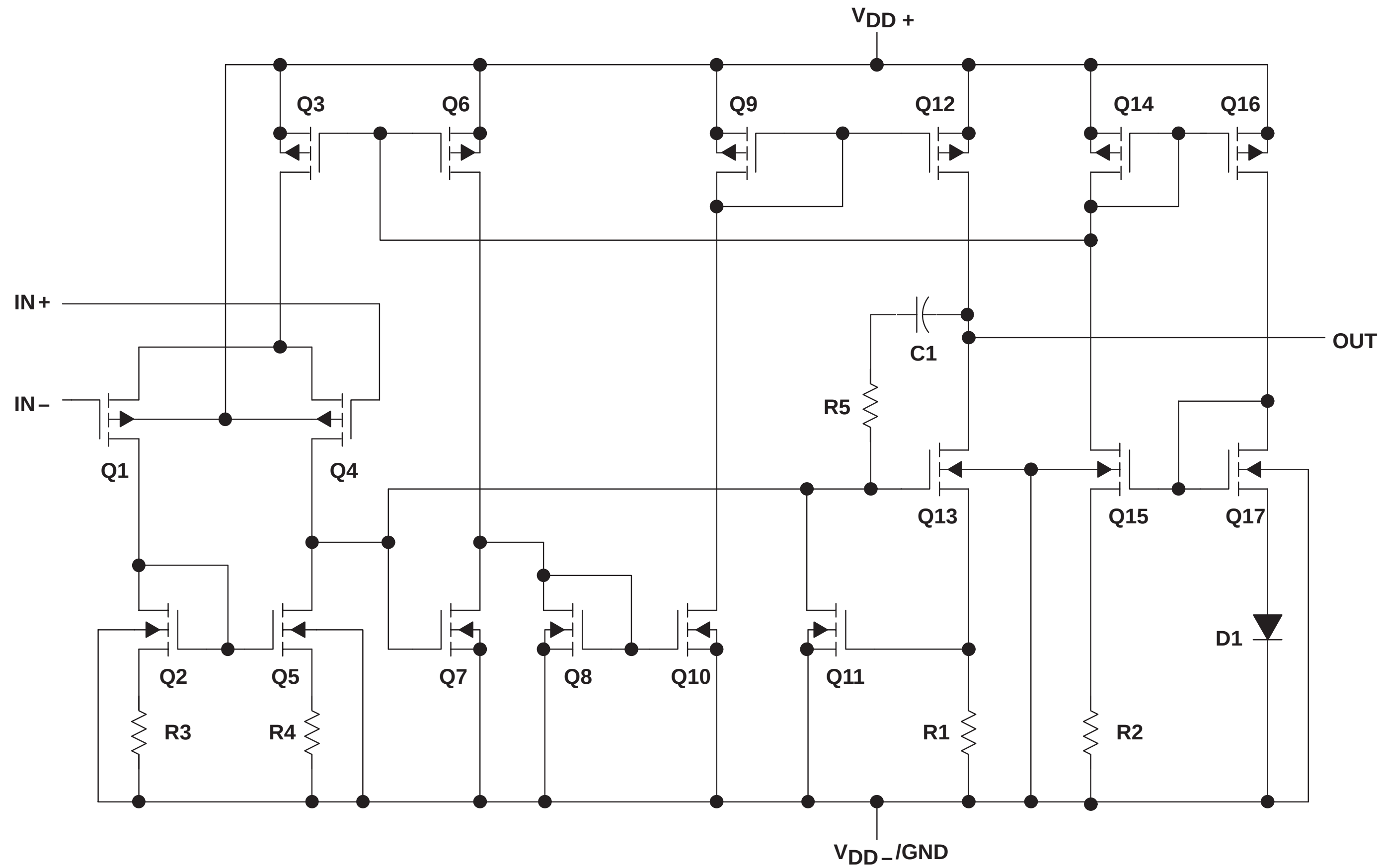
$T_{J\,max}$ = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT	COUNT†
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} . . . . 8 V
Supply voltage, V_{DD-} . . . . –8 V
Differential input voltage, V_{ID} (see Note 1) . . . . ±16 V
Input voltage range, V_I (any input, see Note 2) . . . . ±8 V
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Total current into V_{DD+} . . . . ±50 mA
Total current out of V_{DD-} . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 150°C
Storage temperature range . . . . –65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
2. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mW	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mW	8 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	–40	150	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2872Z			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		300	2500	µV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 150°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.0005		nA
				Full range			3	
I_{IB}	Input bias current			25°C		0.001		nA
				Full range			5	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$		25°C	4.95	4.99		V
		$I_{OH} = -200\ \mu A$		25°C	4.85	4.93		
				Full range	4.75			
		$I_{OH} = -1$ mA		25°C	4.25	4.65		
				Full range	4.25			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50\ \mu A$	25°C		0.01	0.02	V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500\ \mu A$	25°C		0.09	0.15	
				Full range			0.2	
		$V_{IC} = 2.5$ V,	$I_{OL} = 5$ mA	25°C		0.9	1.5	
				Full range			2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 10\ k\Omega$‡	25°C	15	35		V/mV
				Full range	10			
			$R_L = 1\ M\Omega$‡	25°C		175		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	$A_V = 10$	25°C		140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	75		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		2.2	3	mA
				Full range			3	

† Full range is −40°C to 150°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2872Z			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	2.3	3.6		V/µs
				Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50		nV/√Hz
		f = 1 kHz		25°C		9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.4		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		1		MHz
	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		µs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		50°		
	Gain margin			25°C		10		dB

† Full range is –40°C to 150°C.
‡ Referenced to 2.5 V

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electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2872Y MIN	TLC2872Y TYP	TLC2872Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		300	2500	μV
	Input offset voltage long-term drift (see Note 4)				0.002		μV/mo
I_{IO}	Input offset current				0.0005		nA
I_{IB}	Input bias current				0.001		nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	0 to 4	–0.3 to 4.2		V
				0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –20 μA		4.95	4.99		V
		I_{OH} = –200 μA		4.85	4.93		
		I_{OH} = –1 mA		4.25	4.65		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01	0.02	V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	70	75		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load	$V_{IC} = V_{DD}/2$,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		2.2	3	mA

† Referenced to 2.5 V

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2872Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ†, C_L = 100 pF†		2.3	3.6		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1		µV
		f = 0.1 to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ†	A_V = 1		0.0013%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ†, C_L = 100 pF†			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ†, C_L = 100 pF†			1		MHz
	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ†, C_L = 100 pF†	To 0.1%		1.5		µs
			To 0.01%		2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ†, C_L = 100 pF†			50°		
	Gain margin				10		dB

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
α_{VIO}	Input offset voltage temperature coefficient	Distribution	2
I_{IB}/I_{IO}	Input bias and offset currents	vs Free-air temperature	3
V_I	Input voltage range	vs Free-air temperature	4
V_{OH}	High-level output voltage	vs Output current	5
V_{OL}	Low-level output voltage	vs Output current	6, 7
V_{OM}	Maximum output voltage	vs Frequency	8
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	9 10
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	11 12 13
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	14 15
SR	Slew rate	vs Load capacitance vs Free-air temperature	16 17
ϕ_m	Phase margin	vs Frequency vs Load capacitance	12 18
	Gain margin	vs Load capacitance	19

NOTE: All loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2872Z
INPUT OFFSET VOLTAGE

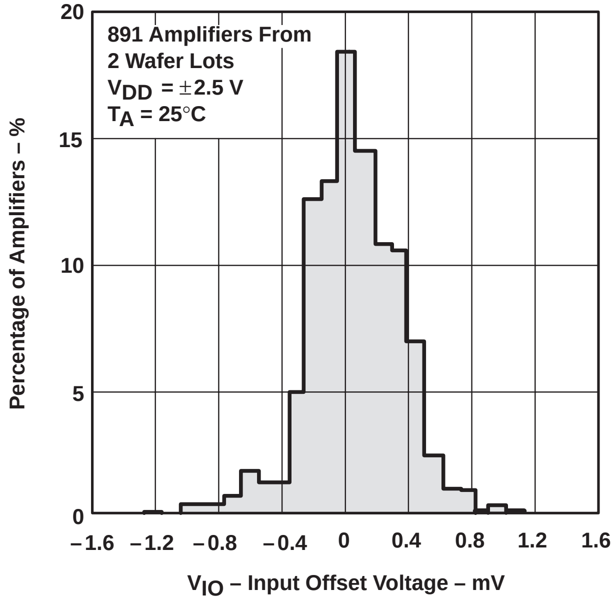


Figure 1

DISTRIBUTION OF TLC2872Z
TEMPERATURE COEFFICIENT

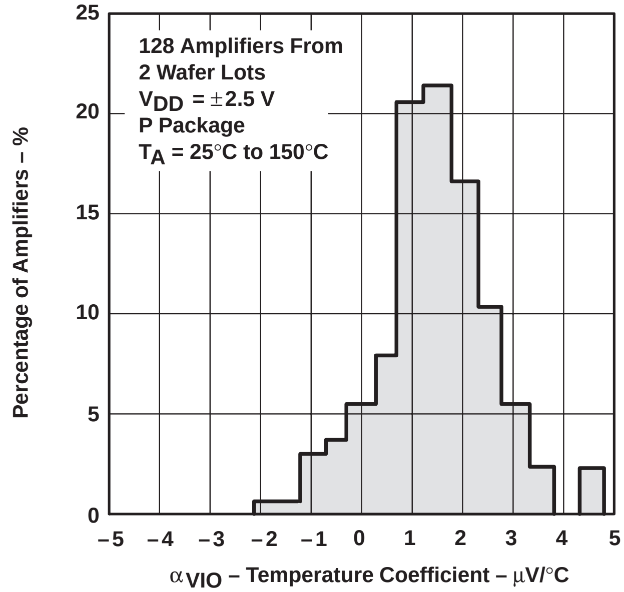


Figure 2

INPUT BIAS AND OFFSET CURRENTS
vs
FREE-AIR TEMPERATURE

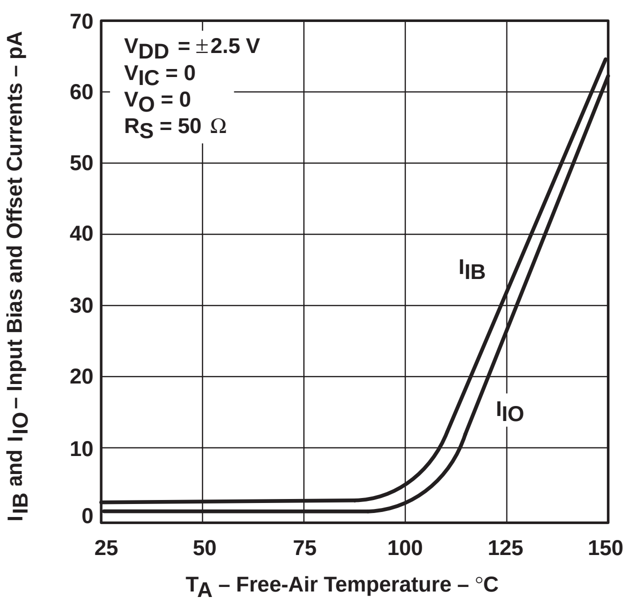


Figure 3

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

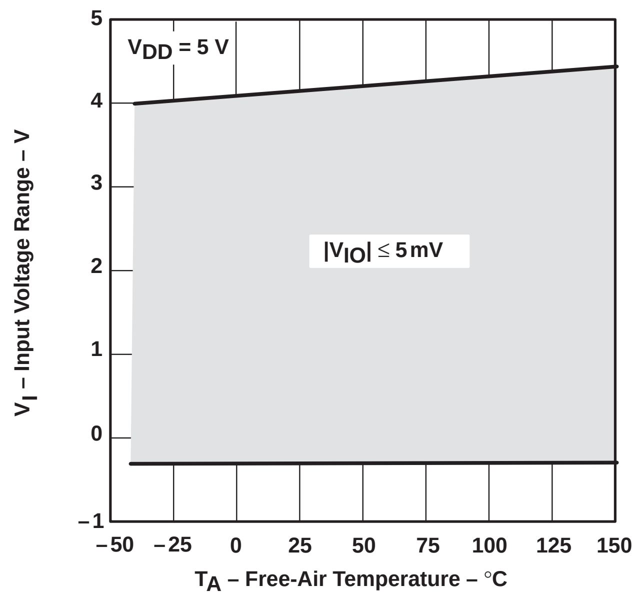


Figure 4

TYPICAL CHARACTERISTICS

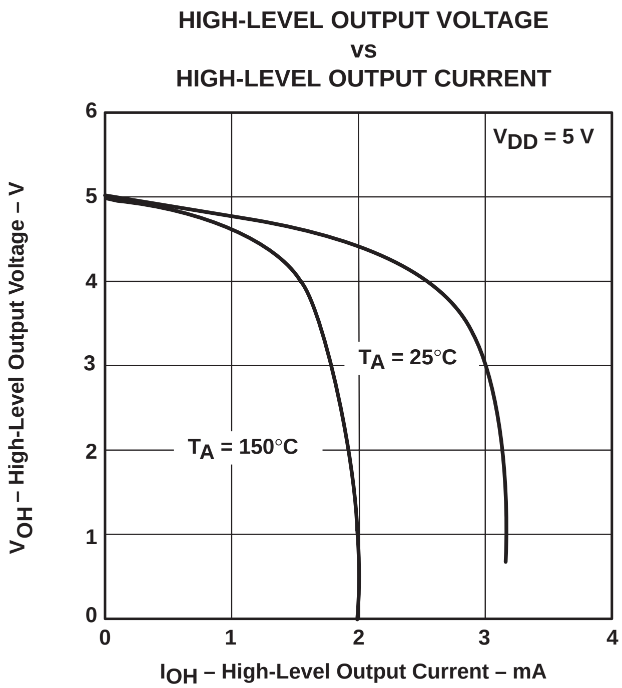


Figure 5

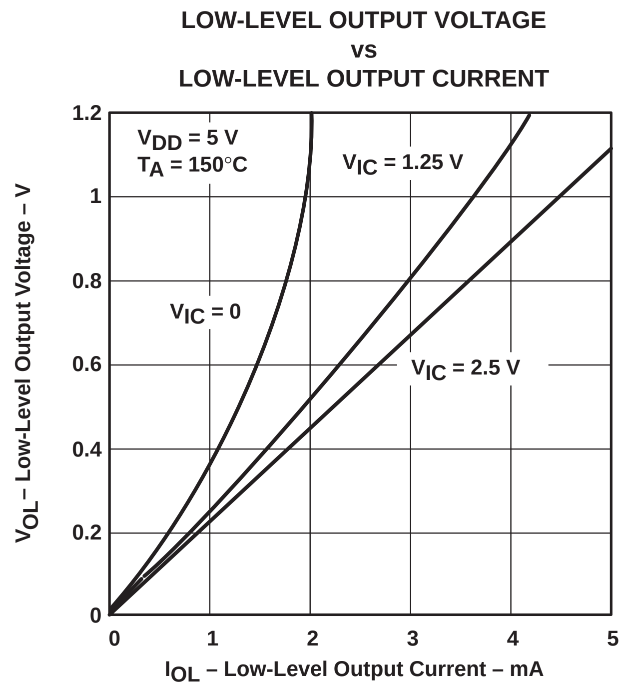


Figure 6

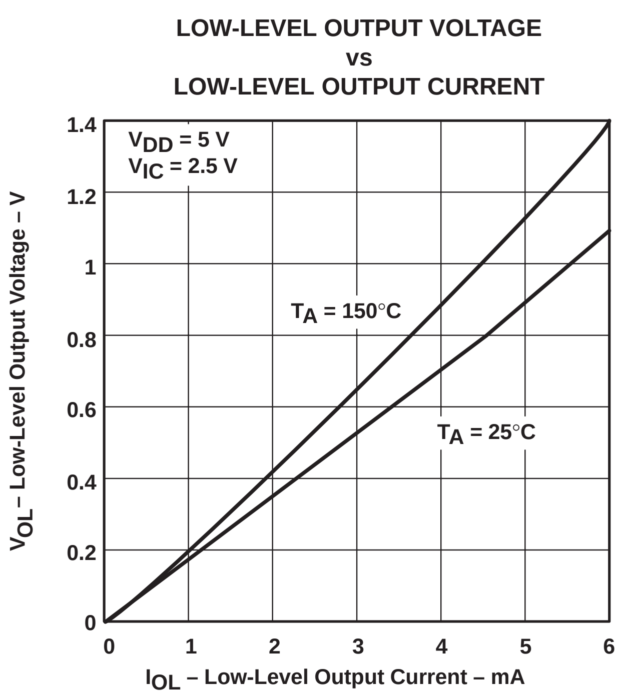


Figure 7

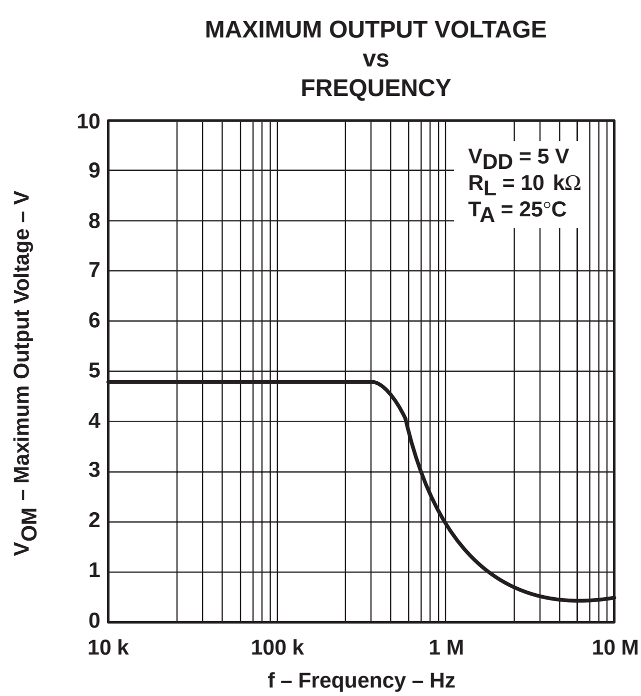


Figure 8

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

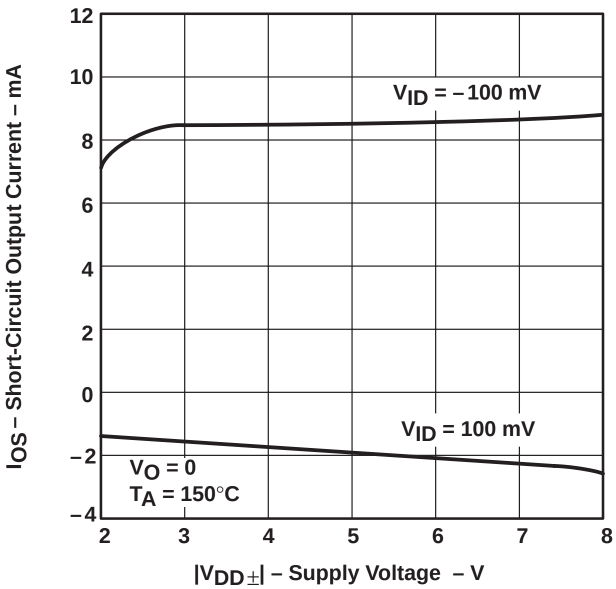


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

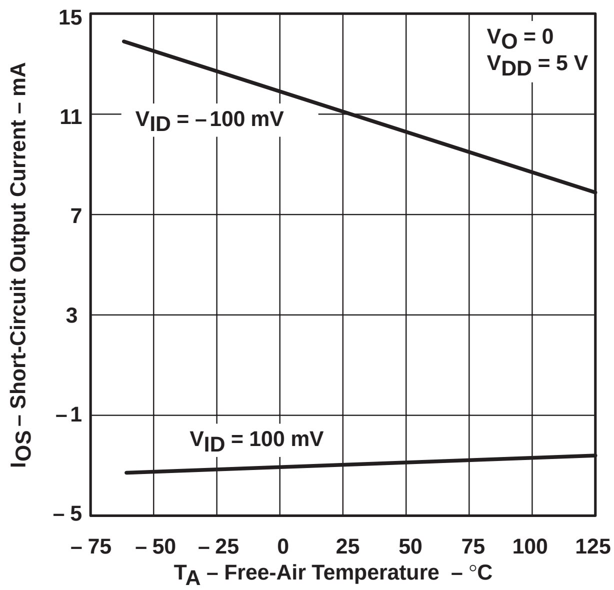


Figure 10

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

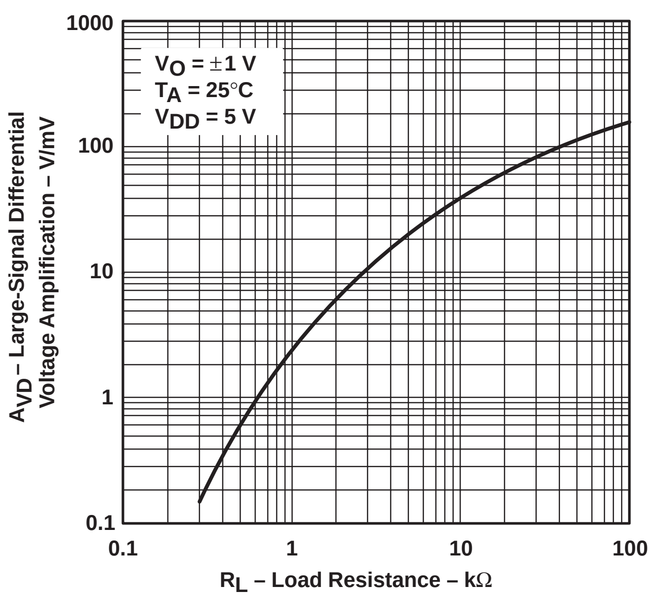


Figure 11

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE MARGIN vs FREQUENCY

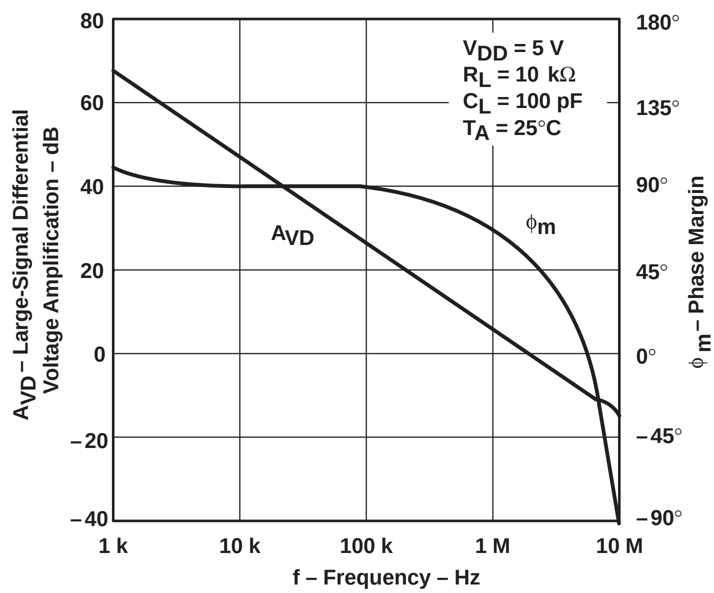


Figure 12

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

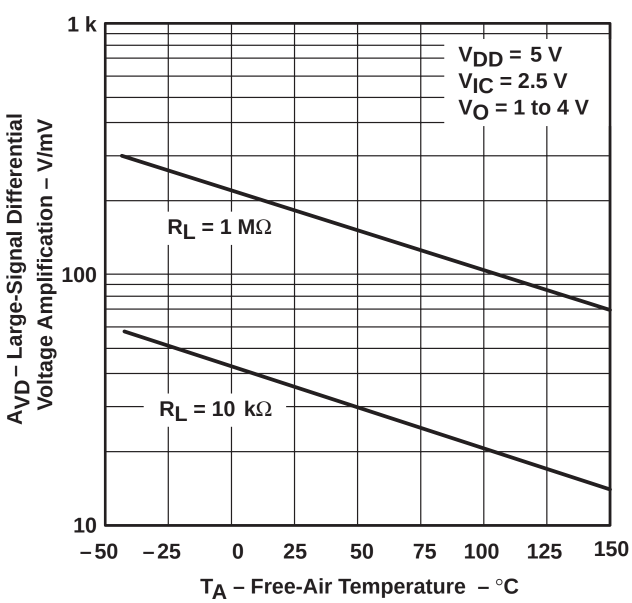


Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

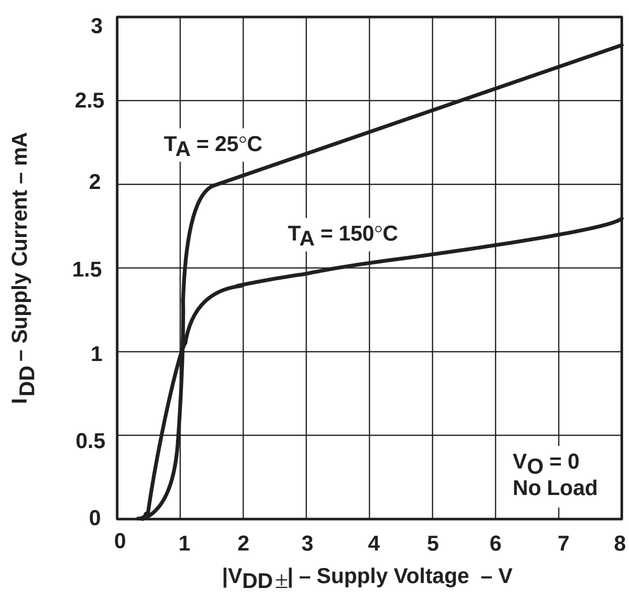


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

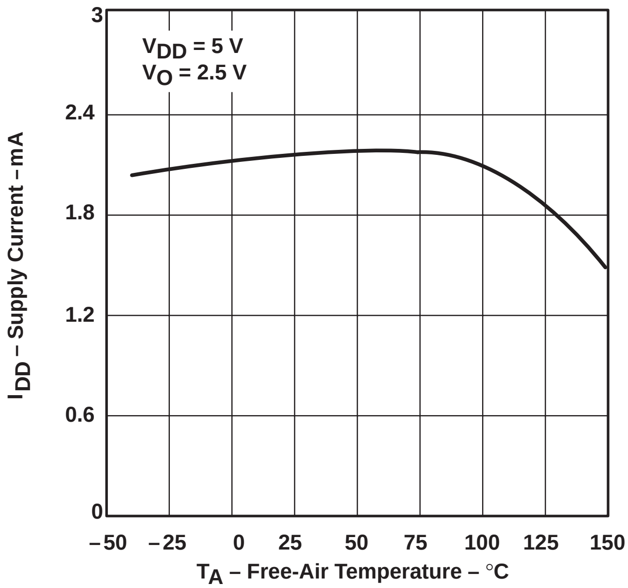


Figure 15

SLEW RATE vs LOAD CAPACITANCE

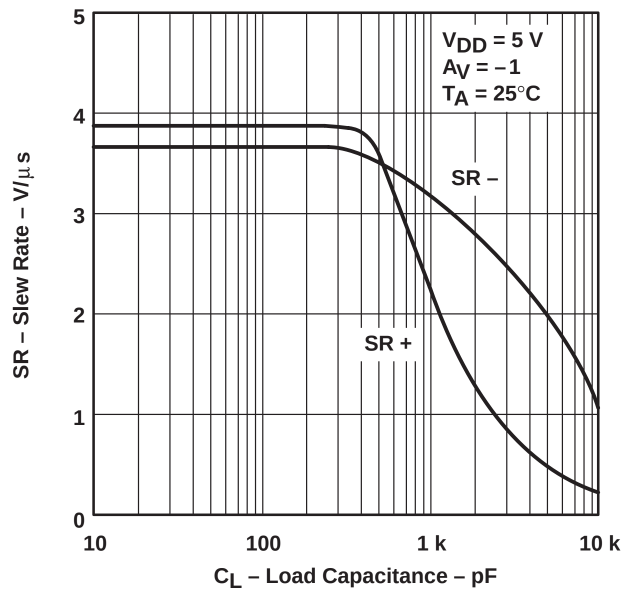


Figure 16

SLEW RATE vs FREE-AIR TEMPERATURE

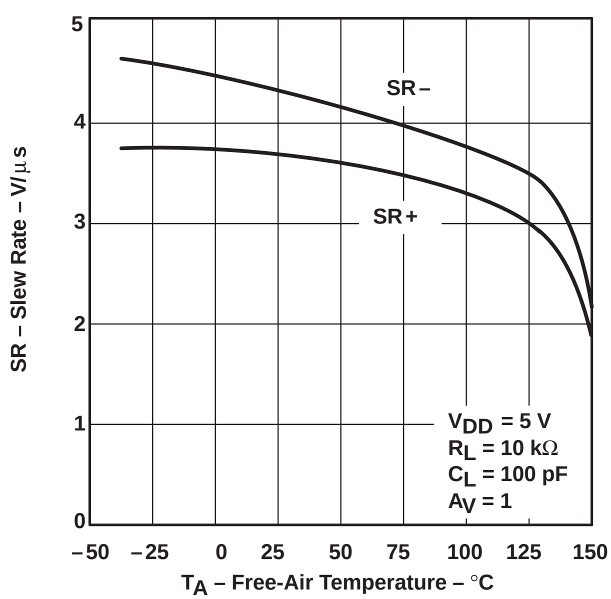


Figure 17

PHASE MARGIN vs LOAD CAPACITANCE

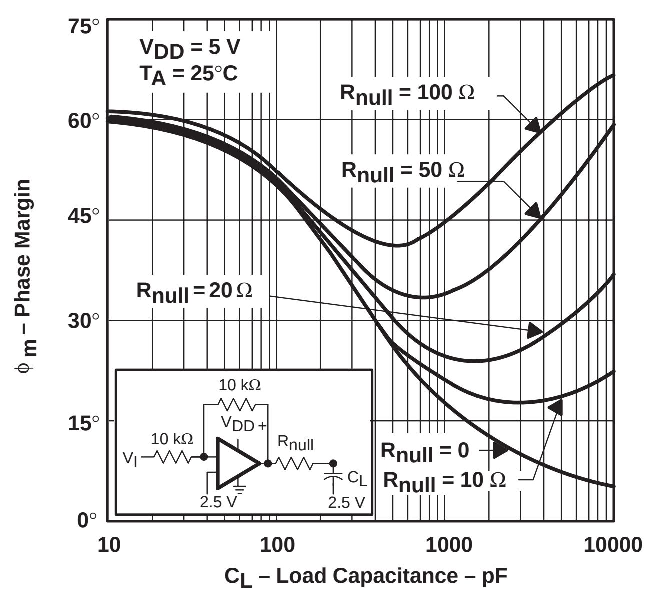


Figure 18

TYPICAL CHARACTERISTICS†

GAIN MARGIN
vs
LOAD CAPACITANCE

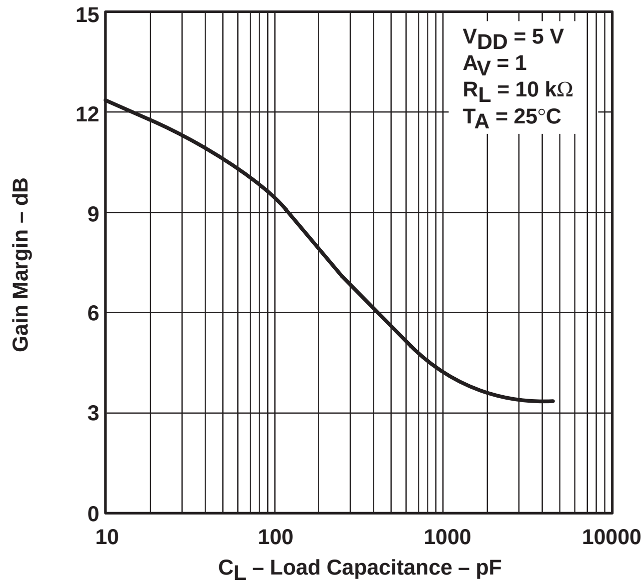


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

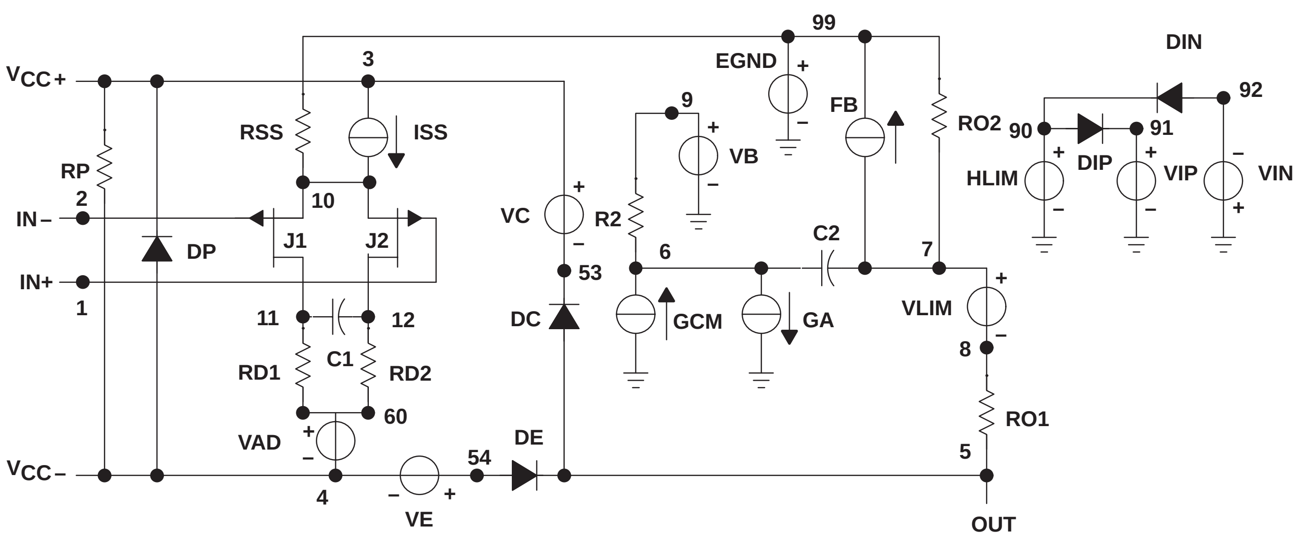
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 20 were generated using the TLC2872Z typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLC2872 1 2 3 4 5
   C1     11   12   14E–12
   C2     6    7    60.00E–12
   DC     5    53   DX
   DE     54   5    DX
   DLP    90   91   DX
   DLN    92   90   DX
   DP     4    3    DX
   EGND   99   0    POLY (2) (3,0) (4,0) 0 .5 .5
   FB 7   99   POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 –1E6 1E6 1E6 –1E6
   GA     6    0    11 12 377.0E–6
   GCM 0 6 10 99 134E–9
   ISS    3    10   DC 216.OE–6
   HLIM   90   0    VLIM 1K
   J1     11   2    10 JX
   J2     12   1    10 JX
   R2     6    9    100.OE3
   RD1  60  11  2.653E3
   RD2  60  12  2.653E3
   R01  8   5   50
   R02  7   99  50
   RP   3   4   4.310E3
   RSS  10  99  925.9E3
   VAD  60  4   –.5
   VB   9   0   DC 0
   VC 3 53 DC .78
   VE   54  4   DC .78
   VLIM 7   8   DC 0
   VLP  91  0   DC 1.9
   VLN  0   92  DC 9.4
 .MODEL DX D(IS=800.0E–18)
 .MODELJXPJF(IS=1.500E–12BETA=1.316E3
 + VTO=–.270)
 .ENDS
```

Figure 20. Boyle Macromodel and Subcircuit

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