



## 1024K X 16 BIT LOW POWER CMOS SRAM

**FEATURES**

- Fast access time : 55ns
- Low power consumption:  
Operating current : 45/30mA (TYP.)  
Standby current : 10μA (TYP.) LL-version  
4μA (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I

**GENERAL DESCRIPTION**

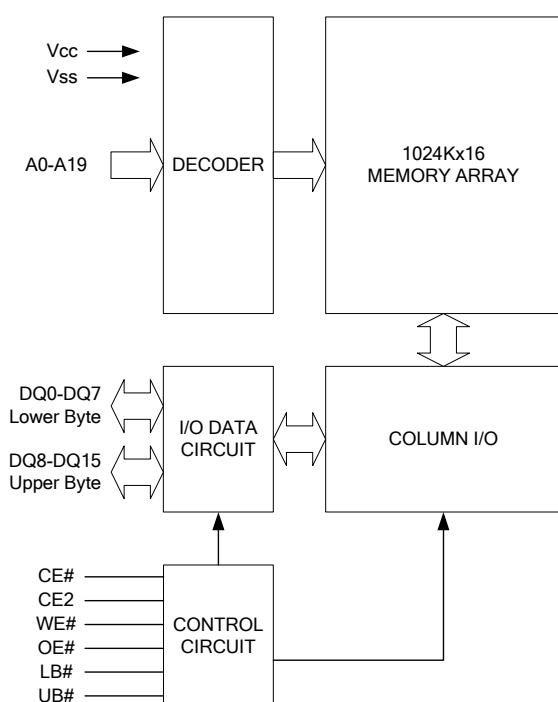
The AS6C1616 is a 16,777,216-bit low power CMOS static random access memory organized as 1,048,576 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1616 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C1616 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

**PRODUCT FAMILY**

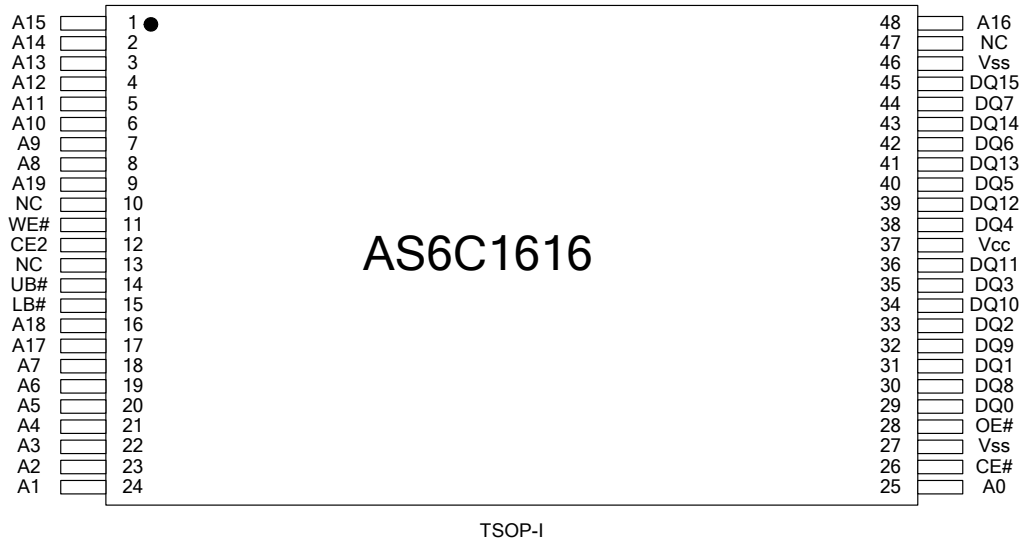
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> , TYP.)	Operating(I <sub>CC</sub> , TYP.)
AS6C1616(I)	-40 ~ 85°C	2.7 ~ 3.6V	55ns	10μA (LL)/4μA(SL)	45/30mA

**FUNCTIONAL BLOCK DIAGRAM****PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground



## 1024K X 16 BIT LOW POWER CMOS SRAM

**PIN CONFIGURATION****ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85(I grade)	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



## 1024K X 16 BIT LOW POWER CMOS SRAM

**TRUTH TABLE**

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High - Z	High - Z	$I_{SB}, I_{SB1}$
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	$I_{CC}, I_{CC1}$
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	$D_{OUT}$	High - Z	$I_{CC}, I_{CC1}$
	L	H	L	H	H	L	High - Z	$D_{OUT}$	
	L	H	L	H	L	L	$D_{OUT}$	$D_{OUT}$	
Write	L	H	X	L	L	H	$D_{IN}$	High - Z	$I_{CC}, I_{CC1}$
	L	H	X	L	H	L	High - Z	$D_{IN}$	
	L	H	X	L	L	L	$D_{IN}$	$D_{IN}$	

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. <sup>*4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>			2.7	3.0	3.6	V	
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>			2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>			- 0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>		- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled		- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA		2.2	2.7	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	- 55	-	45	60	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE#≤0.2V and CE2≥V <sub>CC</sub> -0.2V I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V		-	8	16	mA	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> Other pins at V <sub>IL</sub> or V <sub>IH</sub>		-	0.3	2	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2≤0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	LLI		-	10	100	μA
			SLI <sup>*5</sup>	25℃	-	4	6	μA
				40℃	-	4	6	μA
			SLI		-	4	40	μA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$  for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$  for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.



## 1024K X 16 BIT LOW POWER CMOS SRAM

4. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at  $V_{CC} = V_{CC}(TYP.)$  and  $T = 25^{\circ}C$

5. This parameter is measured at  $V = 3.0V$

**CAPACITANCE** ( $T_A = 25^{\circ}C$ ,  $f = 1.0MHz$ )

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	$C_{IN}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$ , $I_{OH}/I_{OL} = -1mA/2mA$

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	AS6C1616-55		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	55	-	ns
Address Access Time	$t_{AA}$	-	55	ns
Chip Enable Access Time	$t_{ACE}$	-	55	ns
Output Enable Access Time	$t_{OE}$	-	30	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	20	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	20	ns
Output Hold from Address Change	$t_{OH}$	10	-	ns
LB#, UB# Access Time	$t_{BA}$	-	55	ns
LB#, UB# to High-Z Output	$t_{BHZ}^*$	-	25	ns
LB#, UB# to Low-Z Output	$t_{BLZ}^*$	10	-	ns

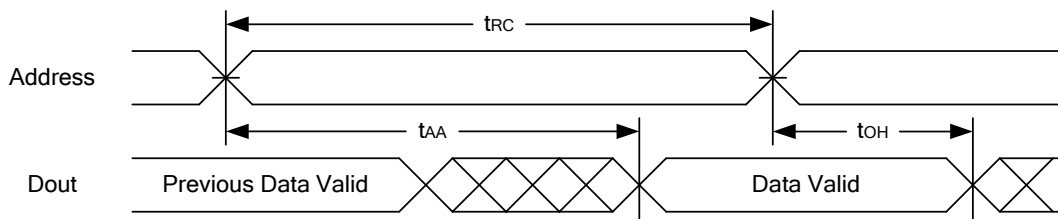
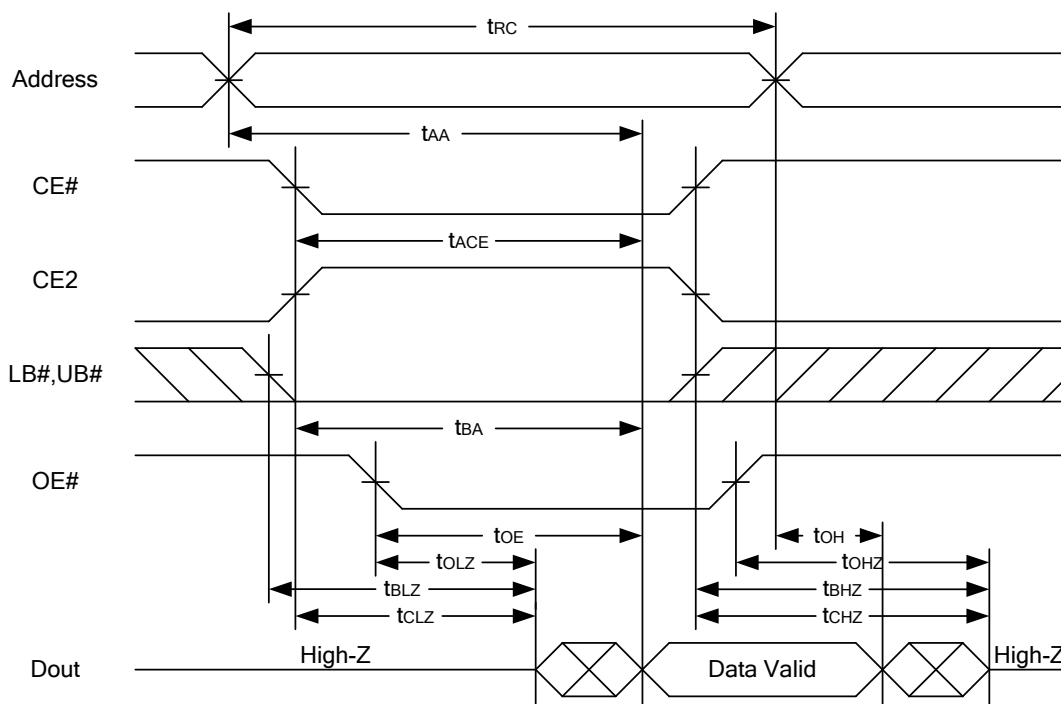
**(2) WRITE CYCLE**

PARAMETER	SYM.	AS6C1616-55		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	55	-	ns
Address Valid to End of Write	$t_{AW}$	50	-	ns
Chip Enable to End of Write	$t_{CW}$	50	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	45	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	25	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	20	ns
LB#, UB# Valid to End of Write	$t_{BW}$	45	-	ns

\*These parameters are guaranteed by device characterization, but not production tested.



## 1024K X 16 BIT LOW POWER CMOS SRAM

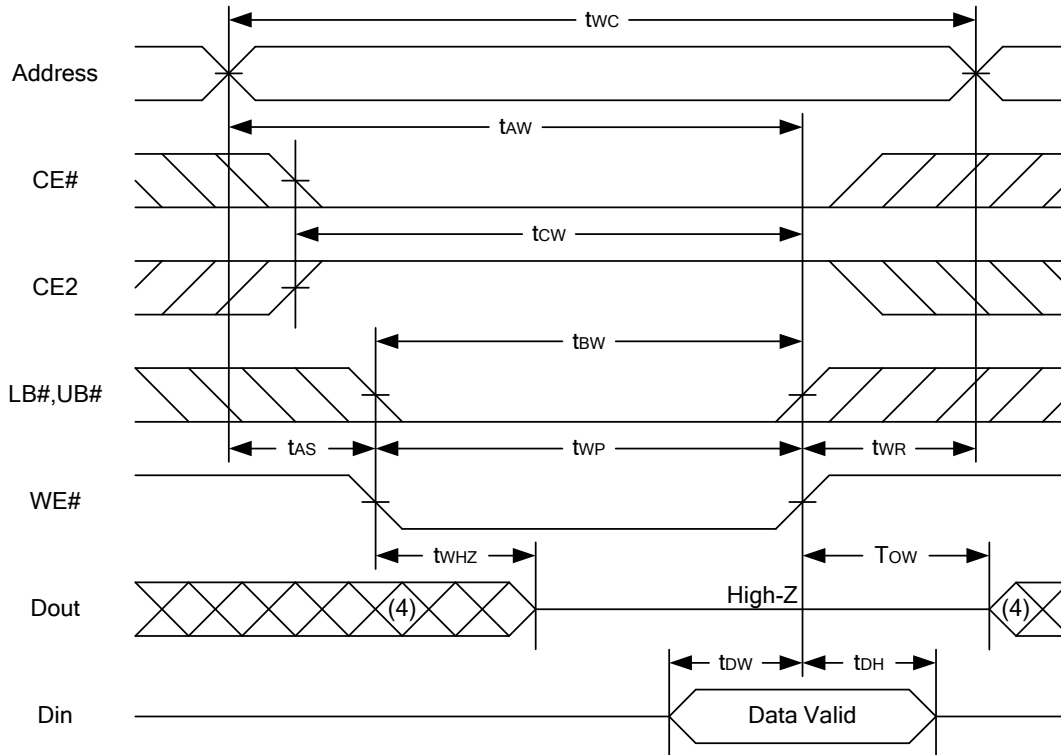
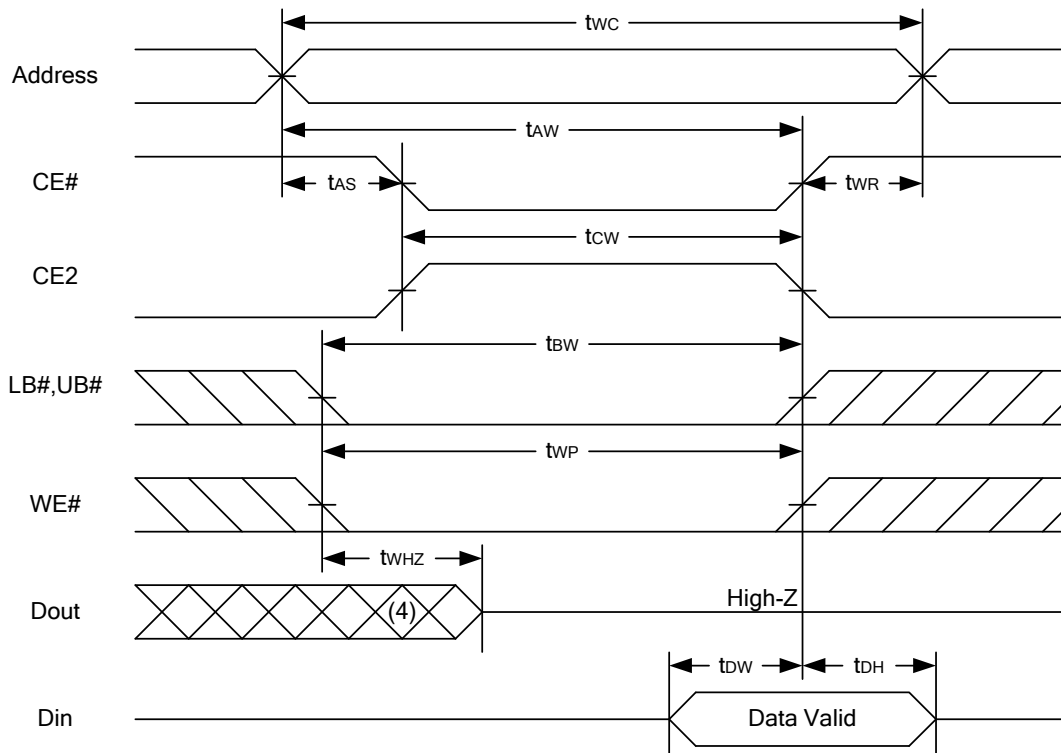
**TIMING WAVEFORMS****READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)**

## Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
4. tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.

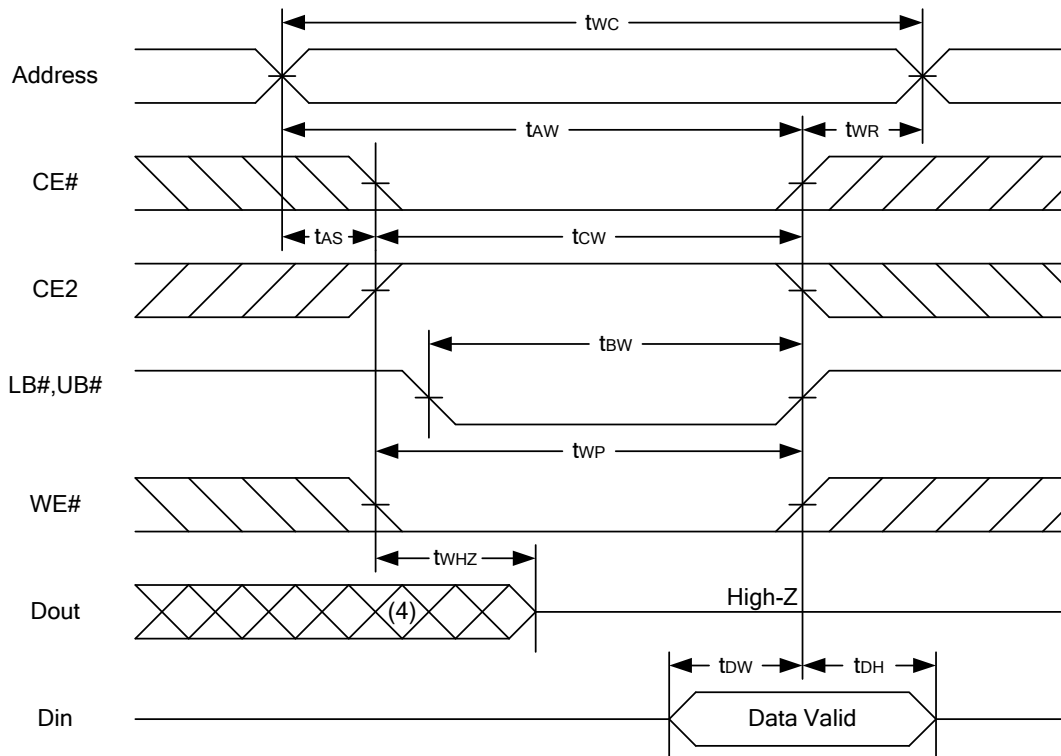


## 1024K X 16 BIT LOW POWER CMOS SRAM

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)****WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)**



## 1024K X 16 BIT LOW POWER CMOS SRAM

**WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)**

## Notes :

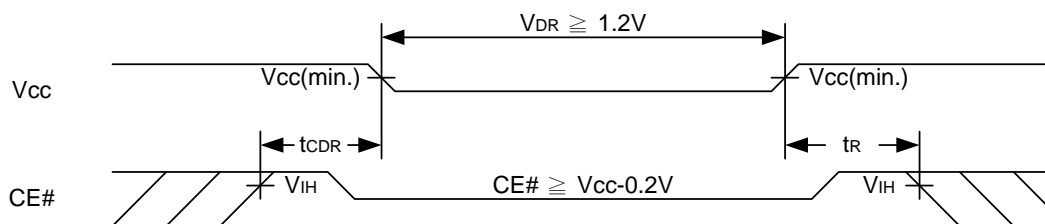
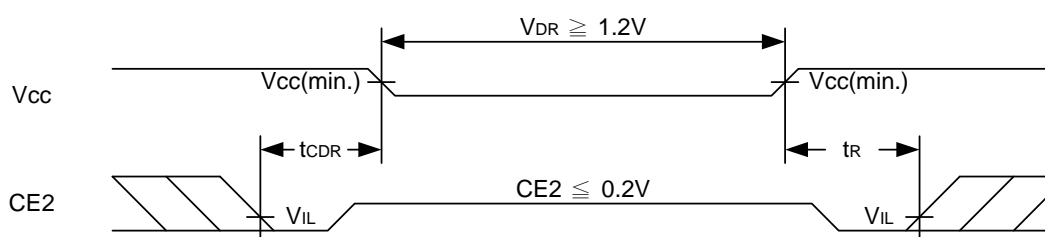
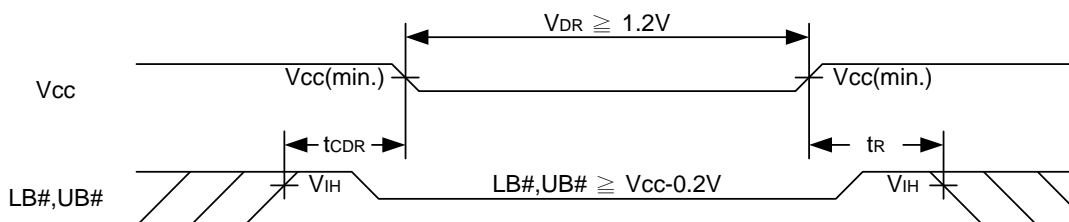
1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured  $\pm 500\text{mV}$  from steady state.



## 1024K X 16 BIT LOW POWER CMOS SRAM

**DATA RETENTION CHARACTERISTICS**

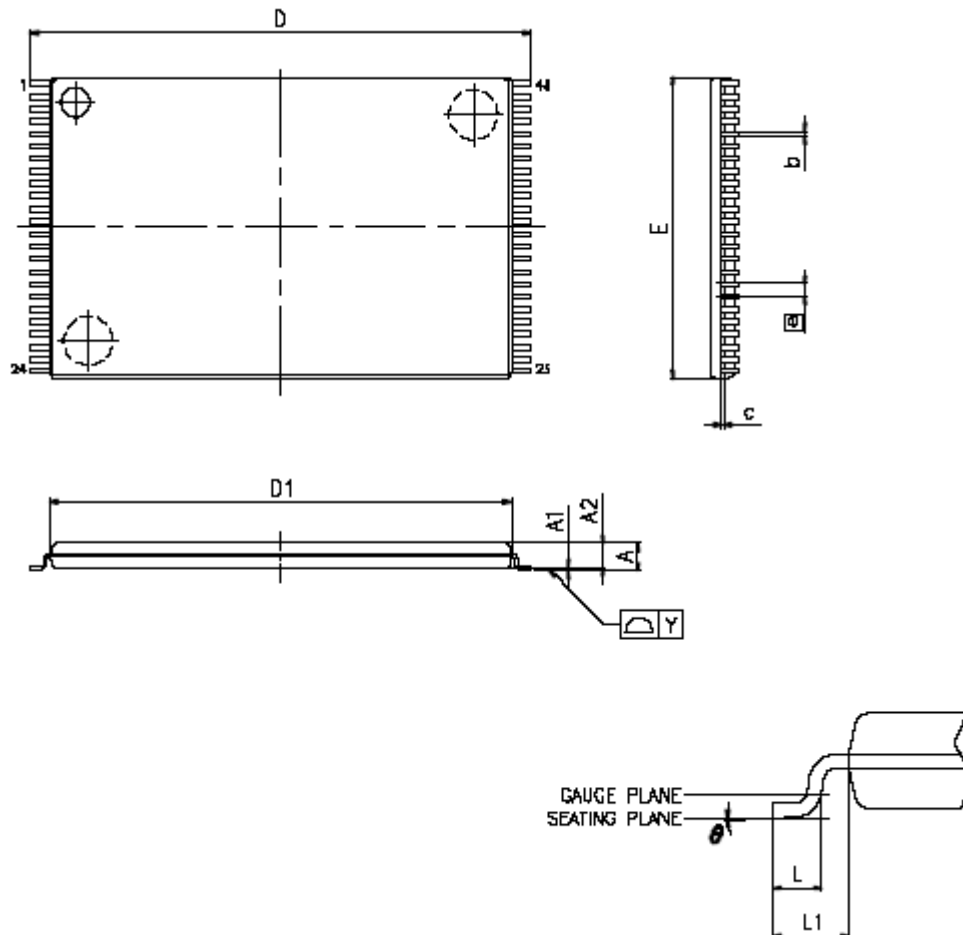
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
VCC for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V		1.2	-	3.6	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.2V CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V other pins at 0.2V or V <sub>CC</sub> -0.2V	LLI		-	4	80	μA
			SLI	25°C	-	2.5	5	μA
				40°C	-	2.5	5	μA
			SLI		-	2.5	40	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)		0	-	-	ns	
Recovery Time	t <sub>R</sub>			t <sub>RC</sub> *	-	-	ns	

t<sub>RC</sub>\* = Read Cycle Time**DATA RETENTION WAVEFORM****Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)****Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)****Low V<sub>CC</sub> Data Retention Waveform (3) (LB#, UB# controlled)**





## 1024K X 16 BIT LOW POWER CMOS SRAM

**PACKAGE OUTLINE DIMENSION****48-pin 12mm x 20mm TSOP-I Package Outline Dimension**

## VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

	SYMBOLS	MIN.	NOM.	MAX
	A	—	—	1.20
	A1	0.05	—	0.15
	A2	0.95	1.00	1.05
	b	0.17	0.22	0.27
	c	0.10	—	0.21
⚠	D	19.80	20.00	20.20
⚠	D1	18.30	18.40	18.50
⚠	E	11.90	12.00	12.10
		0.50 BASIC		
	L	0.50	0.60	0.70
⚠	L1	—	0.80	—
⚠	Y	—	—	0.10
⚠	θ	0°	—	5°

## NOTES:

1. JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



## 1024K X 16 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C1616-55TIN	1024K x 16	2.7 - 3.6V	48pin TSOP-I	Industrial ~ -40 F - 85 F	55

**PART NUMBERING SYSTEM**

AS6C	1616	-55	X	X	N
low power SRAM prefix	Device Number 16 =16M 16 =x16	Access Time	Package Option 48pin TSOP-I	Temperature Range I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part

1024K X 16 BIT LOW POWER CMOS SRAM

---



Alliance Memory, Inc  
551 Taylor Way, Suite 1  
San Carlos, CA 94070, USA  
Phone: 650-610-6800  
Fax: 650-620-9211  
[www.alliancememory.com](http://www.alliancememory.com)

Copyright © Alliance Memory  
All Rights Reserved

© Copyright 2010 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at anytime, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.