FAIRCHILD
SEMICONDUCTOR TM

May 1997
ADVANCE INFORMATION

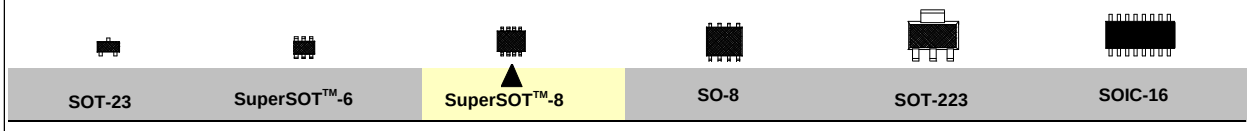
FDR4410
N-Channel Enhancement Mode Field Effect Transistor

General Description

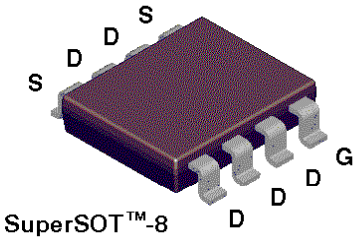
The FDR4410 has been designed as a smaller, low cost alternative to the popular Si4410DY.
The SuperSOT™-8 package is 40% smaller than the SO-8 package.
The SuperSOT-8 advanced package design and optimised pinout allow the typical Power dissipation to be similar to the bigger SO-8 packages.

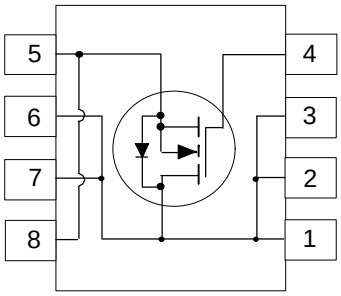
Features

- 9 A, 30 V. $R_{DS(ON)}$ = 0.013 Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ = 0.020 Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Proprietary SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16





Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter		FDR4410	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Draint Current - Continuous	(Note 1a)	9	A
	- Pulsed		27	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ Est	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSS}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSS}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_O = 250 µA	1	1.5	2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 9 A		0.0115	0.013	Ω
		V_{GS} = 4.5 V, I_D = 7.5 A		0.018	0.02	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	27			A
SWITCHING CHARACTERISTICS (Note 2)						
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 9 A, V_{GS} = 10 V		38	55	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

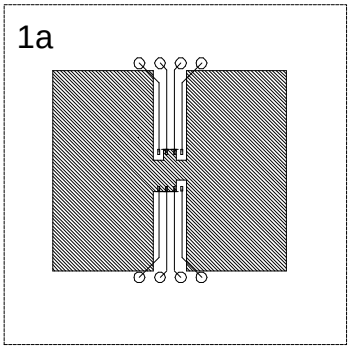
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

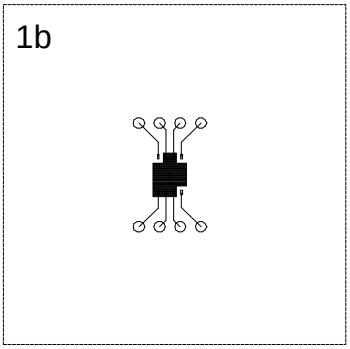
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

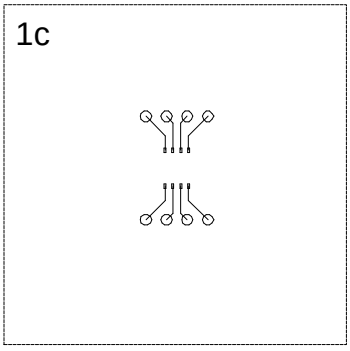
a. 70°C/W when mounted on a 1 in^2 pad of 2oz cpper.

b. 125°C/W when mounted on a 0.026 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%