

110MHz, High Slew Rate, High Output Current Buffer

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Intersil D.I. technologies, the HA-5002 current buffer offers 1300V/ μ s slew rate with 110MHz of bandwidth. The ± 200 mA output current capability is enhanced by a 3Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000k Ω input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

For the military grade product, refer to the HA-5002/883 datasheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA3-5002-5	0 to 75	8 Ld PDIP	E8.3
HA3-5002-5Z (Note)	0 to 75	8 Ld PDIP* (Pb-free)	E8.3
HA4P5002-5	0 to 75	20 Ld PLCC	N20.35
HA9P5002-5 (50025)	0 to 75	8 Ld SOIC	M8.15
HA9P5002-5Z (50025Z) (Note)	0 to 75	8 Ld SOIC (Pb-free)	M8.15
HA9P5002-9 (50029)	-40 to 85	8 Ld SOIC	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

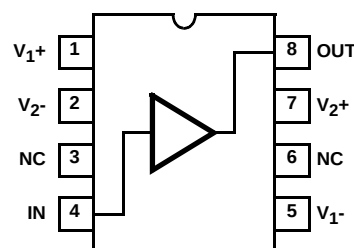
- Voltage Gain 0.995
- High Input Impedance 3000k Ω
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/ μ s
- Very Wide Bandwidth 110MHz
- High Output Current ± 200 mA
- Pulsed Output Current 400mA
- Monolithic Construction
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

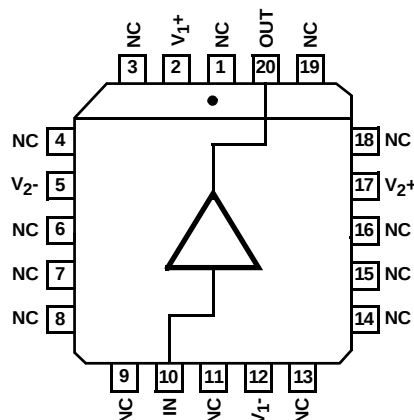
- Line Driver
- Data Acquisition
- 110MHz Buffer
- Radara Cable Driver
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Video Products

Pinouts

HA-5002 (PDIP, SOIC)
TOP VIEW



HA-5002 (PLCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
 Input Voltage V₁+ to V₁-
 Output Current (Continuous) ±200mA
 Output Current (50ms On, 1s Off) ±400mA

Operating Conditions

Temperature Range
 HA-5002-5 0°C to 75°C
 HA-5002-9 -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PDIP Package*. 92 N/A
 PLCC Package. 74 N/A
 SOIC Package 157 N/A

Max Junction Temperature (Hermetic Packages, Note 1) 175°C
 Max Junction Temperature (Plastic Packages, Note 1) 150°C
 Max Storage Temperature Range -65°C to 150°C
 Max Lead Temperature (Soldering 10s) 300°C
 (PLCC and SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the can packages, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 12V$ to $\pm 15V$, $R_S = 50\Omega$, $R_L = 1k\Omega$, $C_L = 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	5	20	mV
		Full	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	μV/°C
Bias Current		25	-	2	7	μA
		Full	-	2.4	10	μA
Input Resistance		Full	1.5	3	-	MΩ
Input Noise Voltage	10Hz-1MHz	25	-	18	-	μV _{P-P}
TRANSFER CHARACTERISTICS						
Voltage Gain, ($V_{OUT} = \pm 10V$)	$R_L = 50\Omega$	25	-	0.900	-	V/V
	$R_L = 100\Omega$	25	-	0.971	-	V/V
	$R_L = 1k\Omega$	25	-	0.995	-	V/V
	$R_L = 1k\Omega$	Full	0.980	-	-	V/V
-3dB Bandwidth	$V_{IN} = 1V_{P-P}$	25	-	110	-	MHz
AC Current Gain		25	-	40	-	A/mA
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 100\Omega$	25	±10	±11.2	-	V
	$R_L = 1k\Omega$, $V_S = \pm 15V$	Full	±10	±13.9	-	V
	$R_L = 1k\Omega$, $V_S = \pm 12V$	Full	±10	±10.5	-	V
Output Current	$V_{IN} = \pm 10V$, $R_L = 40\Omega$	25	-	220	-	mA
Output Resistance		Full	-	3	10	Ω
Harmonic Distortion	$V_{IN} = 1V_{RMS}$, $f = 10kHz$	25	-	<0.005	-	%
TRANSIENT RESPONSE						
Full Power Bandwidth (Note 3)		25	-	20.7	-	MHz
Rise Time		25	-	3.6	-	ns
Propagation Delay		25	-	2	-	ns
Overshoot		25	-	30	-	%
Slew Rate		25	1.0	1.3	-	V/ns
Settling Time	To 0.1%	25	-	50	-	ns

Electrical Specifications $V_{\text{SUPPLY}} = \pm 12\text{V}$ to $\pm 15\text{V}$, $R_S = 50\Omega$, $R_L = 1\text{k}\Omega$, $C_L = 10\text{pF}$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Differential Gain	$R_L = 500\Omega$	25	-	0.06	-	%
Differential Phase	$R_L = 500\Omega$	25	-	0.22	-	Degrees
POWER REQUIREMENTS						
Supply Current		25	-	8.3	-	mA
		Full	-	-	10	mA
Power Supply Rejection Ratio	$A_V = 10\text{V}$	Full	54	64	-	dB

NOTE:

3. $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_{\text{PEAK}}}$; $V_P = 10\text{V}$

Test Circuit and Waveforms

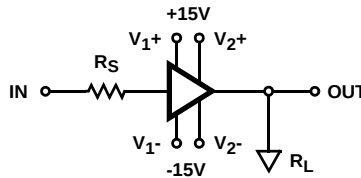
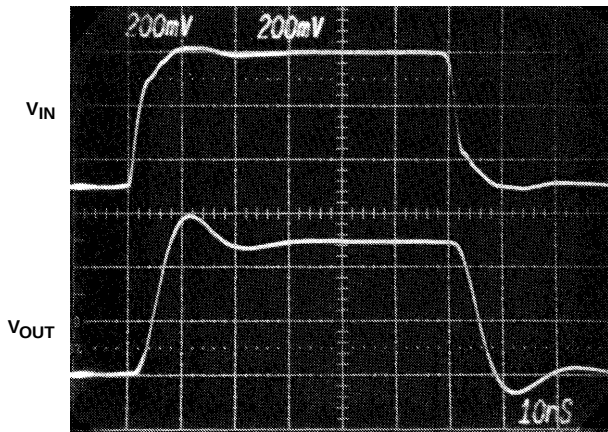
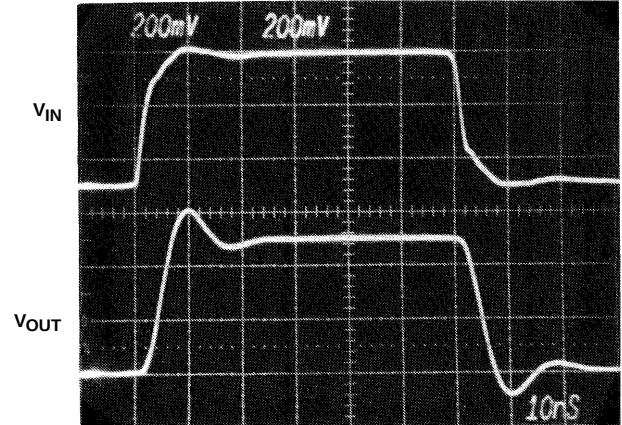


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE



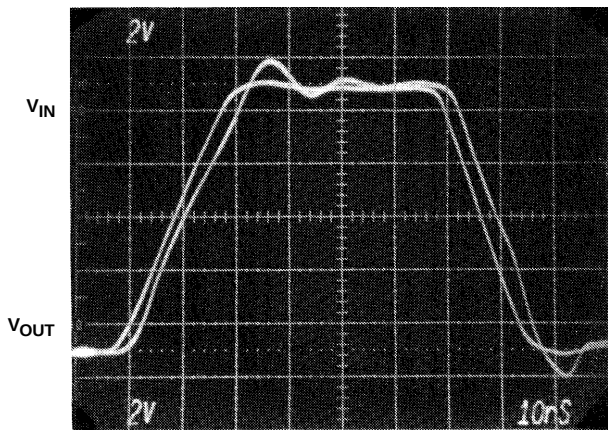
$R_S = 50\Omega$, $R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



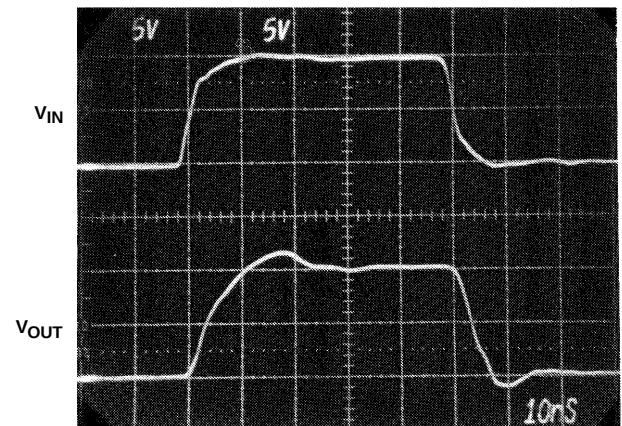
$R_S = 50\Omega$, $R_L = 1\text{k}\Omega$

SMALL SIGNAL WAVEFORMS



$R_S = 50\Omega$, $R_L = 100\Omega$

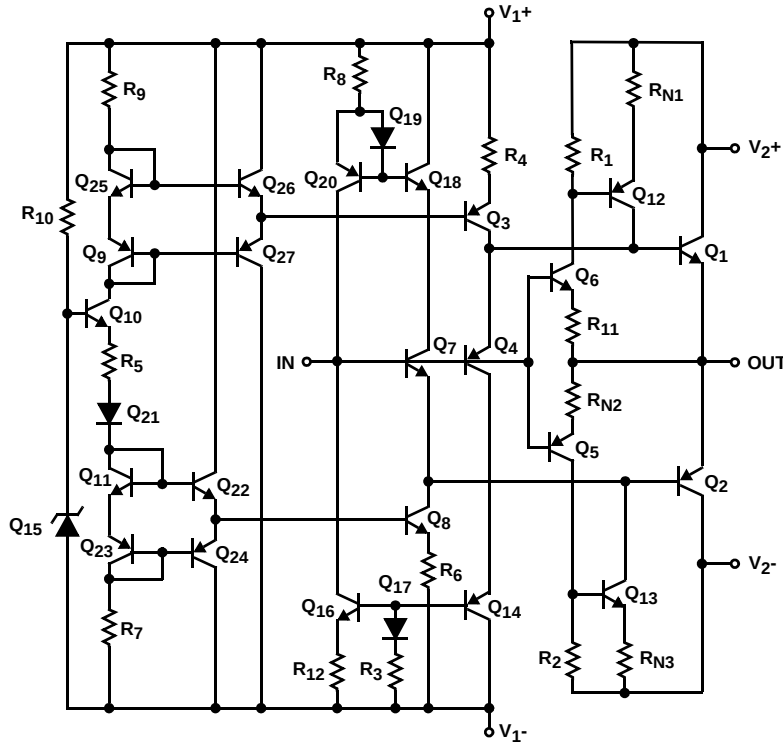
LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$, $R_L = 1\text{k}\Omega$

LARGE SIGNAL WAVEFORMS

Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

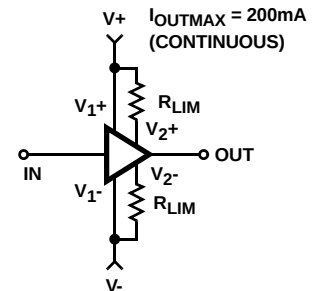
Operation at Reduced Supply Levels

The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

The output current can be limited by using the following circuit:

$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = Cdv/dt$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1kΩ; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

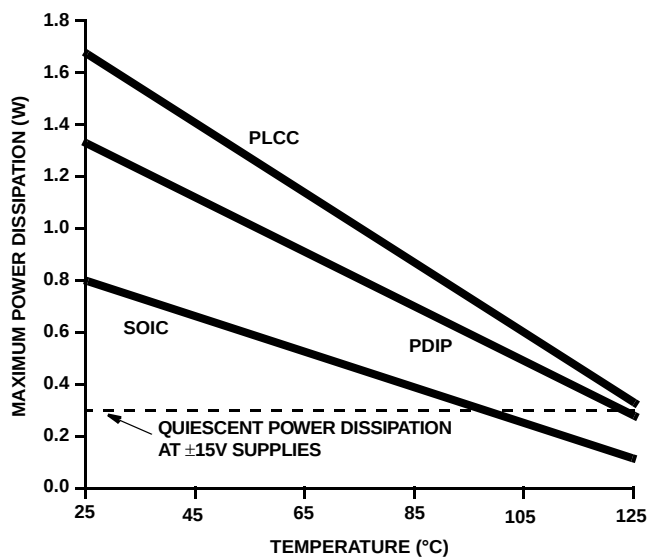


FIGURE 2. MAXIMUM POWER DISSIPATION vs TEMPERATURE

$$P_{D\text{MAX}} = \frac{T_{J\text{MAX}} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where: $T_{J\text{MAX}}$ = Maximum Junction Temperature of the Device

T_A = Ambient

θ_{JC} = Junction to Case Thermal Resistance

θ_{CS} = Case to Heat Sink Thermal Resistance

θ_{SA} = Heat Sink to Ambient Thermal Resistance

Graph is based on: $P_{D\text{MAX}} = \frac{T_{J\text{MAX}} - T_A}{\theta_{JA}}$

Typical Application

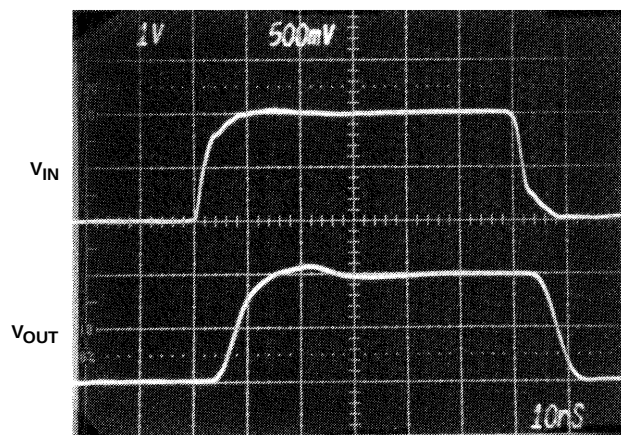
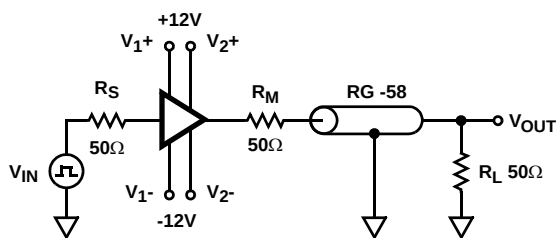
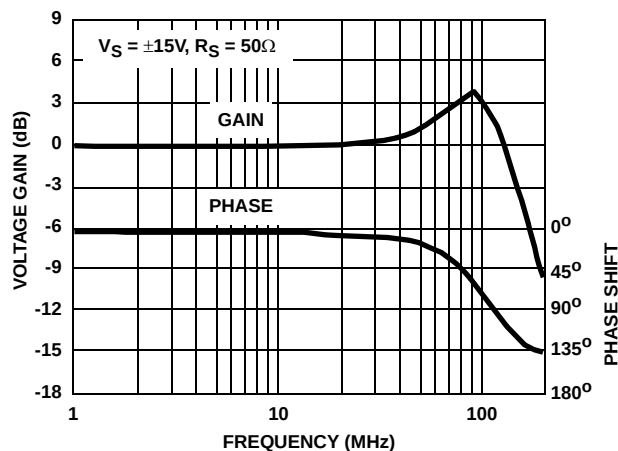
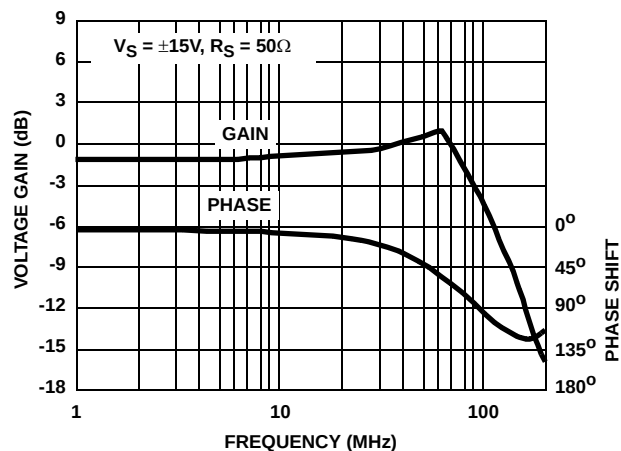


FIGURE 3. COAXIAL CABLE DRIVER - 50Ω SYSTEM

Typical Performance Curves

FIGURE 4. GAIN/PHASE vs FREQUENCY ($R_L = 1k\Omega$)FIGURE 5. GAIN/PHASE vs FREQUENCY ($R_L = 50\Omega$)

Typical Performance Curves (Continued)

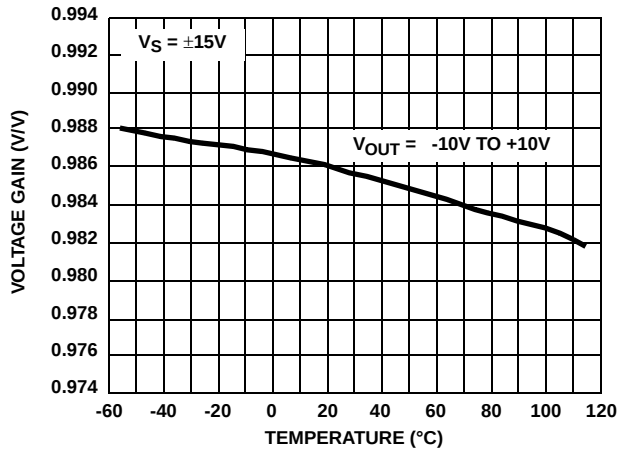
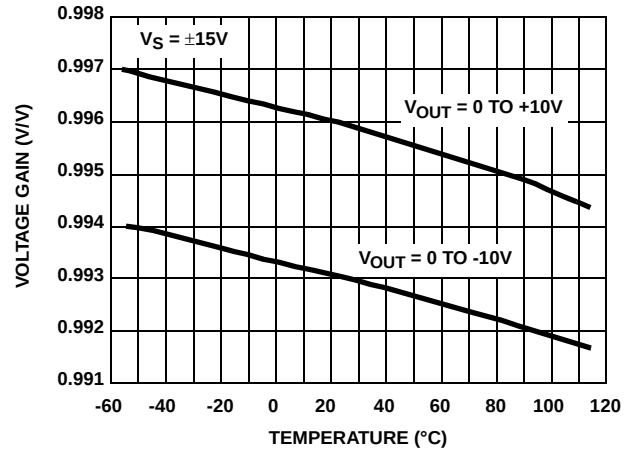
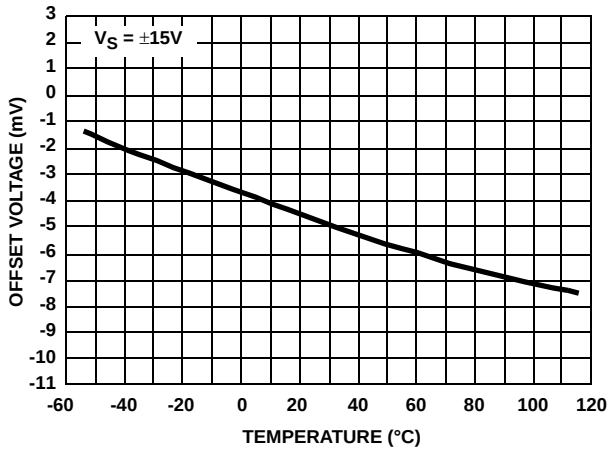
FIGURE 6. VOLTAGE GAIN vs TEMPERATURE ($R_L = 100\Omega$)FIGURE 7. VOLTAGE GAIN vs TEMPERATURE ($R_L = 1k\Omega$)

FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE

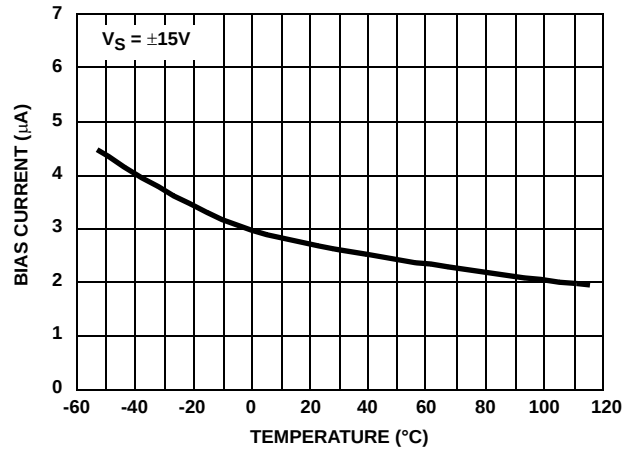


FIGURE 9. BIAS CURRENT vs TEMPERATURE

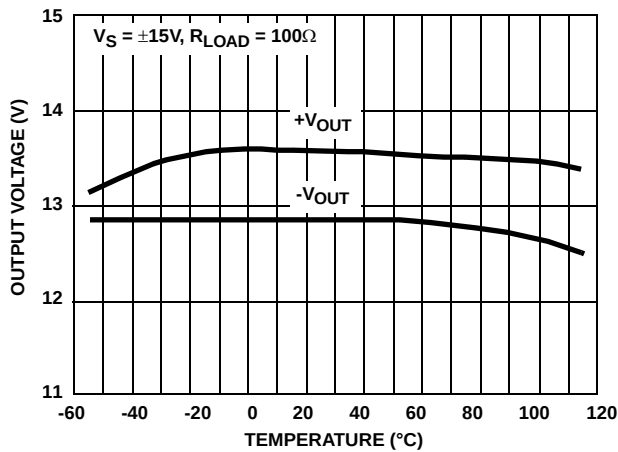


FIGURE 10. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

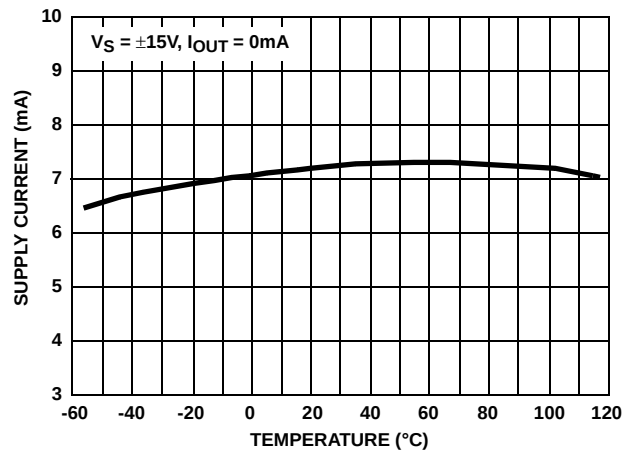


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

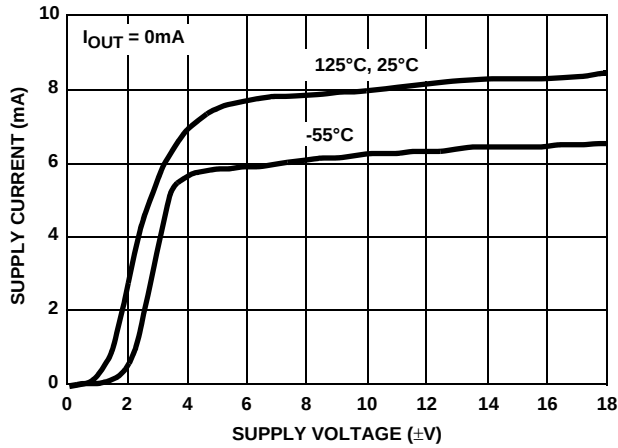


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

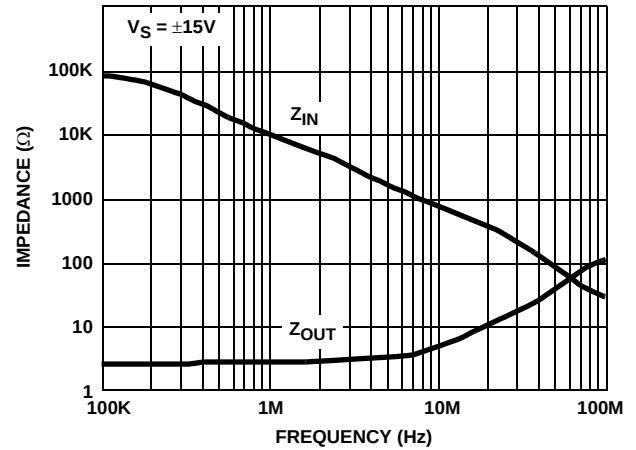


FIGURE 13. INPUT/OUTPUT IMPEDANCE vs FREQUENCY

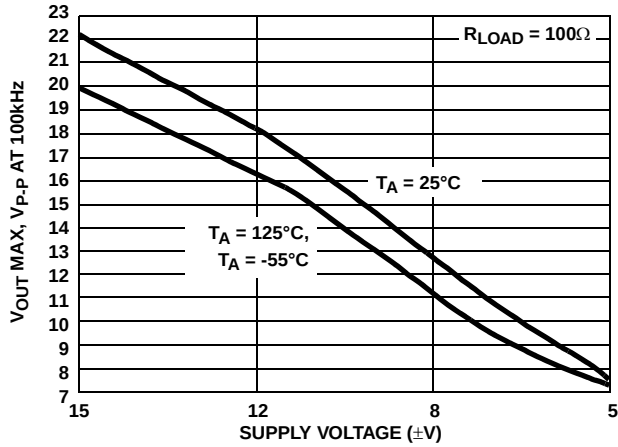
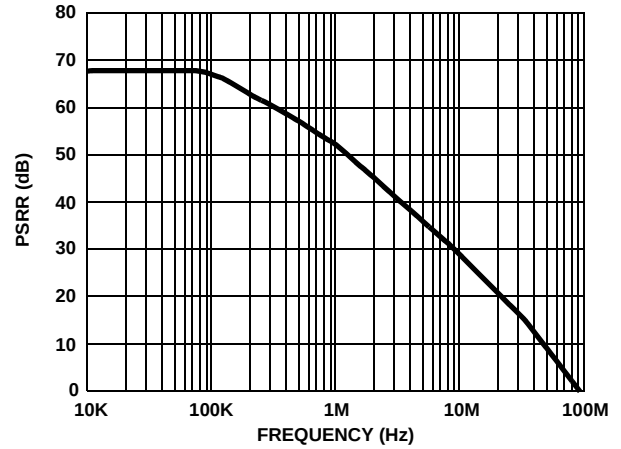
FIGURE 14. V_{OUT} MAXIMUM vs V_{SUPPLY} 

FIGURE 15. PSRR vs FREQUENCY

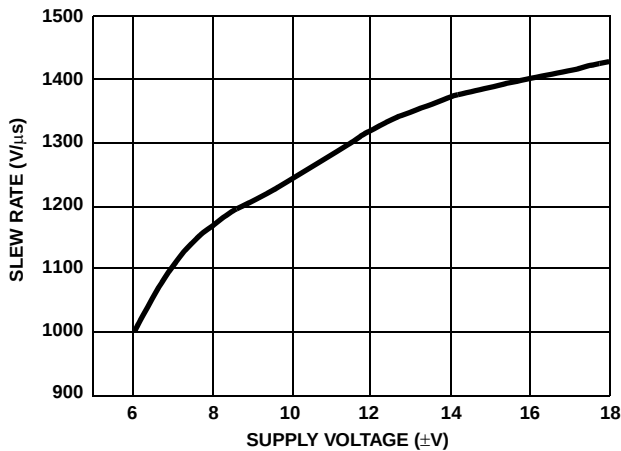


FIGURE 16. SLEW RATE vs SUPPLY VOLTAGE

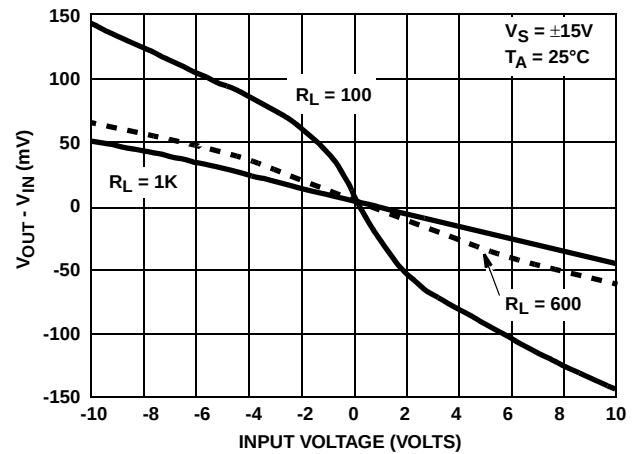


FIGURE 17. GAIN ERROR vs INPUT VOLTAGE

Die Characteristics

DIE DIMENSIONS:

81 mils x 80 mils x 19 mils
2050 μ m x 2030 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 20k $\text{\AA}$ $\pm$ 2k $\text{\AA}$

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2 , 5% Phos.)
Silox Thickness: 12k $\text{\AA}$ $\pm$ 2k $\text{\AA}$
Nitride Thickness: 3.5k $\text{\AA}$ $\pm$ 1.5k $\text{\AA}$

SUBSTRATE POTENTIAL (POWERED UP):

V_1^-

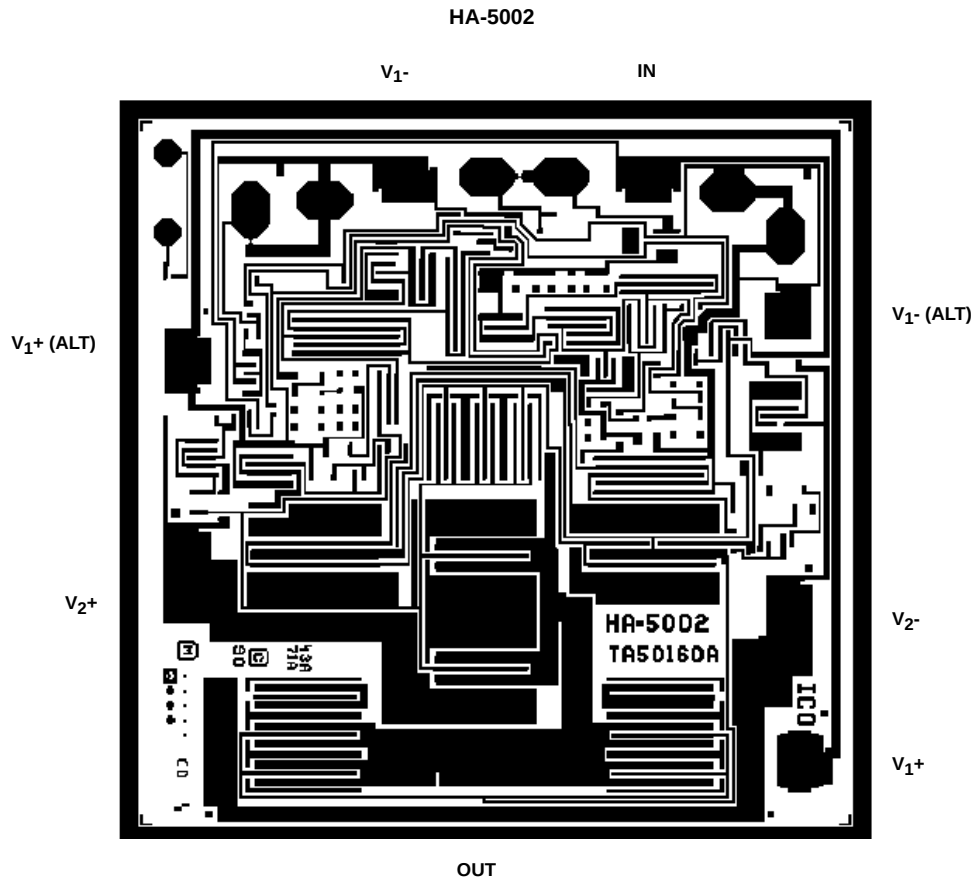
TRANSISTOR COUNT:

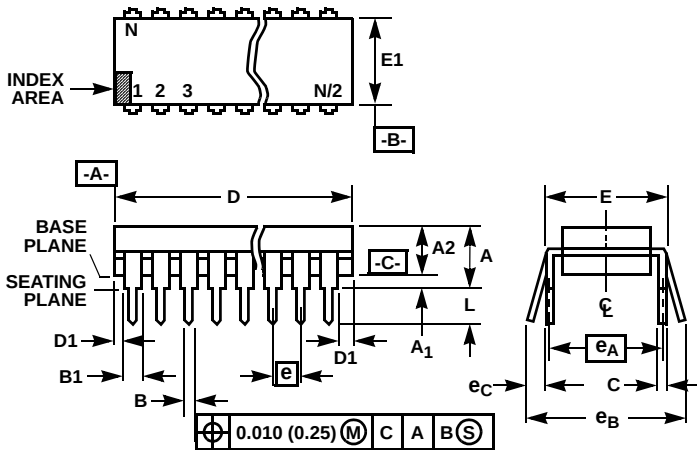
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PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)**NOTES:**

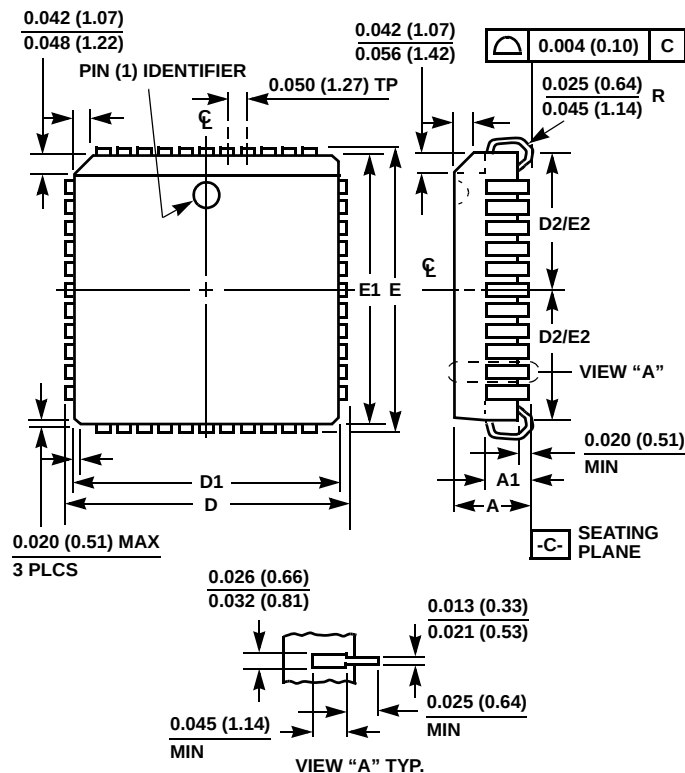
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and eA are measured with the leads constrained to be perpendicular to datum -C-.
7. eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		6
eB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A) 20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

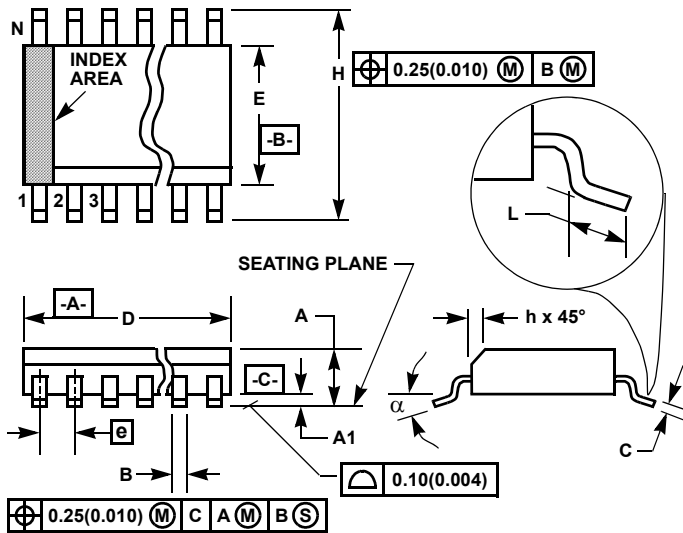
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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