IS61SP12832
IS61SP12836

128K x 32, 128K x 36 SYNCHRONOUS PIPELINED STATIC RAM

FEBRUARY 2004

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA packages
- Single +3.3V, +10%, –5% power supply
- Power-down snooze mode

DESCRIPTION

The *ISSI* IS61SP12832 and IS61SP12836 are high-speed synchronous static RAM designed to provide a burstable, high-performance memory for high speed networking and communication applications. It is organized as 131,072 words by 32 bits and 36 bits, fabricated with *ISSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

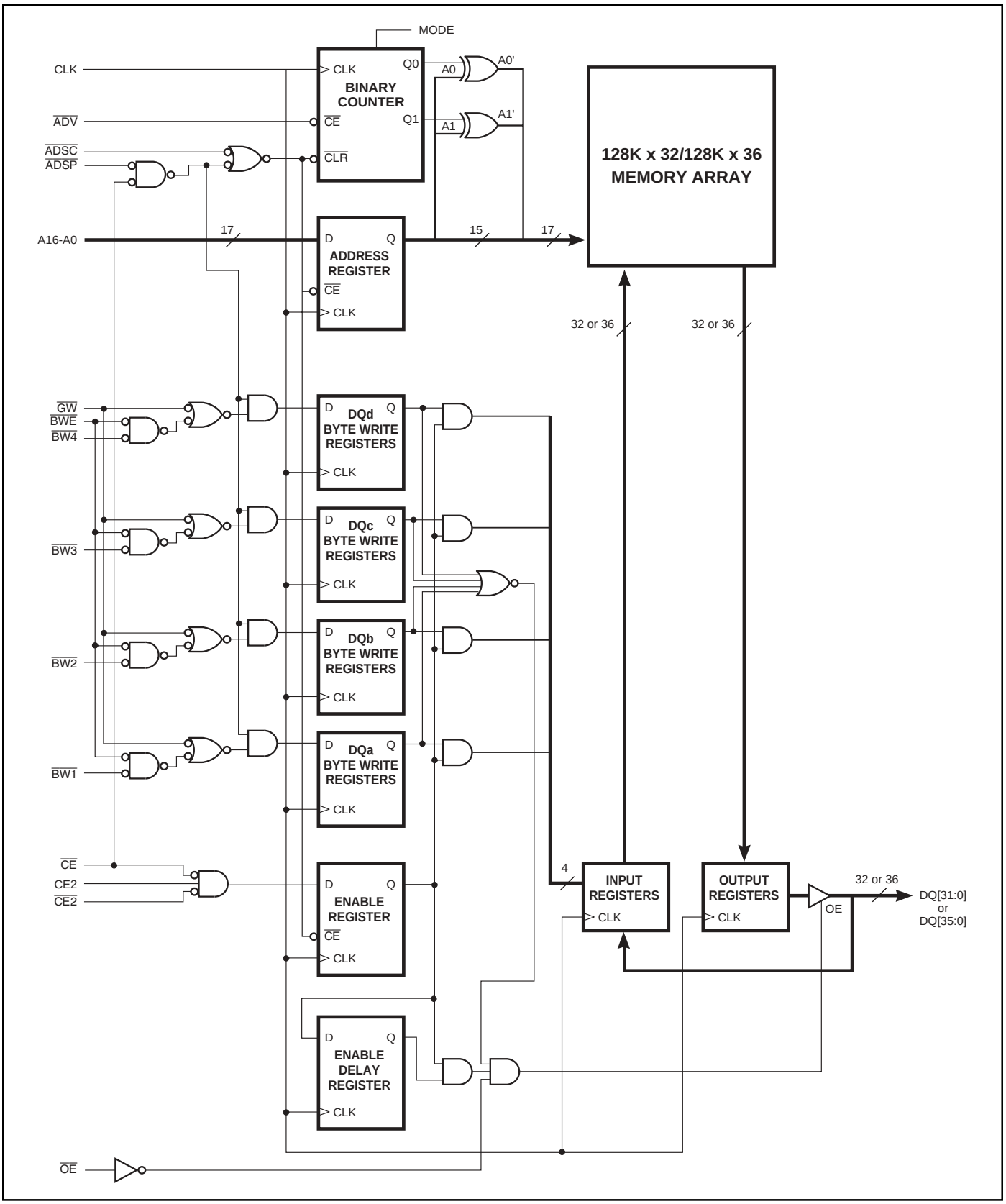
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

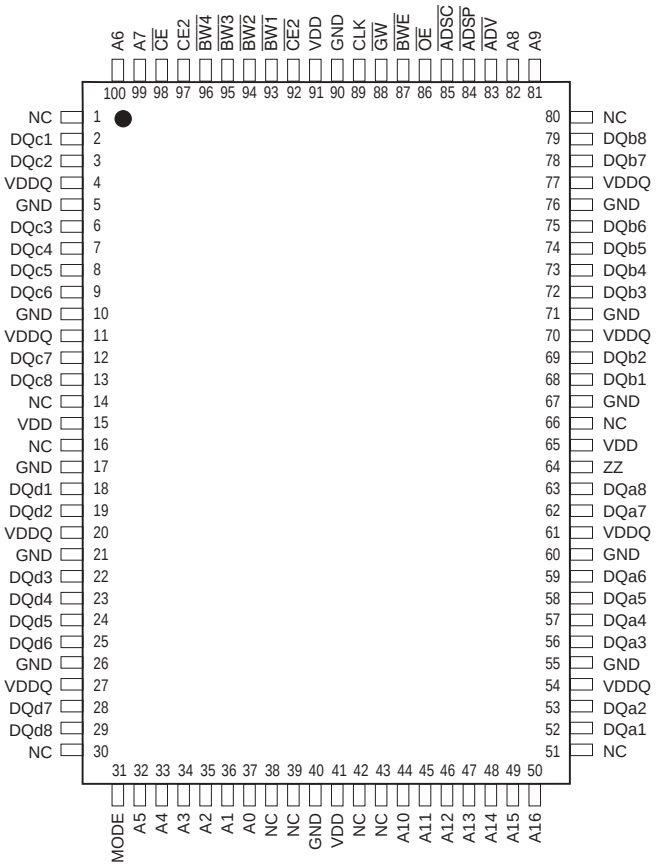
Symbol	Parameter	-166	-133	-5	Units
t_{KQ}	Clock Access Time	3.5	4	5	ns
t_{KC}	Cycle Time	6	7.5	10	ns
	Frequency	166	133	100	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin TQFP



128K x 32

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

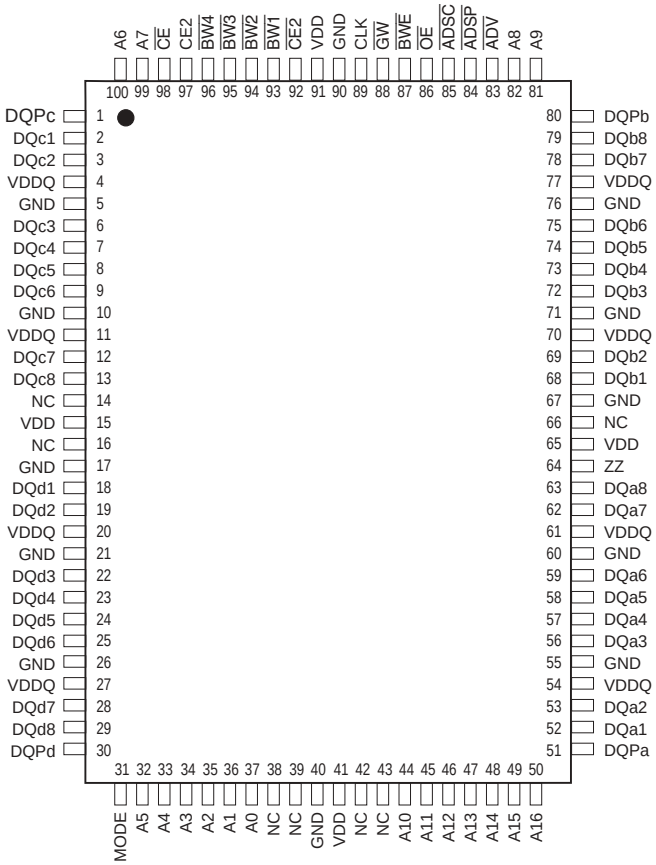
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	$\overline{ADSP}$	A8	A16	VDDQ
B	NC	CE2	A3	$\overline{ADSC}$	A9	$\overline{CE2}$	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	DQc1	DQPc	GND	NC	GND	DQPb	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VDDQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VDDQ
G	DQc5	DQc6	$\overline{BW3}$	$\overline{ADV}$	$\overline{BW2}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BW4}$	NC	$\overline{BW1}$	DQa5	DQa6
M	VDDQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VDDQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	DQPd	GND	A0	GND	DQPa	DQa1
R	NC	A5	MODE	VDD	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

100-Pin TQFP



128K x 36

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

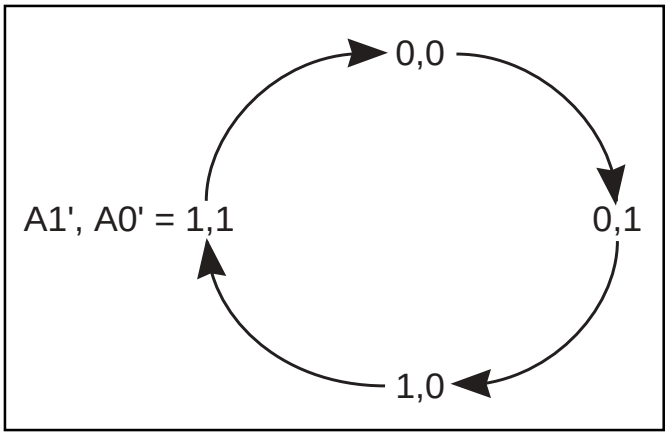
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to GND	–0.5 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V, +10%, –5%
Industrial	–40°C to +85°C	3.3V, +10%, –5%

DC ELECTRICAL CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{DDQ} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{DDQ}[2]	Com.	–2	2	µA
			Ind.	–5	5	
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{DDQ}, $\overline{OE}$ = V_{IH}	Com.	–2	2	µA
			Ind.	–5	5	

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-166 Max.	-133 Max	-5 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, V_{DD} = Max. Cycle Time ≥ t_{KC} min.	Com.	290	230	—	mA
			Ind.	300	—	220	mA
I_{SB}	Standby Current	Device Deselected, V_{DD} = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.	Com.	70	70	—	mA
			Ind.	80	—	75	mA
I_{ZZ}	Power-down Mode Current	ZZ = V_{DD} Clock Running All Inputs ≤ GND + 0.2V or ≥ V_{DD} – 0.2V	Com.	15	15	—	mA
			Ind.	20	—	20	mA

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{DD}.
2. The MODE pin should be tied to V_{DD} or GND. It exhibits ±10 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{DD} – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

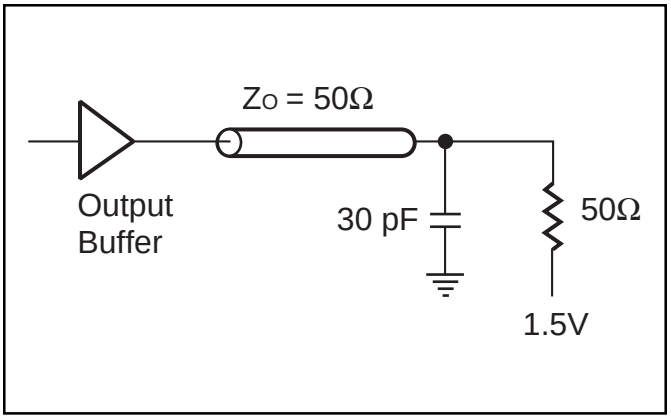


Figure 1

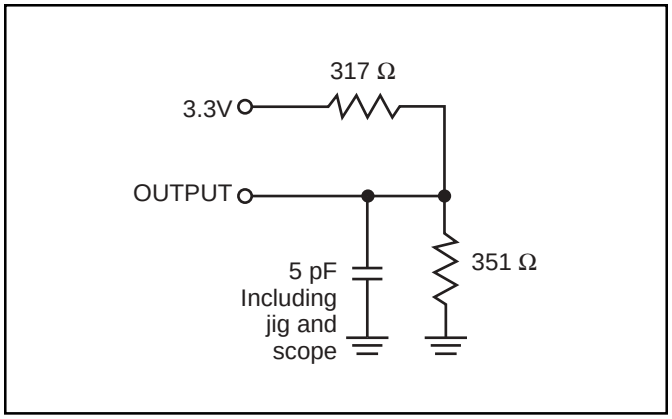


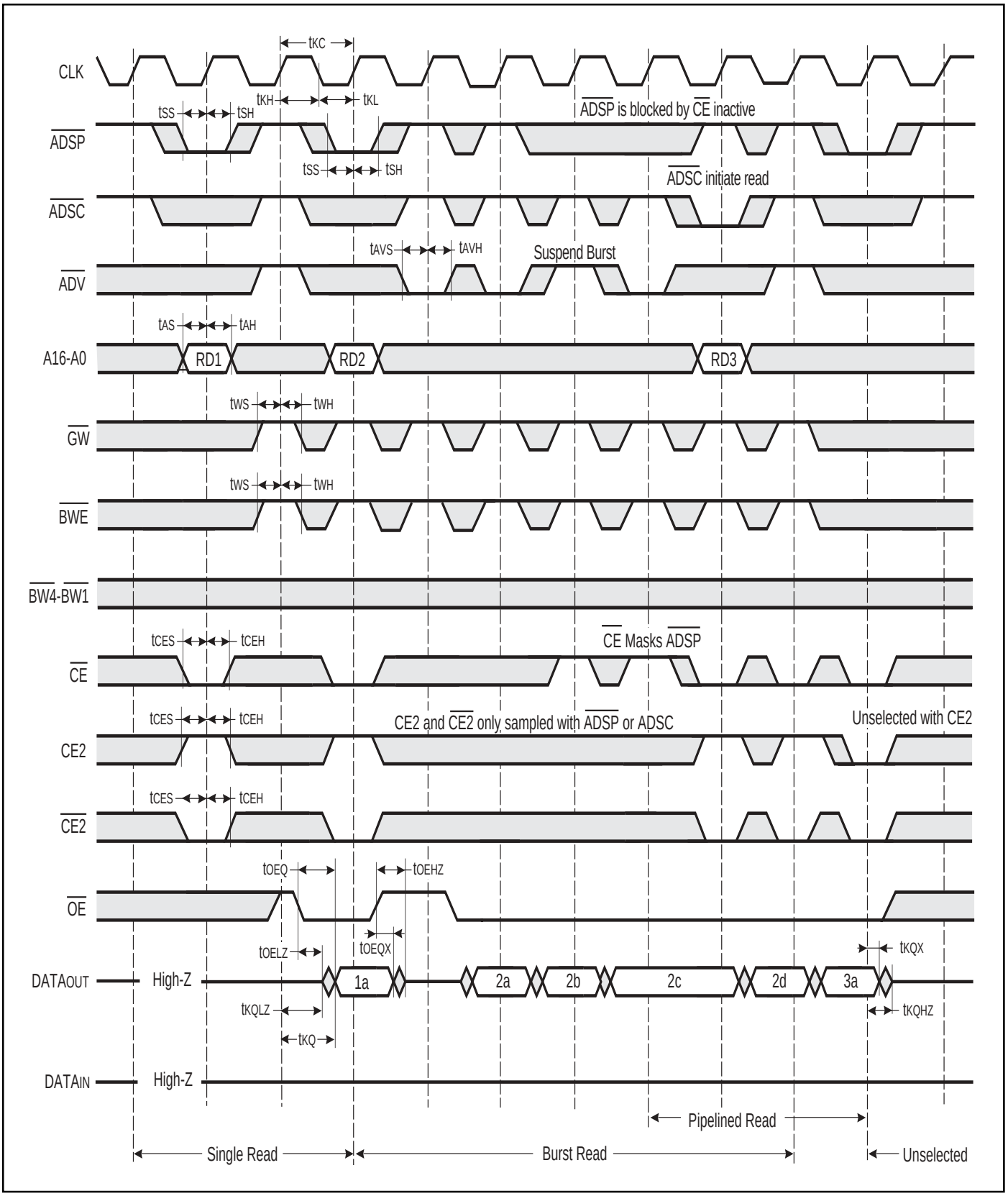
Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		-5		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{MAX}[3]	Clock Frequency	—	166	—	133	—	100	MHz
t_{KC}[3]	Cycle Time	6	—	7.5	—	10	—	ns
t_{KH}	Clock High Time	2.4	—	2.8	—	3	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.8	—	3	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	4	—	5	ns
t_{KQX}[1]	Clock High to Output Invalid	3	—	3	—	3	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.5	—	3.8	—	5	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	3.5	2	3.8	2	5	ns
t_{AS}[3]	Address Setup Time	1.5	—	1.5	—	2	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	2	—	ns
t_{WS}[3]	Write Setup Time	1.5	—	1.5	—	2	—	ns
t_{CES}[3]	Chip Enable Setup Time	1.5	—	1.5	—	2	—	ns
t_{AVS}[3]	Address Advance Setup Time	1.5	—	1.5	—	2	—	ns
t_{AH}[3]	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{SH}[3]	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{WH}[3]	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{CEH}[3]	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{AVH}[3]	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

READ/WRITE CYCLE TIMING

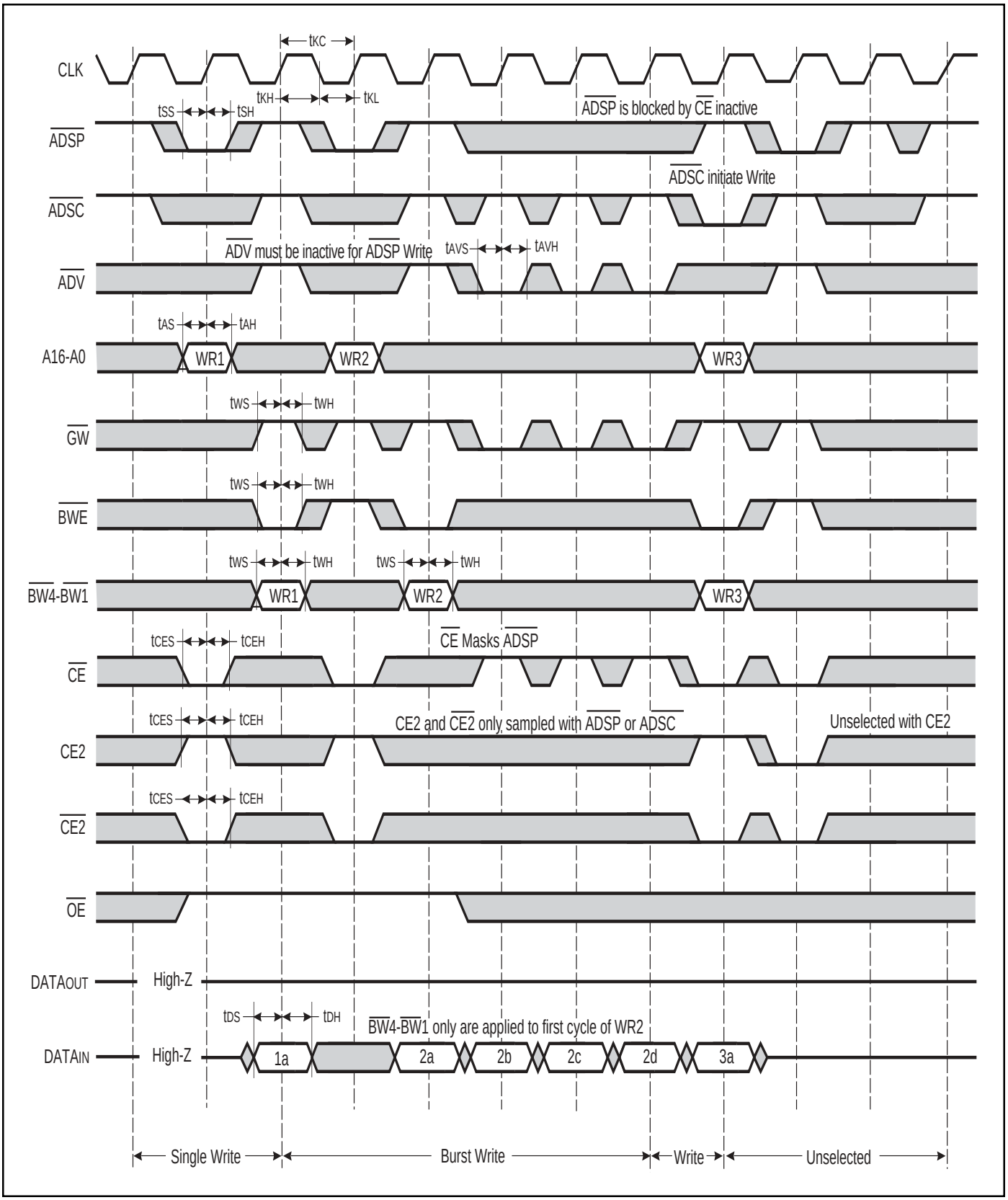


WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		-5		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{KC}(1)	Cycle Time	6	—	7.5	—	10	—	ns
t_{KH}(1)	Clock High Time	2.4	—	2.8	—	4	—	ns
t_{KL}(1)	Clock Low Time	2.4	—	2.8	—	4	—	ns
t_{AS}(1)	Address Setup Time	1.5	—	1.5	—	2	—	ns
t_{SS}(1)	Address Status Setup Time	1.5	—	1.5	—	2	—	ns
t_{WS}(1)	Write Setup Time	1.5	—	1.5	—	2	—	ns
t_{DS}(1)	Data In Setup Time	1.5	—	1.5	—	2	—	ns
t_{CES}(1)	Chip Enable Setup Time	1.5	—	1.5	—	2	—	ns
t_{AVS}(1)	Address Advance Setup Time	1.5	—	1.5	—	2	—	ns
t_{AH}(1)	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{SH}(1)	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{DH}(1)	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{WH}(1)	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{CEH}(1)	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{AVH}(1)	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns

Note:
1. Tested with load in Figure 1.

WRITE CYCLE TIMING

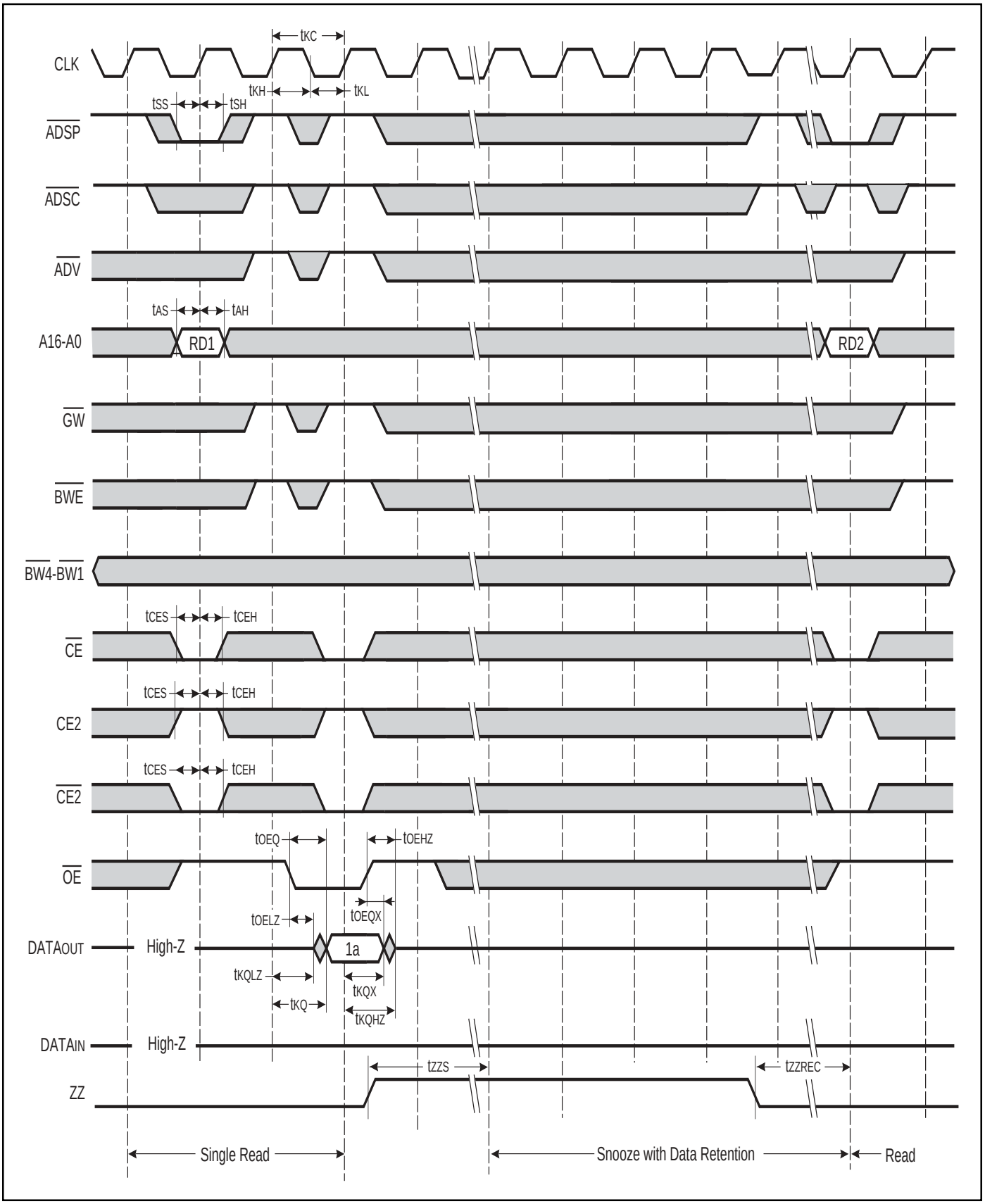


SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		-5		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{KC}[3]	Cycle Time	6	—	7.5	—	10	—	ns
t_{KH}[3]	Clock High Time	2.4	—	2.8	—	4	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.8	—	4	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	4	—	5	ns
t_{KQX}[1]	Clock High to Output Invalid	1.5	—	1.5	—	2.5	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.5	—	3.9	—	5	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	3.5	2	3.8	2	5	ns
t_{AS}[3]	Address Setup Time	1.5	—	1.5	—	2	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	2	—	ns
t_{CES}[3]	Chip Enable Setup Time	1.5	—	1.5	—	2	—	ns
t_{AH}[3]	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{SH}[3]	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{CEH}[3]	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{ZZS}	ZZ Standby	2	—	2	—	2	—	cyc
t_{ZZREC}	ZZ Recovery	2	—	2	—	2	—	cyc

Notes:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
133 MHz	IS61SP12832-133TQ	TQFP

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
166 MHz	IS61SP12832-166TQI	TQFP
5 ns	IS61SP12832-5TQI	TQFP

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

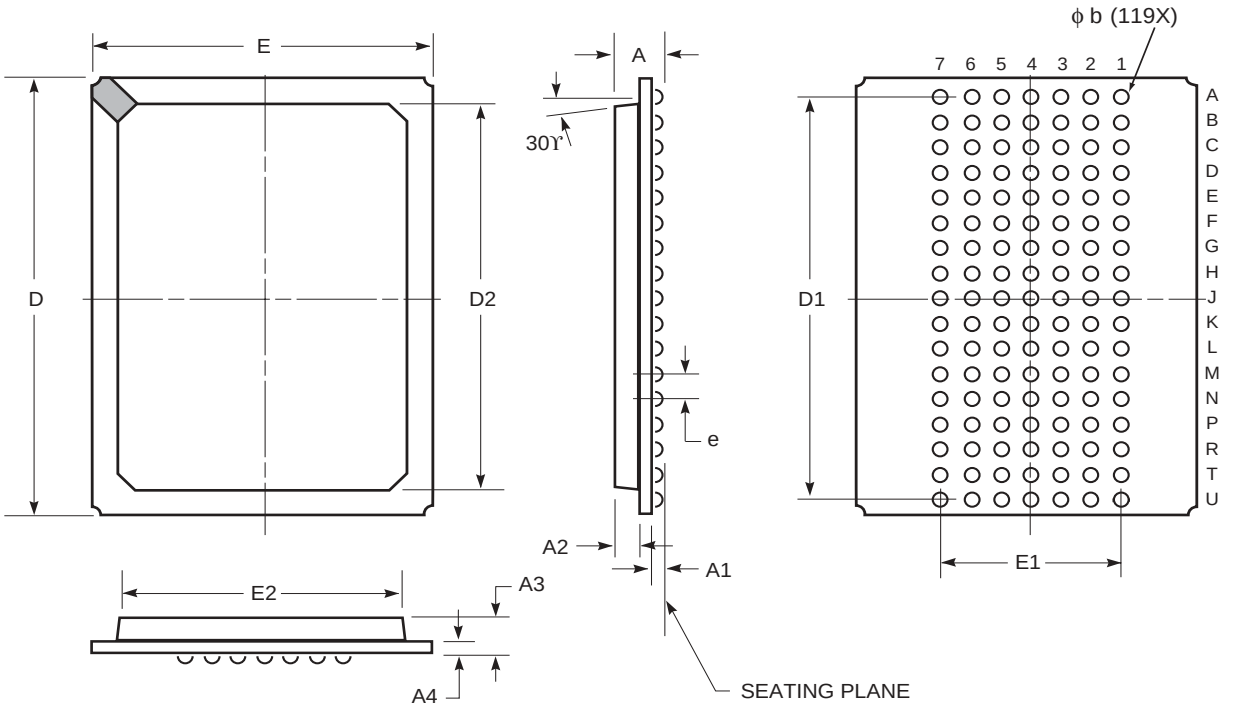
Speed	Order Part Number	Package
166 MHz	IS61SP12836-166TQ	TQFP
	IS61SP12836-166B	PBGA
133 MHz	IS61SP12836-133TQ	TQFP

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
166 MHz	IS61SP12836-166TQI	TQFP

PACKAGING INFORMATION

Plastic Ball Grid Array
Package Code: B (119-pin)

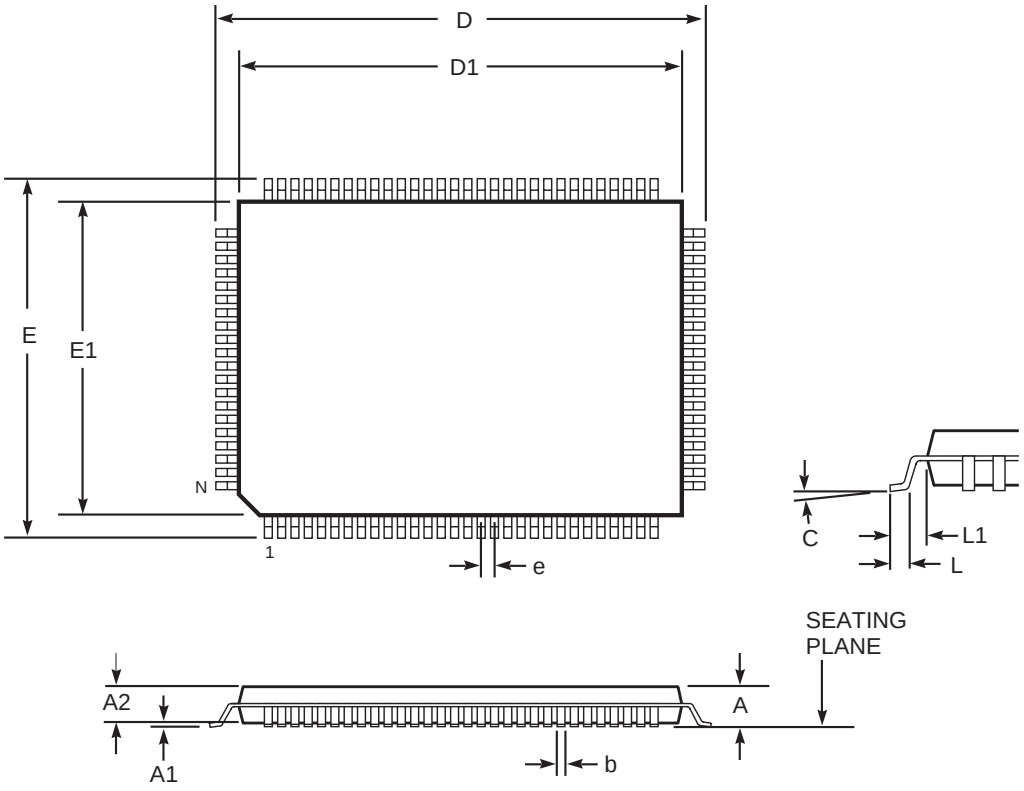


	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
N0. Leads		**119**		
A	—	2.41	—	0.095
A1	0.50	0.70	0.020	0.028
A2	0.80	1.00	0.032	0.039
A3	1.30	1.70	0.051	0.067
A4	0.56 BSC		0.022 BSC	
b	0.60	0.90	0.024	0.035
D	21.80	22.20	0.858	0.874
D1	20.32 BSC		0.800 BSC	
D2	19.40	19.60	0.764	0.772
E	13.80	14.20	0.543	0.559
E1	7.62 BSC		0.300 BSC	
E2	11.90	12.10	0.469	0.476
e	1.27 BSC		0.050 BSC	

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flat Pack (TQ)								
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads (N)	100				128			
A	—	1.60	—	0.063	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°	0°	7°	0°	7°

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.