

# NTB6412AN, NTP6412AN, NVB6412AN

## N-Channel Power MOSFET 100 V, 58 A, 18.2 mΩ

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

| Parameter                                                                                                                                                          |                        |                        | Symbol                            | Value       | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|-----------------------------------|-------------|------|
| Drain-to-Source Voltage                                                                                                                                            |                        |                        | V <sub>DSS</sub>                  | 100         | V    |
| Gate-to-Source Voltage – Continuous                                                                                                                                |                        |                        | V <sub>GS</sub>                   | ± 20        | V    |
| Continuous Drain Current R <sub>θJC</sub>                                                                                                                          | Steady State           | T <sub>C</sub> = 25°C  | I <sub>D</sub>                    | 58          | A    |
|                                                                                                                                                                    |                        | T <sub>C</sub> = 100°C |                                   | 41          |      |
| Power Dissipation R <sub>θJC</sub>                                                                                                                                 | Steady State           | T <sub>C</sub> = 25°C  | P <sub>D</sub>                    | 167         | W    |
| Pulsed Drain Current                                                                                                                                               | t <sub>p</sub> = 10 μs |                        | I <sub>DM</sub>                   | 240         | A    |
| Operating Junction and Storage Temperature Range                                                                                                                   |                        |                        | T <sub>J</sub> , T <sub>stg</sub> | –55 to +175 | °C   |
| Source Current (Body Diode)                                                                                                                                        |                        |                        | I <sub>S</sub>                    | 58          | A    |
| Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 50 Vdc, V <sub>GS</sub> = 10 Vdc, I <sub>L(pk)</sub> = 44.7 A, L = 0.3 mH, R <sub>G</sub> = 25 Ω) |                        |                        | E <sub>AS</sub>                   | 300         | mJ   |
| Lead Temperature for Soldering Purposes, 1/8” from Case for 10 Seconds                                                                                             |                        |                        | T <sub>L</sub>                    | 260         | °C   |

### THERMAL RESISTANCE RATINGS

| Parameter                             | Symbol          | Max | Unit               |
|---------------------------------------|-----------------|-----|--------------------|
| Junction-to-Case (Drain) Steady State | $R_{\theta JC}$ | 0.9 | $^\circ\text{C/W}$ |
| Junction-to-Ambient (Note 1)          | $R_{\theta JA}$ | 33  |                    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

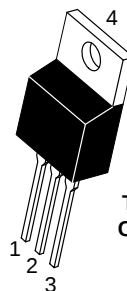
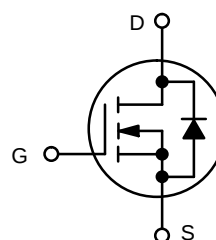


ON Semiconductor®

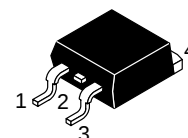
[www.onsemi.com](http://www.onsemi.com)

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$<br>(Note 1) |
|---------------|--------------------------|-------------------------------|
| 100 V         | 18.2 mΩ @ 10 V           | 58 A                          |

### N-Channel

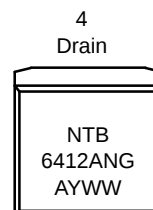
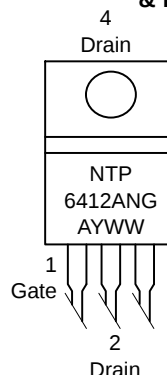


TO-220AB  
CASE 221A  
STYLE 5



D²PAK  
CASE 418B  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



6412AN = Specific Device Code  
G = Pb-Free Device  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTB6412AN, NTP6412AN, NVB6412AN

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|--------|----------------|-----|-----|-----|------|
|-----------------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                                           |                   |                                                     |                           |     |           |               |
|-----------------------------------------------------------|-------------------|-----------------------------------------------------|---------------------------|-----|-----------|---------------|
| Drain-to-Source Breakdown Voltage                         | $V_{(BR)DSS}$     | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 100                       |     |           | V             |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ |                                                     |                           | 103 |           | mV/°C         |
| Zero Gate Voltage Drain Current                           | $I_{DSS}$         | $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$        | $T_J = 25^\circ\text{C}$  |     | 1.0       | $\mu\text{A}$ |
|                                                           |                   |                                                     | $T_J = 125^\circ\text{C}$ |     | 100       |               |
| Gate-to-Source Leakage Current                            | $I_{GSS}$         | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$     |                           |     | $\pm 100$ | nA            |

### ON CHARACTERISTICS (Note 2)

|                                            |                  |                                                 |     |      |      |            |
|--------------------------------------------|------------------|-------------------------------------------------|-----|------|------|------------|
| Gate Threshold Voltage                     | $V_{GS(th)}$     | $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ | 2.0 |      | 4.0  | V          |
| Negative Threshold Temperature Coefficient | $V_{GS(th)}/T_J$ |                                                 |     | 9.2  |      | mV/°C      |
| Drain-to-Source On-Resistance              | $R_{DS(on)}$     | $V_{GS} = 10\text{ V}, I_D = 58\text{ A}$       |     | 16.8 | 18.2 | m $\Omega$ |
|                                            |                  | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$       |     | 15.6 | 18.2 |            |
| Forward Transconductance                   | $g_{FS}$         | $V_{DS} = 5\text{ V}, I_D = 20\text{ A}$        |     | 31   |      | S          |

### CHARGES, CAPACITANCES & GATE RESISTANCE

|                              |              |                                                                 |  |      |      |          |
|------------------------------|--------------|-----------------------------------------------------------------|--|------|------|----------|
| Input Capacitance            | $C_{iss}$    | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$   |  | 2700 | 3500 | pF       |
| Output Capacitance           | $C_{oss}$    |                                                                 |  | 400  | 500  |          |
| Reverse Transfer Capacitance | $C_{rss}$    |                                                                 |  | 150  |      |          |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 80\text{ V}, I_D = 58\text{ A}$ |  | 73   | 100  | nC       |
| Threshold Gate Charge        | $Q_{G(TH)}$  |                                                                 |  | 2.5  |      |          |
| Gate-to-Source Charge        | $Q_{GS}$     |                                                                 |  | 13.5 |      |          |
| Gate-to-Drain Charge         | $Q_{GD}$     |                                                                 |  | 35   |      |          |
| Plateau Voltage              | $V_{GP}$     |                                                                 |  | 5.6  |      | V        |
| Gate Resistance              | $R_G$        |                                                                 |  | 2.2  |      | $\Omega$ |

### SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

|                     |              |                                                                                          |  |     |  |    |
|---------------------|--------------|------------------------------------------------------------------------------------------|--|-----|--|----|
| Turn-On Delay Time  | $t_{d(on)}$  | $V_{GS} = 10\text{ V}, V_{DD} = 80\text{ V}, I_D = 58\text{ A}, R_G = 6.2\text{ }\Omega$ |  | 16  |  | ns |
| Rise Time           | $t_r$        |                                                                                          |  | 140 |  |    |
| Turn-Off Delay Time | $t_{d(off)}$ |                                                                                          |  | 70  |  |    |
| Fall Time           | $t_f$        |                                                                                          |  | 126 |  |    |

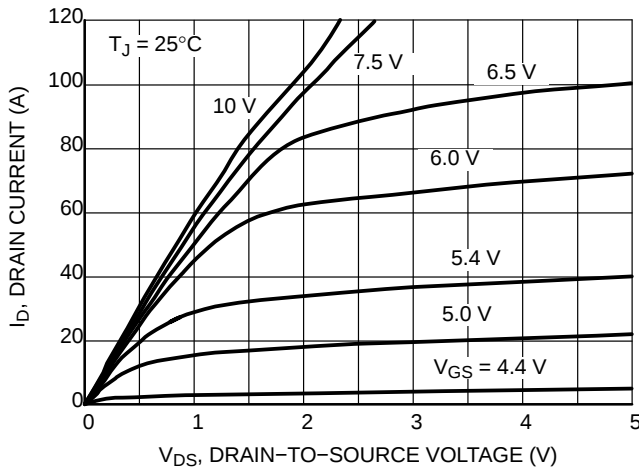
### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |                 |                                                                                  |                        |  |      |     |    |
|-------------------------|-----------------|----------------------------------------------------------------------------------|------------------------|--|------|-----|----|
| Forward Diode Voltage   | V <sub>SD</sub> | I <sub>S</sub> = 58 A                                                            | T <sub>J</sub> = 25°C  |  | 0.96 | 1.3 | V  |
|                         |                 |                                                                                  | T <sub>J</sub> = 125°C |  | 0.89 |     |    |
| Reverse Recovery Time   | t <sub>rr</sub> | V <sub>GS</sub> = 0 V, I <sub>S</sub> = 58 A,<br>dI <sub>SD</sub> /dt = 100 A/μs |                        |  | 85   |     | ns |
| Charge Time             | t <sub>a</sub>  |                                                                                  |                        |  | 60   |     |    |
| Discharge Time          | t <sub>b</sub>  |                                                                                  |                        |  | 25   |     |    |
| Reverse Recovery Charge | Q <sub>RR</sub> |                                                                                  |                        |  | 270  |     | nC |

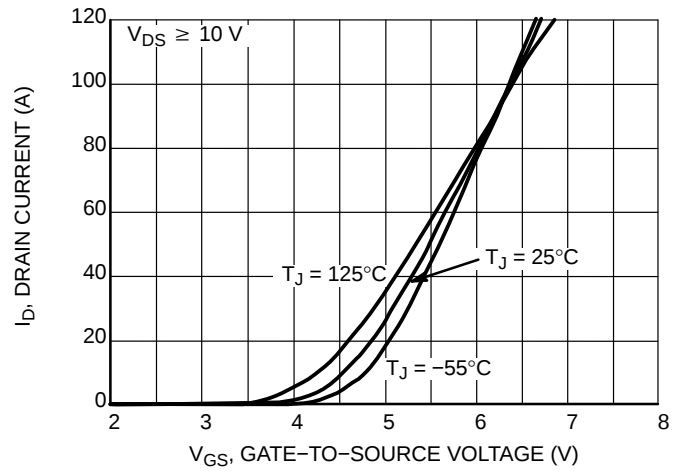
2. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

3. Switching characteristics are independent of operating junction temperatures.

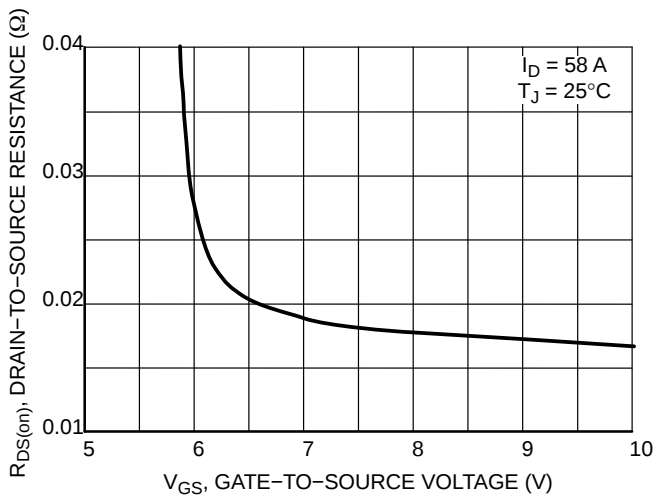
# NTB6412AN, NTP6412AN, NVB6412AN



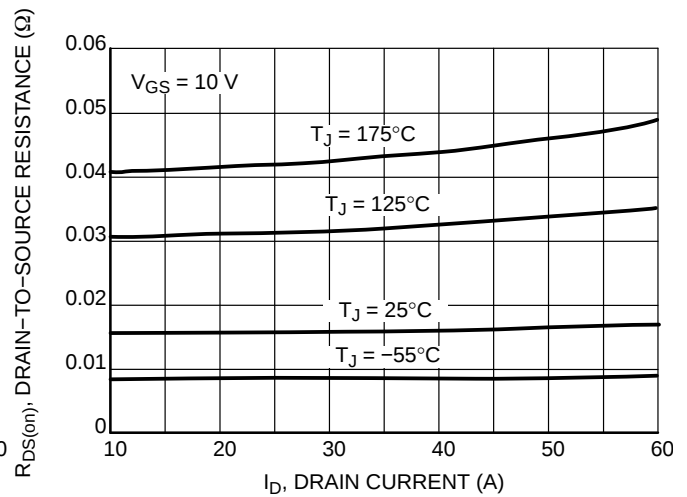
**Figure 1. On-Region Characteristics**



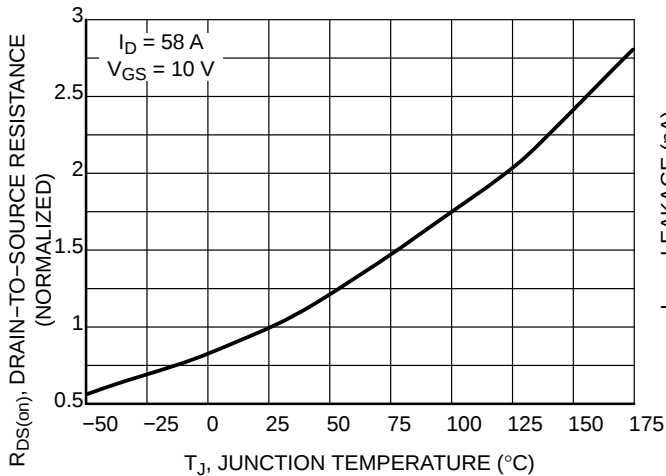
**Figure 2. Transfer Characteristics**



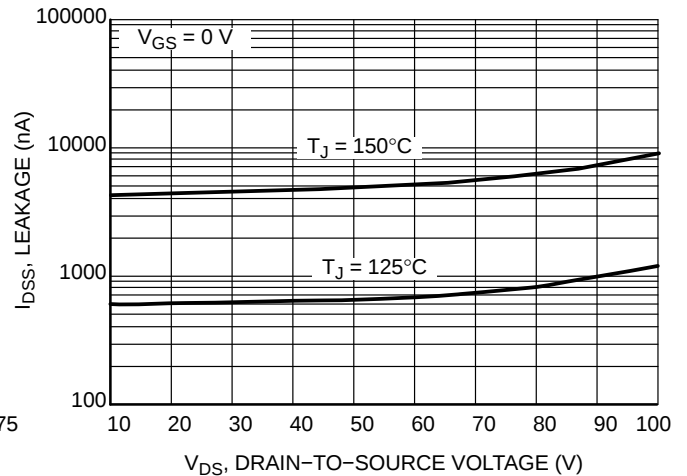
**Figure 3. On-Region versus Gate Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

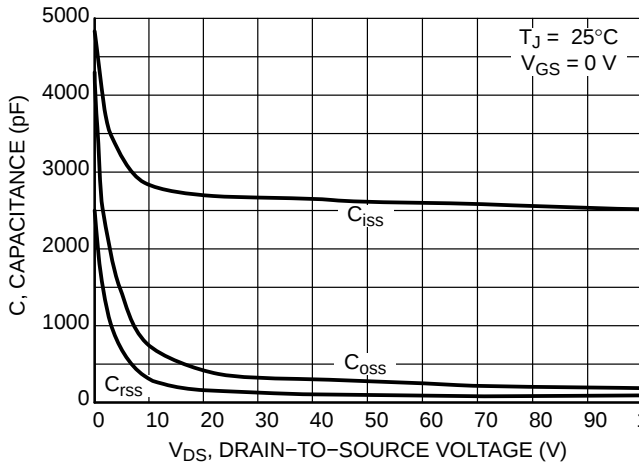


Figure 7. Capacitance Variation

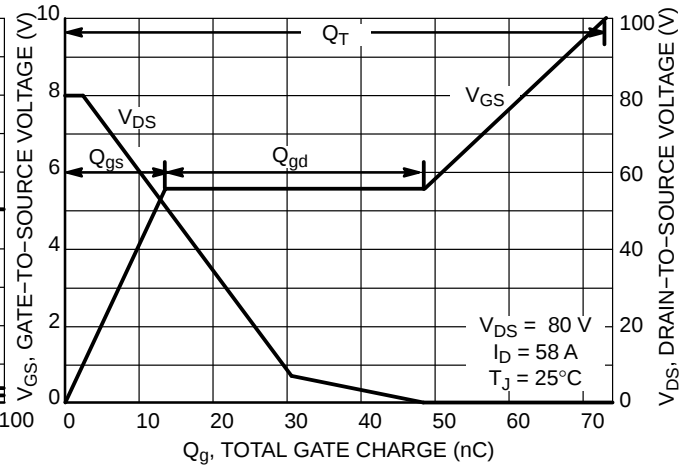


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

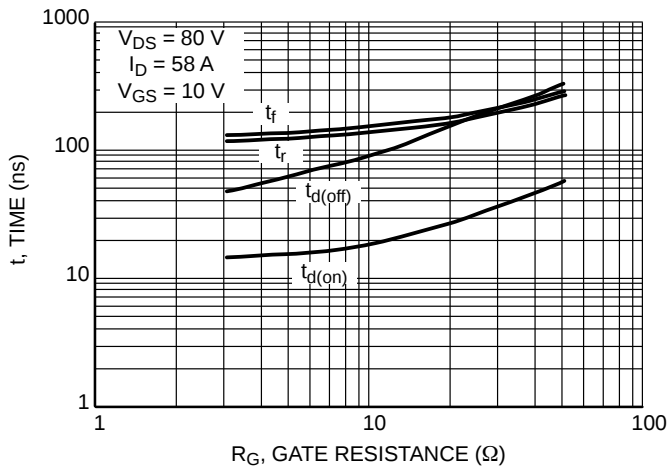


Figure 9. Resistive Switching Time Variation versus Gate Resistance

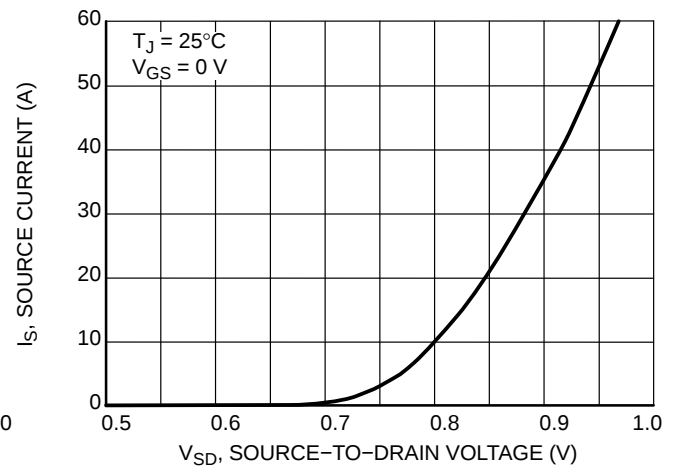


Figure 10. Diode Forward Voltage versus Current

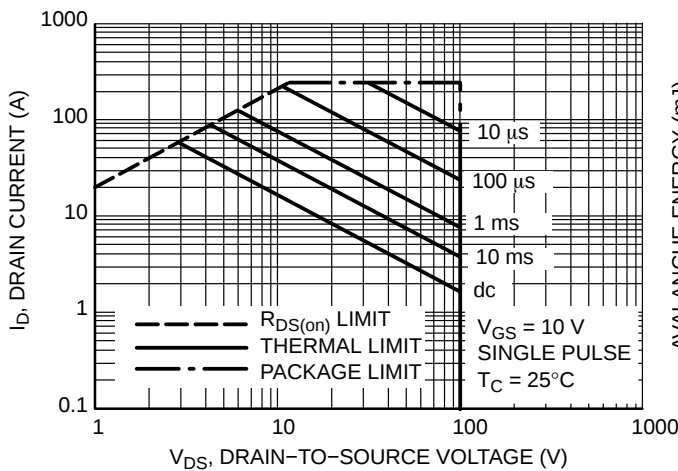


Figure 11. Maximum Rated Forward Biased Safe Operating Area

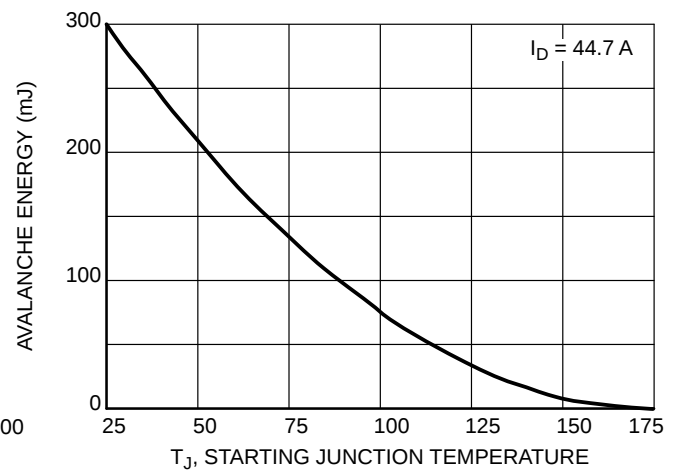
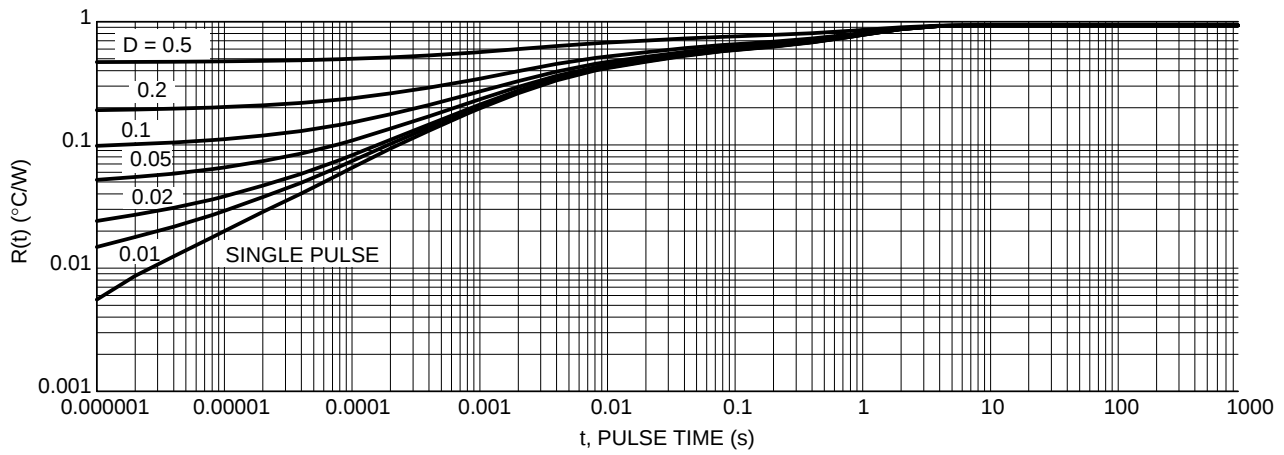


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTB6412AN, NTP6412AN, NVB6412AN



**Figure 13. Thermal Response**

## ORDERING INFORMATION

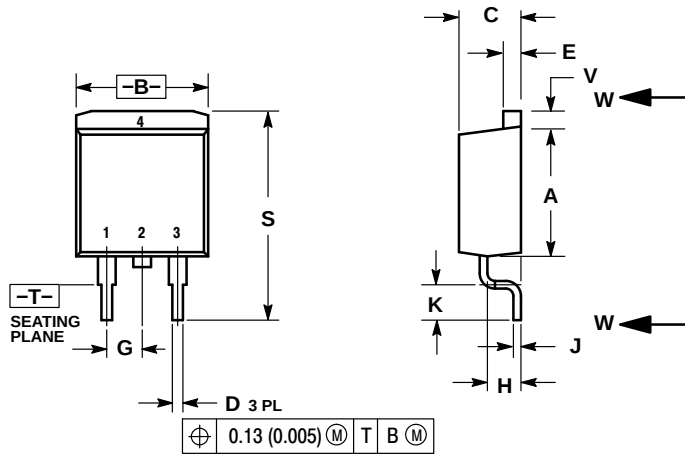
| Device       | Package                         | Shipping <sup>†</sup> |
|--------------|---------------------------------|-----------------------|
| NTB6412ANG   | D <sup>2</sup> PAK<br>(Pb-Free) | 50 Units / Rail       |
| NTB6412ANT4G | D <sup>2</sup> PAK<br>(Pb-Free) | 800 / Tape & Reel     |
| NTP6412ANG   | TO-220<br>(Pb-Free)             | 50 Units / Rail       |
| NVB6412ANT4G | D <sup>2</sup> PAK<br>(Pb-Free) | 800 / Tape & Reel     |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTB6412AN, NTP6412AN, NVB6412AN

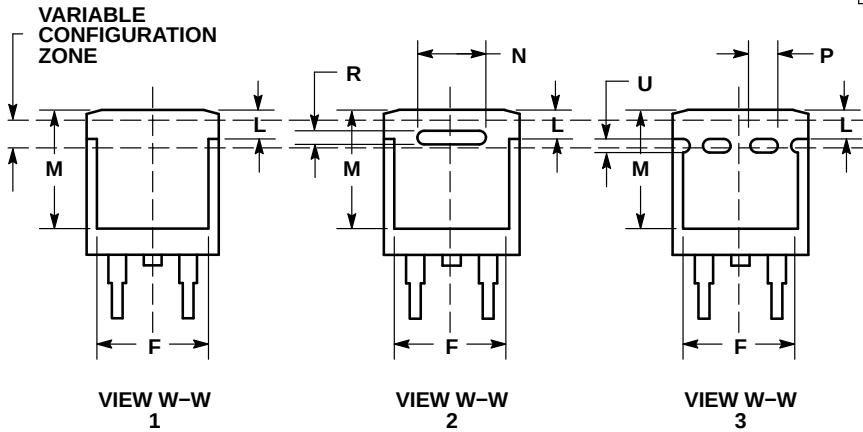
## PACKAGE DIMENSIONS

### D<sup>2</sup>PAK 3 CASE 418B-04 ISSUE K



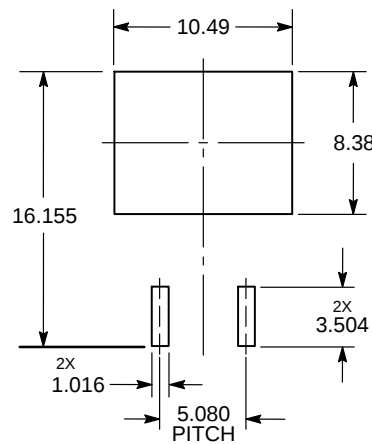
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.340     | 0.380 | 8.64        | 9.65  |
| B   | 0.380     | 0.405 | 9.65        | 10.29 |
| C   | 0.160     | 0.190 | 4.06        | 4.83  |
| D   | 0.020     | 0.035 | 0.51        | 0.89  |
| E   | 0.045     | 0.055 | 1.14        | 1.40  |
| F   | 0.310     | 0.350 | 7.87        | 8.89  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.080     | 0.110 | 2.03        | 2.79  |
| J   | 0.018     | 0.025 | 0.46        | 0.64  |
| K   | 0.090     | 0.110 | 2.29        | 2.79  |
| L   | 0.052     | 0.072 | 1.32        | 1.83  |
| M   | 0.280     | 0.320 | 7.11        | 8.13  |
| N   | 0.197 REF |       | 5.00 REF    |       |
| P   | 0.079 REF |       | 2.00 REF    |       |
| R   | 0.039 REF |       | 0.99 REF    |       |
| S   | 0.575     | 0.625 | 14.60       | 15.88 |
| V   | 0.045     | 0.055 | 1.14        | 1.40  |



- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### SOLDERING FOOTPRINT\*



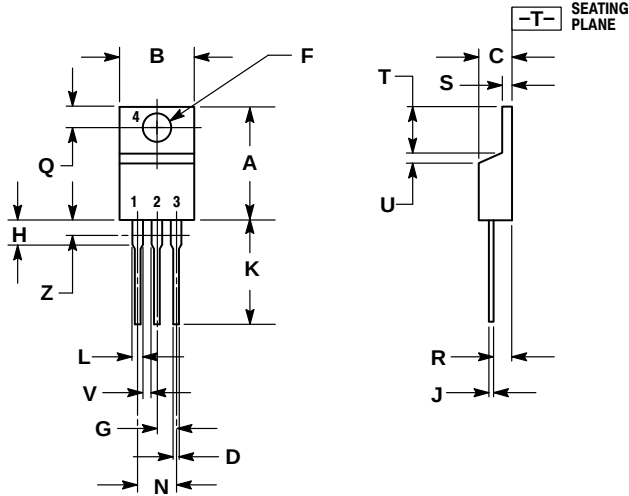
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTB6412AN, NTP6412AN, NVB6412AN

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AH



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN    | MAX   | MIN         | MAX   |
| A   | 0.570  | 0.620 | 14.48       | 15.75 |
| B   | 0.380  | 0.415 | 9.66        | 10.53 |
| C   | 0.160  | 0.190 | 4.07        | 4.83  |
| D   | 0.025  | 0.038 | 0.64        | 0.96  |
| F   | 0.142  | 0.161 | 3.61        | 4.09  |
| G   | 0.095  | 0.105 | 2.42        | 2.66  |
| H   | 0.110  | 0.161 | 2.80        | 4.10  |
| J   | 0.014  | 0.024 | 0.36        | 0.61  |
| K   | 0.500  | 0.562 | 12.70       | 14.27 |
| L   | 0.045  | 0.060 | 1.15        | 1.52  |
| N   | 0.190  | 0.210 | 4.83        | 5.33  |
| Q   | 0.100  | 0.120 | 2.54        | 3.04  |
| R   | 0.080  | 0.110 | 2.04        | 2.79  |
| S   | 0.045  | 0.055 | 1.15        | 1.39  |
| T   | 0.235  | 0.255 | 5.97        | 6.47  |
| U   | 0.000  | 0.050 | 0.00        | 1.27  |
| V   | 0.045  | ---   | 1.15        | ---   |
| Z   | ---    | 0.080 | ---         | 2.04  |

### STYLE 5:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NTB6412AN/D