WM8725

99dB Stereo DAC

DESCRIPTION

WM8725 is a high-performance stereo DAC designed for use in portable audio equipment, video CD players and similar applications. It comprises selectable normal or I^2S compatible serial data interfaces for 16 to 24-bit digital inputs, high performance digital filters, and sigma-delta output DACs, achieving an excellent 99dB signal-to-noise performance.

The device is available in a 14-lead SOIC package that offers selectable mute and de-emphasis functions using a minimum of external components.

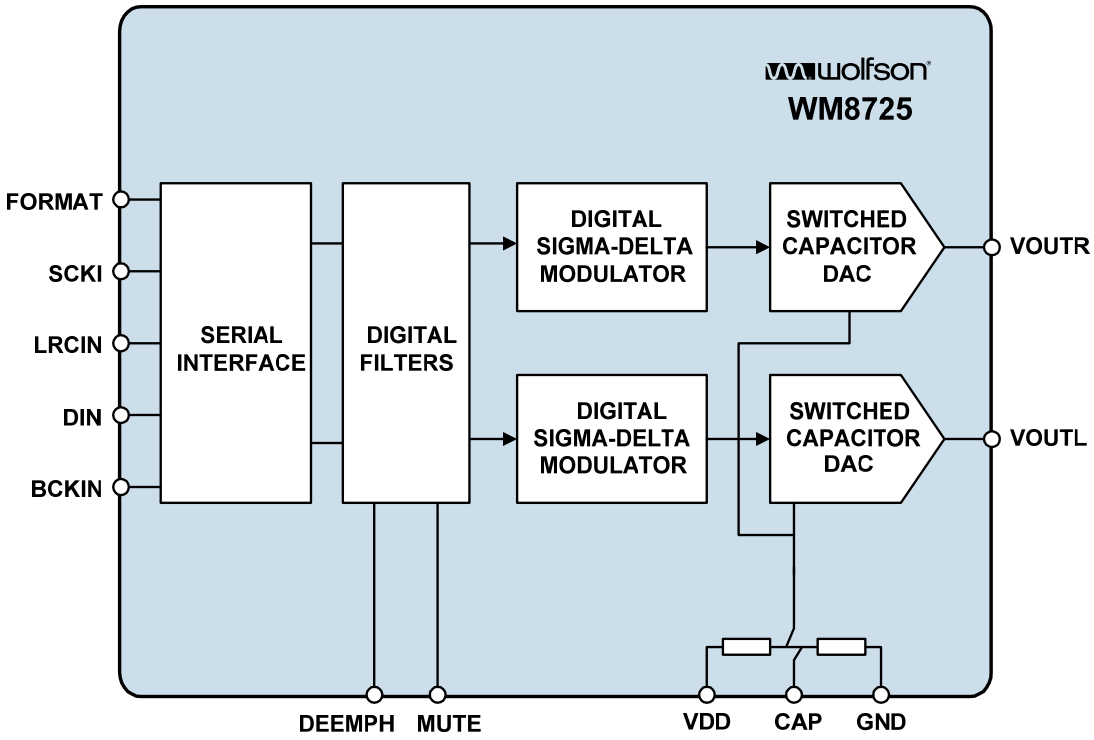
FEATURES

- 99dB SNR performance
- Stereo DAC with input sampling from 8kHz to 96kHz
- Additional mute feature
- Normal or I^2S compatible data format
- Sigma-delta design with 64x oversampling
- System clock 256fs or 384fs
- Supply range 3V to 5V
- 14-lead SOIC package

APPLICATIONS

- Portable audio equipment
- Video CD players

BLOCK DIAGRAM



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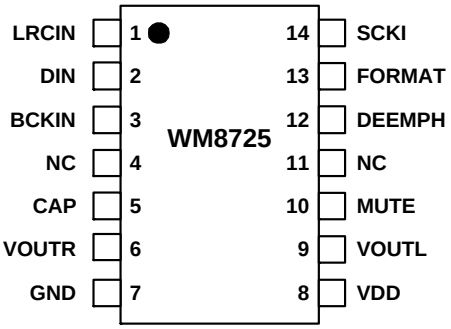
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK BODY TEMPERATURE
WM8725CGED	-40°C to +85°C	14-lead SOIC (lead free)	MSL1	260°C
WM8725CGED/R	-40°C to +85°C	14-lead SOIC (Pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity: 3,000

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7.0V
Reference input		VCC+0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature	-65°C	+150°C
Lead temperature (soldering, 10 seconds)		+240°C
Lead temperature (soldering, 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Range	VDD		-10%	3.0 to 5.0	+10%	V
Ground	GND			0		V
Supply Current		VDD = 5V		15	25	mA
		VDD = 3V		7.5		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

V_{DD} = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Analogue Output Levels						
Load Resistance		To midrail or AC coupled (5V supply)	1			kΩ
		To midrail or AC coupled (3V supply)	1			kΩ
Maximum capacitance load		5V or 3V		100		pF
Output DC level				$V_{DD}/2$		V
Reference Levels						
Potential divider resistance		V_{DD} to CAP and CAP to GND	80	100	120	kΩ
Voltage at CAP		VDD = 5V	2.3	2.5	2.7	V
DAC Circuit Specifications						
SNR (Note 1)		VDD = 5V	90	99		dB
		VDD = 3V		97		dB
Full scale output voltage		Into 10kohm VDD = 5V, 0dB	0.9	1.0	1.1	V_{RMS}
		Into 10kohm VDD = 3V, 0dB		0.6		V_{RMS}
THD (Full scale)		0dB		0.01	0.02	%
THD+N (Dynamic range)		-60dB		92		dB
Frequency response			0		20,000	Hz
Transition band			20,000			Hz
Out of band rejection				-40		dB
Channel Separation				90		dB
Gain mismatch channel-to-channel				±1	±5	%FSR
Audio Data Input and System Clock Timing Information						
BCKIN pulse cycle time	t_{BCY}		100			ns
BCKIN pulse width high	t_{BCH}		50			ns
BCKIN pulse width low	t_{BCL}		50			ns
BCKIN rising edge to LRCIN edge	t_{BL}		30			ns
LRCIN rising edge to BCKIN rising edge	t_{LB}		30			ns
DIN setup time	t_{DS}		30			ns
DIN hold time	t_{DH}		30			ns
System clock pulse width high	t_{SCKIH}		13			ns
System clock pulse width low	t_{SCKIL}		13			ns

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured "A" weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible, it may affect dynamic specification values.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial data input
3	BCKIN	Digital input	Bit clock input
4	NC	No connect	No internal connection
5	CAP	Analogue output	Analogue internal reference
6	VOUTR	Analogue output	Right channel DAC output
7	GND	Supply	0V supply
8	VDD	Supply	Positive supply
9	VOUTL	Analogue output	Left channel DAC output
10	MUTE	Digital input	Mute control, high = muted. Internal pull-down
11	NC	No connect	No internal connection
12	DEEMPH	Digital input	De-emphasis select, high = de-emphasis ON. Internal pull-up
13	FORMAT	Digital input	Data input format select, low = normal, high = I^2S. Internal pull-up
14	SCKI	Digital input	System clock input (256fs or 384fs)

INTERNAL POWER ON RESET

The WM8725 includes an internal power-on reset circuit. This is shown in Figure 1.This reset circuit is used to reset the digital logic into a default state after power up.

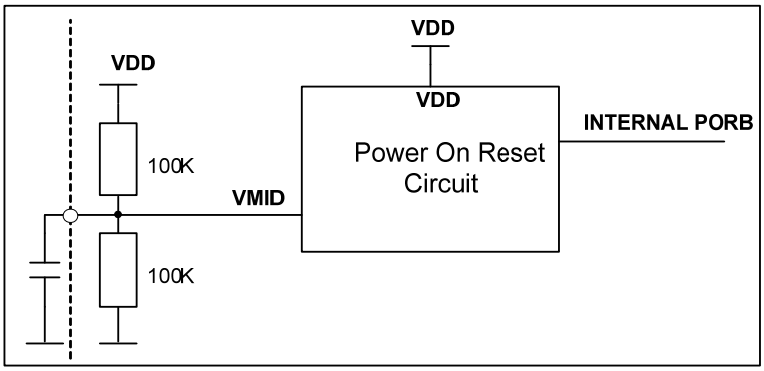


Figure 1 Internal Power on Reset Circuit

The timing of the power on reset is shown in Figure 2 The circuit monitors VDD and VMID (CAP pin) and asserts PORB low when VMID is below the minimum threshold Vpor. It is assumed that VMID will rise slower than VCC due to the capacitor on VMID.

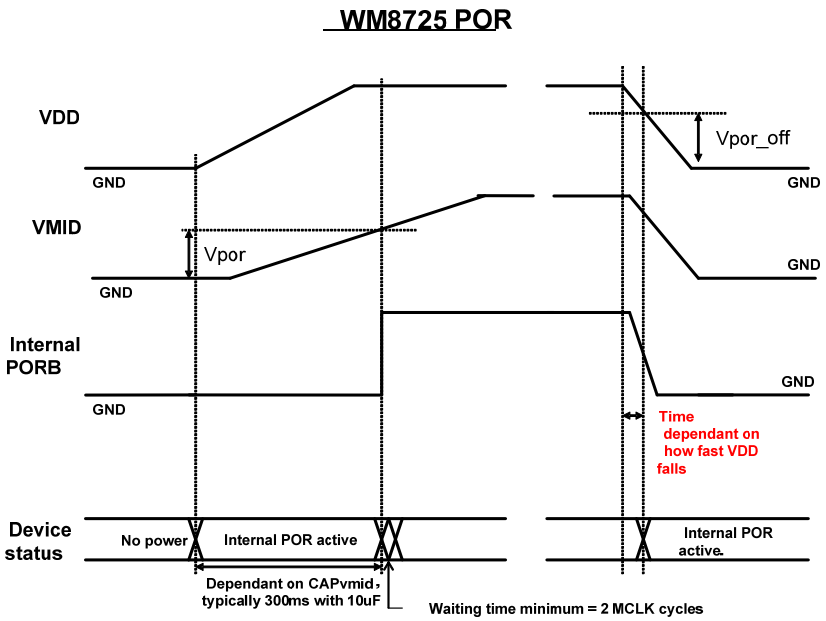


Figure 2 Power on/off Reset Timing

SYMBOL	Min	Typ	Max	Unit
Vpor	0.85	1.0	1.2	V
Vpor_off	2.25	2.5	2.75	V

Table 1 Power on/off Reset Timing

At power on, when VDD and VMID have been established, PORB is released and the WM8725 has been reset.

At power down, PORB is asserted low whenever VMID drops below the minimum threshold of Vpor_off.

If VDD is removed at any time, the internal power-on reset circuit is powered down and PORB will follow VDD.

DEVICE DESCRIPTION

INTRODUCTION

WM8725 is a complete stereo audio 16-24 bit digital-to-analogue converter, including digital interpolation filter, multibit sigma-delta with dither, and switched capacitor multibit stereo DAC and output smoothing filters.

Special functions of mute and de-emphasis are provided, and operation using system clock of 256fs or 384fs is provided, selection between either clock rate being automatically controlled. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

MUTE	DESCRIPTION
0	Mute is OFF
1	Mute is ON

Table 2 Mute Control

A novel multi bit sigma-delta DAC design is used, utilising a 64x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance.

Internally generated midrail references are used to DC bias output signals, requiring only a single external capacitor for decoupling purposes.

Single 3V to 5V supplies may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption, and the low pin count small package, make the WM8725 attractive for many consumer type applications.

DAC CIRCUITS

The WM8725 DACs are designed to allow playback of 16-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates up to 96ks/s may be used, with much lower sample rates acceptable provided that the ratio of sample rate (LRCIN) to system clock is maintained at the required 256fs or 384fs times.

The DACs on WM8725 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the 96ks/s input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the full performance to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images, on the output of the DAC. To ensure that generation of tones characteristic to sigma-delta convertors is not a problem, dithering is used in the digital modulator and a higher order modulator is used. The switched capacitor technique used in the DAC reduces sensitivity to clock jitter compared to switched current techniques used in other implementations.

De-emphasis of 44.1kHz signals may be applied if required.

DEEMPH	DESCRIPTION
0	De-emphasis is OFF
1	De-emphasis is ON

Table 3 De-emphasis Control

The voltage on the CAP pin is used as the reference for the DACs, therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP. An external reference could be used to drive into the CAP pin if desired, but a value typically of about midrail should be used for optimum performance.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers. These amplifiers will source load current of several mA and sink current up to 1.5mA, so allowing significant loads to be driven. The output source is active and the sink is Class A, i.e. fixed value, so greater loads might be driven if an external 'pull-down' resistor is connected at the output.

Typically an external low pass filter circuit will be used to remove residual sampling noise of the 64x oversampling used and if desired adjust the signal amplitude and device strength.

SERIAL DATA INTERFACE

WM8725 has serial interface formats that are fully compatible with both normal (MSB first, 16 bit right-justified) and I^2S interfaces. The data format is selected with the FORMAT pin. When FORMAT is LOW, normal data format is selected. When the format is HIGH, I^2S format is selected. It must be noted that in "packed" mode operation (exactly 32 BCLKs per LRCIN period), the data word must align exactly with LRCIN clock edges (effectively both left and right justified at the same time). This is true in both normal and I^2S modes.

FORMAT	DESCRIPTION
0	Normal format (MSB-first, 16 bit right justified)
1	I^2S format (Philips serial data protocol)

Table 4 Serial Interface Formats

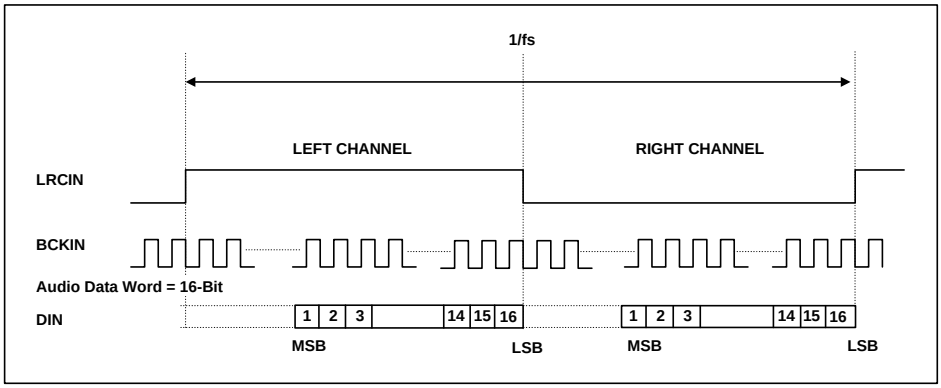


Figure 3 'Normal' Data Input Timing

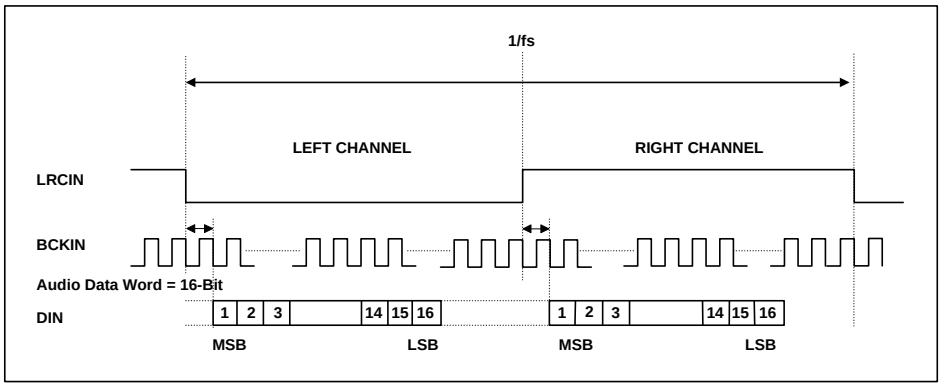


Figure 4 I2S Data Input Timing

SYSTEM CLOCK

The system clock is used to operate the digital filters and the noise shaping circuits. The system clock input is at pin 14 (SCKI). The frequency of WM8725's system clock should be set to 256fs or 384fs, (where fs is the audio sampling frequency). The sample rate is typically: 32 kHz, 44.1 kHz, 48 kHz or 96kHz.

WM8725 has a system clock detection circuit that automatically determines whether the system clock being supplied is at 256fs or 384fs. The system clock should be synchronised with LRCIN, but WM8725 is tolerant of phase differences. Severe distortion in the phase difference between LRCIN and the system clock will be detected, and cause the device to automatically resynchronise. During resynchronisation, the output of the device will either repeat the previous sample, or drop the next sample, depending on the nature of the phase slip. This will ensure minimal "click" at the analogue outputs during resynchronisation.

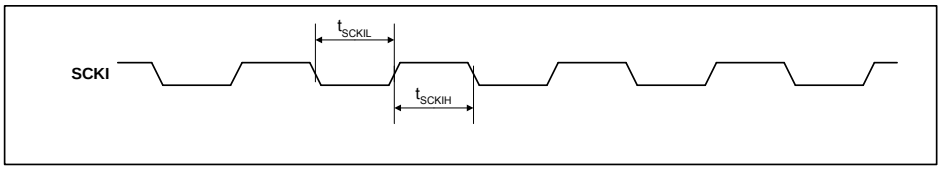


Figure 5 System Clock Timing Requirements

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHz)	
	256fs	384fs
32 kHz	8.192	12.288
44.1 kHz	11.2896	16.9340
48 kHz	12.288	18.432
96kHz	24.576[1]	36.864[1]

Table 5 System Clock Frequencies Versus Sampling Rate

Notes:

1 96kHz sample rate at either 256fs or 384fs are only supported with 5V supplies.

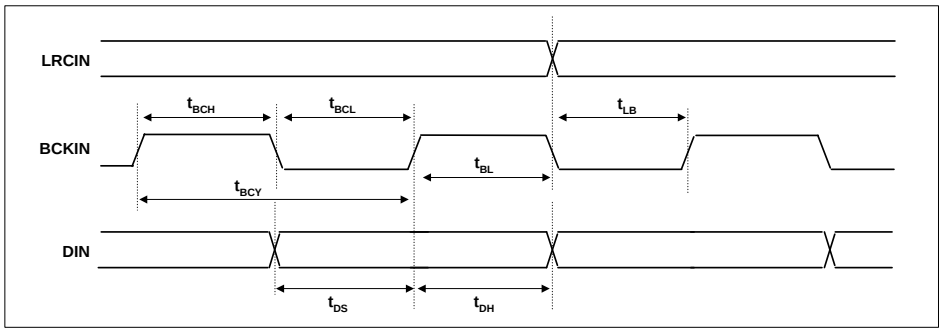


Figure 6 Audio Data Input Timing

RECOMMENDED EXTERNAL COMPONENTS

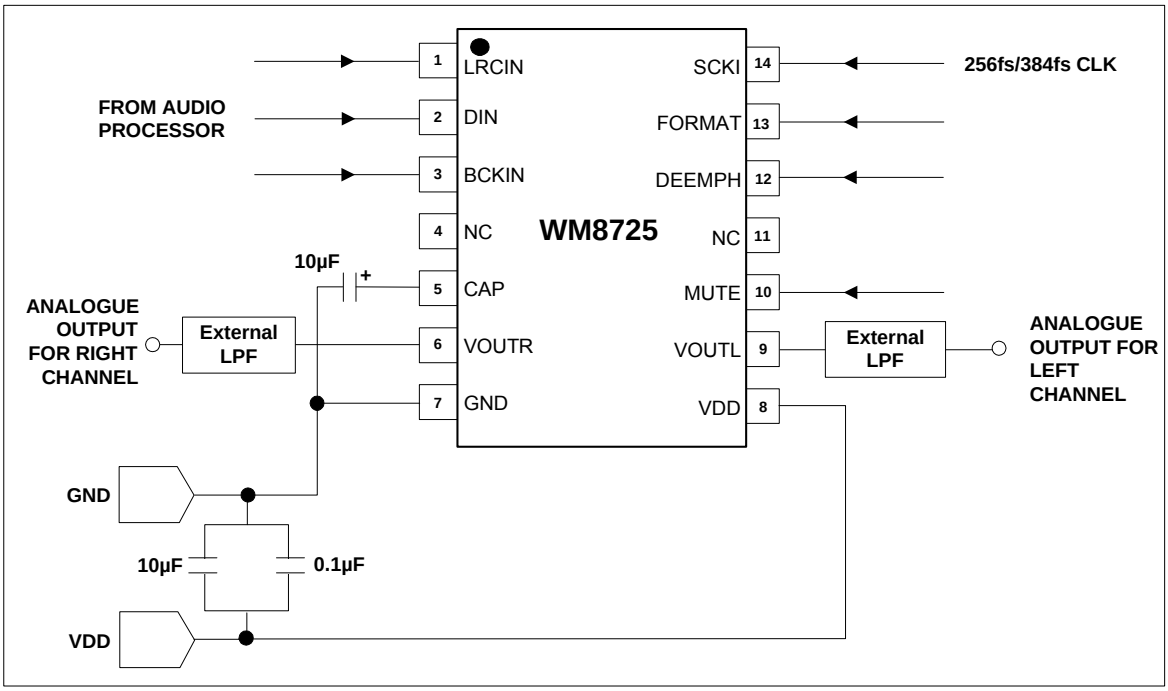


Figure 7 Recommended External Components

DETAIL OF RECOMMENDED EXTERNAL COMPONENTS SHOWING THE EXTERNAL LOW PASS FILTER

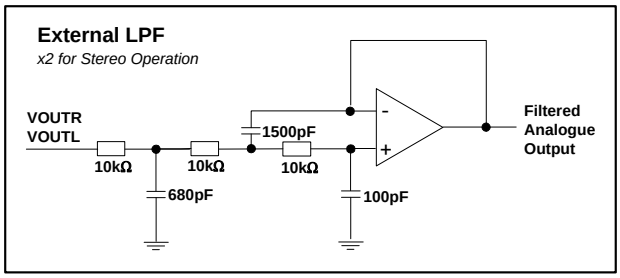


Figure 8 Third-Order Low Pass Filter (LPF) Example

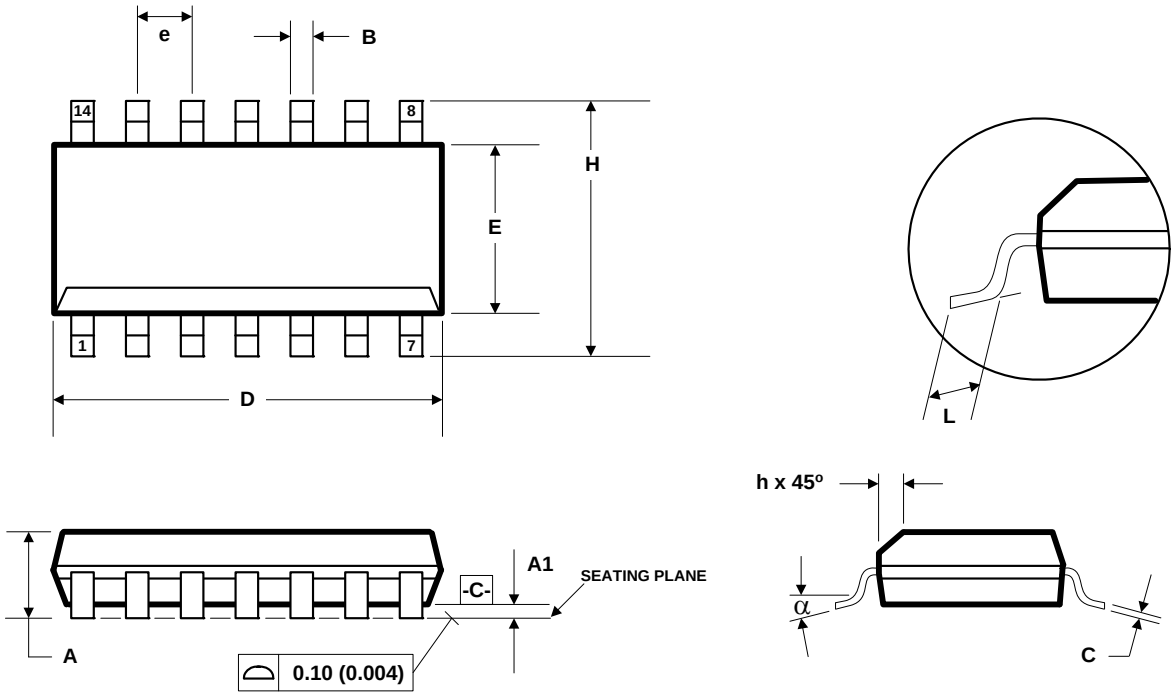
An external low pass filter is recommended (see Figure 8) if the device is driving a wideband amplifier. In some applications, second-order or passive RC filter may be adequate.

PCB LAYOUT

1. Place all supply decoupling capacitors as close as possible to their respective supply pins and provide a low impedance path from the capacitors to the appropriate ground.
2. Separate analogue and digital ground planes should be situated under respective analogue and digital device pins.
3. Avoid noise on the CAP reference pin. The decoupling capacitor should be placed as close to this pin as possible with a low impedance path from the capacitor to analogue ground.
4. Digital input signals should be screened from each other and from other sources of noise to avoid cross-talk and interference. They should also run over the digital ground plane to avoid introducing unwanted noise into the analogue ground plane.
5. Analogue output signal tracks should be kept as short as possible and over the analogue ground plane reducing the possibility of losing signal quality.

PACKAGE DIMENSIONS

D: 14 PIN SOIC 3.9mm Wide Body **DM001.C**



Symbols	Dimensions (MM)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
20/02/12	4.3	JMacD	Order codes updated from WM8725GED/V and WM8725GED/RV to WM8725**C**GED and WM8725**C**GED/R to reflect change to copper wire bonding.
20/02/12	4.3	JMacD	MSL changed from MSL2 to MSL1.
01/02/12	4.3	JMacD	Operating Temp changed to -40°C to +85°C