CX74001

Rx ASIC for CDMA, AMPS, and PCS Applications

The CX74001 Application-Specific Integrated Circuit (ASIC) is a triple-mode, dual-band receiver (Rx) intended for use in Code Division Multiple Access (CDMA) portable phones in both cellular and Personal Communications System (PCS) bands, as well as Advanced Mobile Phone System (AMPS) mode.

The device is a highly integrated super-heterodyne receiver. It incorporates all the components required to implement the receiver chain, from the low-noise amplifier (LNA) to the In-Phase and Quadrature (I/Q) demodulator stages, except for the external Surface Acoustic Wave (SAW) filters and matching components. There are two internal Low Noise Amplifiers (LNAs). The Cellular LNA has three-step gain stages, and the PCS LNA gain has a bypass feature.

After RF signal amplification and filtering, the received signal is mixed down from RF to the Intermediate Frequency (IF). There are separate mixers for AMPS, CDMA, and PCS bands. The CDMA cellular and PCS mixers have balanced outputs for the IF SAW filters, while the AMPS differential output can be combined externally to mate to a single-ended SAW filter. After IF filtering, the IF signal is amplified by a Variable Gain Amplifier (VGA) and fed to an I/Q demodulator resulting in baseband I/Q signals at the output.

The VGA has a minimum dynamic range of 90 dB with a control voltage range from 0.5 to 2.5 Volts, and it is common to all modes. There are two VHF oscillators which operates with external tank circuits to provide Local Oscillator (LO) frequencies for the I/Q demodulator in the cellular and PCS bands.

The noise figure, gain, and third order Input Intercept Point (IIP3) of each stage in the receiver chip are optimized to meet the system requirements for AMPS and CDMA modes as per TIA/EIA-98-C. Employing BiCMOS technology, the ASIC is designed for low cost, high performance, and a high level of integration.

A device package and pinout is shown in Figure 1, a block diagram is shown in Figure 2, a schematic diagram is shown Figure 4, and a package drawing is shown in Figure 5.

Features

- Supports single, dual-band, and tri-mode handsets
- Battery cell operation (2.7 V < Vcc < 3.3 V)
- Dual Low Noise Amplifiers (800 MHz / 1900 MHz)
- PCS LNA With Bypass Feature
- Three-Step Cellular LNA Gain
- I/Q Interface
- Dual 200-600 MHz VHF Oscillators
- VCO On/Off control For Standby Current Optimization
- CDMA Single IF Feature
- 7 x 7 mm RF Land Grid Array (RF-LGA™) package with down-set paddle (Figure 1)

Applications

- Cellular and PCS band phones
- CDMA and AMPS modes in the cellular band:
  - AMPS
  - CDMA-US
  - CDMA-Japan
- CDMA mode in the PCS band:
  - PCS-US
  - PCS-Korea

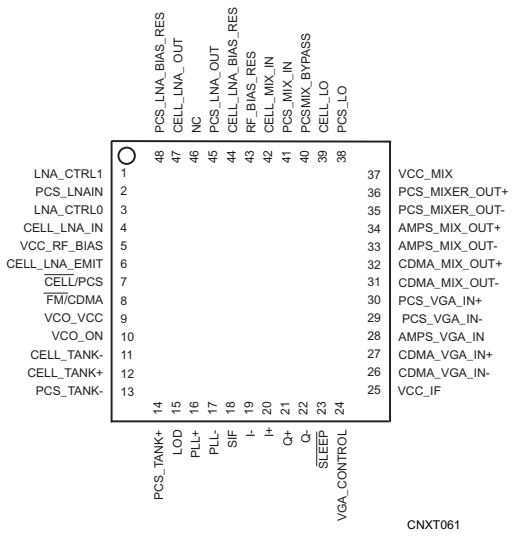


Figure 1. CX74001 Rx ASIC Pinout (Top View)

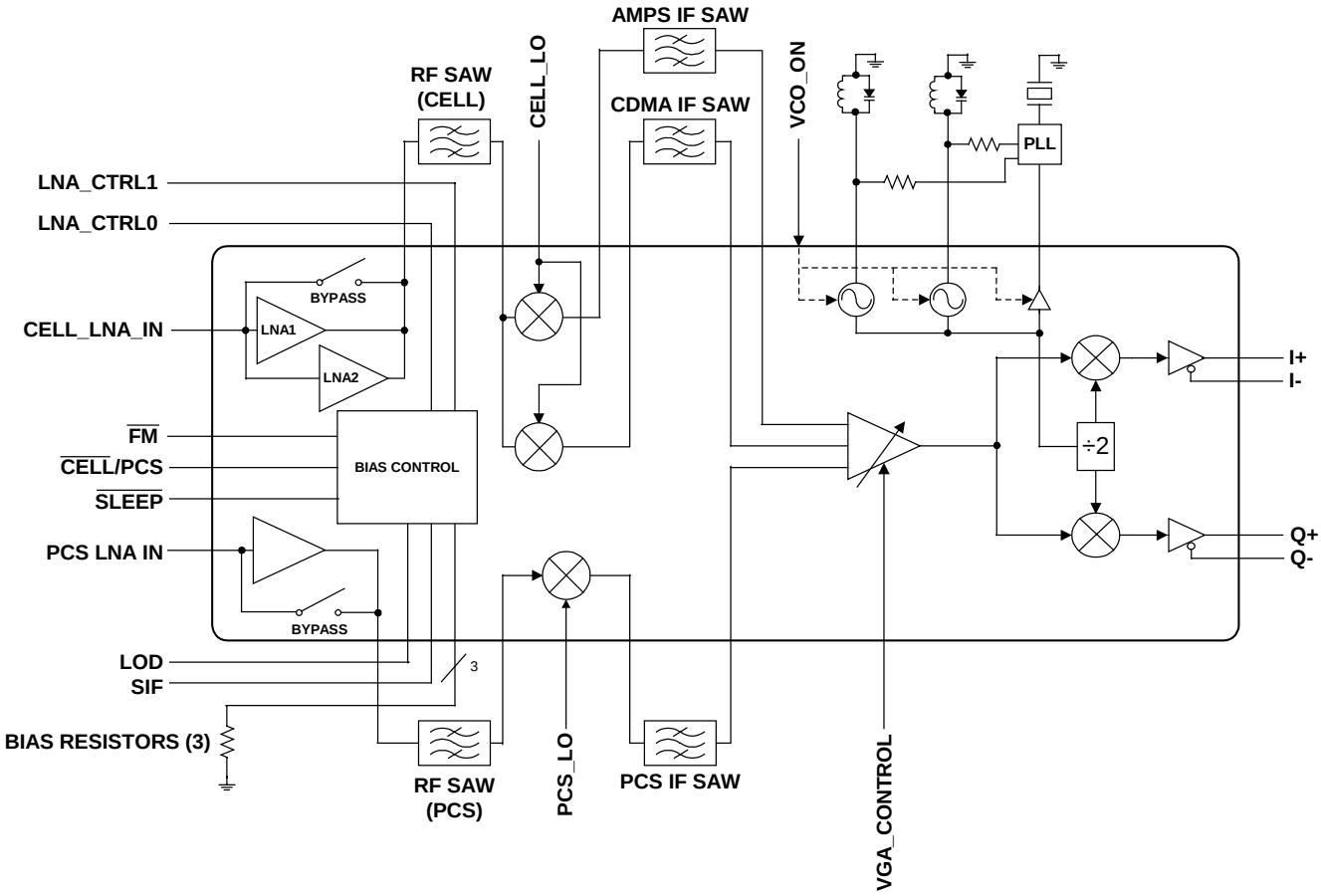


Figure 2. CX74001 Rx ASIC Block Diagram

Technical Description

Low Noise Amplifiers (LNAs). The cellular band LNA is designed with a low noise figure and high linearity to achieve receiver sensitivity and single-tone requirements. The cellular LNA is a three-step gain LNA designed to meet the inter-modulation distortion specifications in CDMA per TIA/EIA 98-C.

The PCS band LNA is also designed to provide a low noise figure and high linearity to achieve receiver sensitivity and single-tone requirements. At high signal strength, it is preferable to bypass the LNA completely, and the PCS LNA supports this feature.

Mixers. The CX74001 Rx ASIC has three independent mixers, one for the PCS band and two for the cellular band (AMPS and CDMA). The mixers are designed to operate with LO powers of –10 dBm, typical.

The cellular and PCS band mixers have a high gain and IIP3, and a low noise figure that allow them to meet the system requirements with margin. The cellular CDMA and PCS mixers have balanced output to drive the IF SAW filters. The differential outputs of the AMPS mixer are combined externally to mate to a single-ended input IF SAW filter.

Variable Gain Amplifier (VGA). The high dynamic range required by CDMA handsets is achieved by the VGA, which is common to all modes. It has three different inputs and the appropriate signal path is switched inside the chip. The VGA has a dynamic range of 90 dB with a control voltage of 0.5 to 2.5 volts. It has a low noise figure at maximum gain, which allows it to meet the system noise figure requirements. The balanced output is common for all the modes and is fed directly to the I/Q Demodulator.

I/Q Demodulator. The VGA stage is internally AC coupled to the I/Q demodulator. The LO signals are derived from one of the on-chip VCOs, then fed to a divider block that divides the VCO frequency by two. The differential I and Q outputs are designed specifically with a low DC output offset and a low phase and amplitude imbalance when cascaded with the baseband processor.

Voltage Controlled Oscillators (VCOs). The active cores of the two VCOs are present on the CX74001, requiring only differential external LC tanks and a PLL synthesizer. The VCO core current is automatically adjusted to give a constant VCO output swing, regardless of the external tank Q.

Mode Control. The operation of the chip is controlled by signals CELL/PCS, $\overline{FM}$, and $\overline{SLEEP}$. The Single IF (SIF) is added to use a common IF frequency for CDMA mode in cellular and PCS band. This allows the use of one IF SAW filter for the PCS and CDMA modes to reduce system implementation cost. The logic blocks are powered off of the Vcc_IF, so it must be present to obtain chip functionality.

Electrical and Mechanical Specifications. Included in this document are Tables 1 through 7 and Figures 1 through 3, which define the electrical and mechanical specifications of the CX74001.

ESD Sensitivity

The CX74001 is a Class 1 device. The following extreme Electrostatic Discharge (ESD) precautions are required according to the Human Body Model (HBM):

- Protective outer garments.
- Handle device in ESD safeguarded work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection equipment.

The HBM ESD withstand threshold value, with respect to ground, is ±1.5 kV. The HBM ESD withstand threshold value, with respect to VDD (the positive power supply terminal) is also ±1.5 kV.

Table 1. CX74001 Pin Assignments and Signal Descriptions (1 of 2)

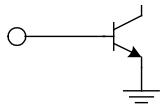
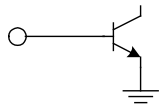
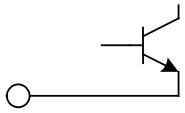
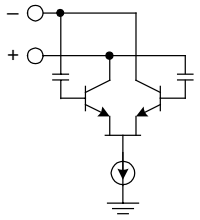
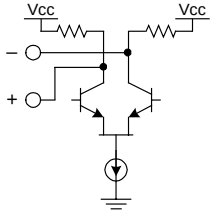
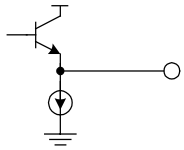
Pin #	Name	Description	Equivalent Circuit
1	LNA_CTRL1	Digital signal used in conjunction with pin 3 to control LNA gain step.	
2	PCS_LNAIN	PCS LNA input pin. High-Q matching network should be used to minimize noise figure, and a DC blocking capacitor is required.	
3	LNA_CTRL0	Digital signal used in conjunction with pin 1 to control LNA gain step.	
4	CELL_LNA_IN	Cellular LNA input pin. High-Q matching network should be used to minimize noise figure, and a DC blocking capacitor is required.	
5	VCC_RF_BIAS	Supply voltage to the RF bias (needed by all LNA/Mixer blocks) . An RF bypass capacitor should be connected from the pin to ground with minimal trace length.	
6	CELL_LNA_EMIT	Ground directly to ground with minimum trace length.	
7	$\overline{\text{CELL}}$/PCS	Digital signal used for band selection: 0 = cellular (800 MHz), 1 = PCS (1900 MHz).	
8	$\overline{\text{FM}}$/CDMA	Digital signal used in cellular band for mode selection: 0 = AMPS, 1 = CDMA.	
9	VCO_VCC	Voltage supply to the VCO buffers. A bypass capacitor should be placed close to the device from pin 9 to ground with minimal trace length.	
10	VCO_ON	VCO control signal to turn VCO and PLL buffer ON/OFF during slotted paging modes, thereby increasing standby time.	
11	CELL_TANK–	Differential tank cellular band VCO pin. Care should be taken during the layout of the external tank circuit to prevent parasitic oscillations.	
12	CELL_TANK+	Differential tank cellular band VCO pin. Care should be taken during the layout of the external tank circuit to prevent parasitic oscillations.	
13	PCS_TANK–	Differential tank PCS band VCO pin. Care should be taken during the layout of the external tank circuit to prevent parasitic oscillations.	
14	PCS_TANK+	Differential tank PCS band VCO pin. Care should be taken during the layout of the external tank circuit to prevent parasitic oscillations.	
15	LOD	Linearity On Demand. It provides the bias control for the mixers, thereby reducing the chip current consumption at the expense of input IP3.	
16	PLL+	Differential buffered VCO output.	
17	PLL–	Differential buffered VCO output.	
18	SIF	Digital control signal for SIF selection: 1 = SIF, 0 = Normal.	
19	I–	I channel differential output.	
20	I+	I channel differential output.	
21	Q+	Q channel differential output.	
22	Q–	Q channel differential output.	

Table 1. CX74001 Pin Assignments and Signal Descriptions (2 of 2)

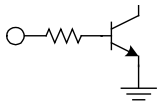
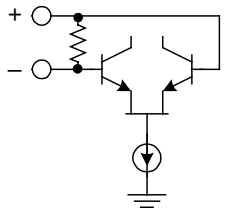
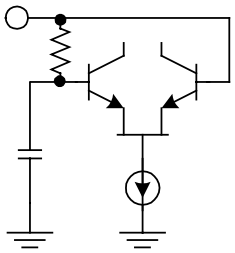
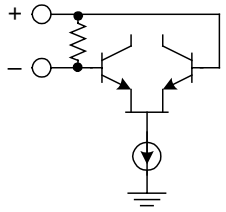
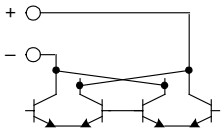
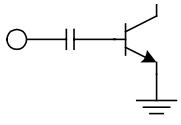
Pin #	Name	Description	Equivalent Circuit
23	$\overline{\text{SLEEP}}$	Digital signal used to activate the receiver ASIC: 0 = sleep, 1= enable.	
24	VGA_CONTROL	Analog gain control of the VGA. Typical 0.5 to 2.5V to control VGA dynamic range of greater than 90dB.	
25	VCC_IF	Voltage supply to VGA from I/Q demodulator stages and logic blocks. Supply should be bypassed to prevent signal modulation to the supply line.	
26	CDMA_VGA_IN–	CDMA differential VGA input	
27	CDMA_VGA_IN+	CDMA differential VGA input	
28	AMPS_VGA_IN	AMPS VGA input	
29	PCS_VGA_IN–	PCS differential VGA input	
30	PCS_VGA_IN+	PCS differential VGA input	
31	CDMA_MIX_OUT–	CDMA differential cellular mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
32	CDMA_MIX_OUT+	CDMA differential cellular mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
33	AMPS_MIX_OUT–	AMPS differential mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
34	AMPS_MIX_OUT+	AMPS differential mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
35	PCS_MIXER_OUT–	PCS differential mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
36	PCS_MIXER_OUT+	PCS differential mixer open collector output. VCC pull up inductor is required, and the output impedance is set by an external matching network.	
37	VCC_MIX	Voltage supply for the mixers. RF bypass capacitor should be close to pin with minimal trace length.	
38	PCS_LO	The local oscillator input for the PCS band mixer.	
39	CELL_LO	The local oscillator input for the cellular band mixer.	

Table 1. CX74001 Pin Assignments and Signal Descriptions (2 of 2)

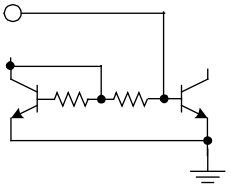
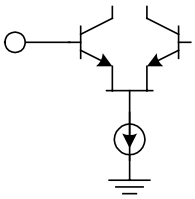
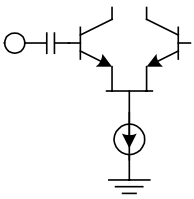
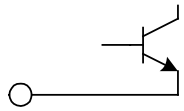
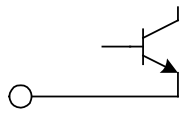
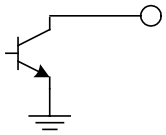
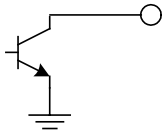
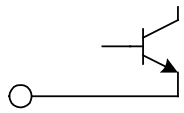
Pin #	Name	Description	Equivalent Circuit
40	PCSMIX_BYPASS	Low frequency bypass for the PCS mixer. Typically, a 47 nF is connected from pin to ground.	
41	PCS_MIX_IN	PCS mixer input. Requires AC coupling capacitor	
42	CELL_MIX_IN	Cellular mixer input	
43	RF_BIAS_RES	This sets the RF bias current. Typically, a 15 kΩ resistor is connected from the pin to ground.	
44	CELL_LNA_BIAS_RES	This sets the cellular LNA bias current. Typically, 27 kΩ is connected to ground.	
45	PCS_LNA_OUT	PCS LNA open collector output. VCC inductor pull up and external matching network are required.	
46	NC	No Connection.	
47	CELL_LNA_OUT	Cellular LNA open collector output. VCC inductor pull up and external matching network are required.	
48	PCS_LNA_BIAS_RES	This set the PCS LNA bias current. Typically, a 220 Ω resistor is connected from the pin to ground.	

Table 2. Mode Control Select Signal Switching

$\overline{\text{SLEEP}}$	$\overline{\text{CELL}}$/PCS	$\overline{\text{FM}}$	AMPS CHAIN	CELL CDMA CHAIN	PCS CDMA CHAIN
0	X	X	OFF (Note 1)	OFF (Note 1)	OFF (Note 1)
1	0	0	ON		
1	0	1		ON	
1	1	X			ON

Key: 0 = Low, OFF
1 = High, ON
X = Do not care

Notes: 1. All blocks except VCO, which is independently controlled by VCO_ON in this state.

Table 3. VCO_ON Control (SIF = 0)

VCO_ON	$\overline{\text{SLEEP}}$	$\overline{\text{CELL}}$/PCS	CELLULAR VCO	PCS VCO
1	X	0	ON	
1	X	1		ON
X	1	0	ON	
X	1	1		ON

Key: 0 = Low, OFF
1 = High, ON
X = Do not care

Table 4. SIF Control – Single IF ($\overline{\text{SLEEP}}$ = 1)

SIF	$\overline{\text{CELL}}$/PCS	$\overline{\text{FM}}$	VGA INPUT			VCO1 CELL	VCO2 PCS
			AMPS	CDMA	PCS		
0	0	0	ON			ON	
0	0	1		ON		ON	
0	1	X			ON		ON
1	0	0	ON			ON	
1	0	1		ON			ON
1	1	X		ON			ON

Key: 0 = Low, OFF
1 = High, ON
X = Do not care

Table 5. Logic Control for LNA Gain Step

LNA_CTRL0	LNA_CTRL1	AMPS	CELL CDMA	PCS CDMA
0	0	HIGH	HIGH	HIGH
1	0	MEDIUM (Note 1)	MEDIUM	BYPASS
0	1	BYPASS (Note 1)	BYPASS	HIGH
1	1	BYPASS (Note 1)	BYPASS	BYPASS

Key: 0 = Low, OFF
1 = High, ON
X = Do not care

Notes: 1. These modes are available but not used to meet the IS-98 Specifications.

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (V_{CC})	–0.3	+5.5	V
Input voltage range	–0.3	V_{CC}	V
LNA input power		+5	dBm
Power dissipation		600	mW
Ambient operating temperature	–30	+80	°C
Storage temperature	–40	+125	°C

Table 7. Recommended Operating Conditions

Parameter	Min	Typical	Max	Units
Supply voltage (V_{CC})	2.7	3.0	3.3	V
Operating temperature	–30	+25	+80	°C
Impedance of logic inputs		50		KΩ
VIL Logic Low Input Voltage	0.0		0.5	V
VIH Logic High Input Voltage	V_{CC} – 0.5		V_{CC}	V

Table 8. CX74001 Rx ASIC Electrical Specifications (1 of 3)
T_A = 25° C, V_{CC} = 3.0 V

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
800 MHz LNA CDMA						
High Gain				15.5		dB
Medium Gain				6		dB
Low Gain				–5.5		dB
Noise Figure @ High Gain				1.6		dB
Noise Figure @ Medium Gain				2.8		dB
Noise Figure @ Low Gain				6.4		
Input IP3 @ High Gain				5		dBm
Input IP3 @ Medium Gain				17.7		dBm
Input IP3 @ Low Gain				22		dBm
Reverse isolation				20		dB
Input return loss (869-894 MHz)				–15		dB
Output return loss (869-894 MHz)				–12		dB
Total supply current (adjustable)				8		mA
800 MHz LNA AMPS						
Gain @ 881 MHz				15		dB
Noise Figure				1.5		dB
Input IP3				0		dBm
Reverse Isolation				20		dB
Input return loss				–15		dB
Output return loss				–15		dB
Total supply current				4.5		mA
1900 MHz LNA						
Gain 1				15.5		dB
Gain 2				–4		dB
Noise Figure 1				1.9		dB
Noise Figure 2				4		
Input IP3 1				3		dBm
Input IP3 2				21		
Reverse Isolation				20		dB
Input return loss (1930-1990 MHz)				–10		dB
Output return loss (1930-1990 MHz)				–10		dB
Total supply current (Adjustable)				6.5		mA

Table 8. CX74001 Rx ASIC Electrical Specifications (2 of 3)
T_A = 25° C, V_{CC} = 3.0 V

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
800 MHz Mixer						
Conversion Gain (Power): CDMA Mode AMPS Mode				 10.5 11		 dB dB
Single-Sideband Noise Figure: CDMA Mode AMPS Mode				 8.5 8.5		 dB dB
P1dB @ Input: CDMA Mode AMPS Mode				 –2 –8		 dBm dBm
IP3 @ Input: CDMA Mode AMPS Mode				 7.5 3		 dBm dBm
Mixer RF Input Return Loss (869-894 MHz) (RF Port 1)				 –14		 dB
IF output Resistance: CDMA (differential) AMPS (differential)				 2000 1700		 Ohms Ohms
LO Input Power Level				–10		dBm
LO Input Return Loss (524-1149 MHz)				–12		dB
IF Frequency Range			50		300	MHz
LO/RF Isolation				20		dB
Total supply current (Mixer and LO Buffer) CDMA AMPS				 22.5 16		 mA mA
1900 MHz Mixer (1930-1990 MHz)						
Conversion Gain (Power)				10		dB
Single-Sideband Noise Figure				9.5		dB
P1dB @ Input				–7		dBm
IP3 @ Input				3		dBm
RF Input Return Loss (1930-1990 MHz)				–15		dB
LO Input Power Level				–10		dBm
LO Input Return Loss (1600-2300 MHz)				–11		dB
IF output resistance (differential)				1000		Ohms
IF Frequency Range			50		300	MHz
Total Supply Current (Mixer and LO Buffer)				22.5		mA

Table 8. CX74001 Rx ASIC Electrical Specifications (3 of 3)
T_A = 25° C, V_{CC} = 3.0 V

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
VGA and IQ Cascaded Performance						
Input Frequency Range (-2 dB)			50		300	MHz
Input impedance: CDMA (differential) AMPS(single-ended) PCS (differential)			 1000 1000 1000			 Ohms Ohms Ohms
Cascaded Noise Figure: @ Max Gain Min Gain				 5 50		 dB dB
VGA control range			0.5		2.5	Volts
Gain: Minimum Maximum (CDMA and PCS) Maximum (AMPS)				 57 63	 -36	 dB dB dB
Gain Slope				45		dB/V
Gain Slope Linearity (over any 6 dB segment)				±3		dB
Gain variation over Signal Bandwidth: CDMA and PCS (1 kHz-630 kHz) AMPS (100 Hz-15 kHz)				 0.2 0.2	 0.55 0.55	 dB dB
Gain variation over temperature and supply				±2		dB
Input 1 db compression at minimum gain				–10		dBm
OIP3 @ greater than 30 dB gain			5.5		6	dBm
Output Level: CDMA AMPS				 2. 5 2.75		 mVrms mVrms
Maximum Output			1.25			Vppd
Output Common Mode Voltage Variation Over Supply			0.9		1.8	V
I-Ib and Q-Qb DC Offset					6	mV
I-Q Gain Mismatch				0.2	0.3	dB
I-Q Phase Mismatch				2	4	degree
I-Q DC Offset					30	mV
Total supply current (VGA, IQ, dividers) CDMA / PCS AMPS				 10.5 14		 mA mA
Oscillator						
Frequency range			100		600	MHz
Phase Noise (fc = 200 MHz, unloaded Q = 20) @ 100 kHz offset				–117		dBc/Hz
Second harmonic distortion (application dependent)				–30		dBc
Total Supply Current				6		mA
Buffered VCO Output						
Frequency range			100		600	MHz
Output Level (peak differential)				150		mV
Output impedance (differential)				300		Ohms
Reverse isolation			–30		–40	dB
Total supply current				3		mA

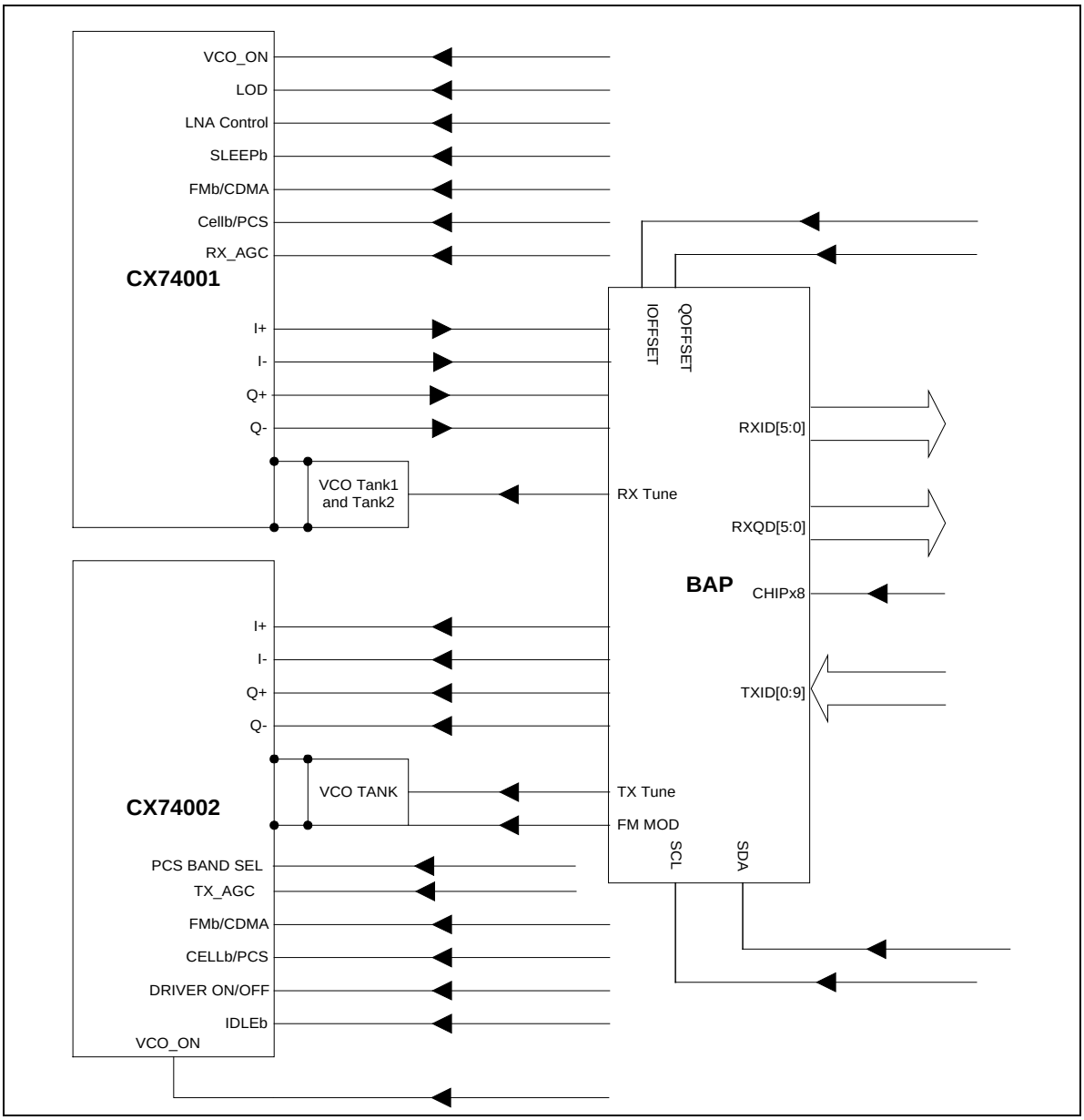


Figure 3. CX74001/CX74002 Interconnect Diagram with Baseband Analog Processor (BAP)

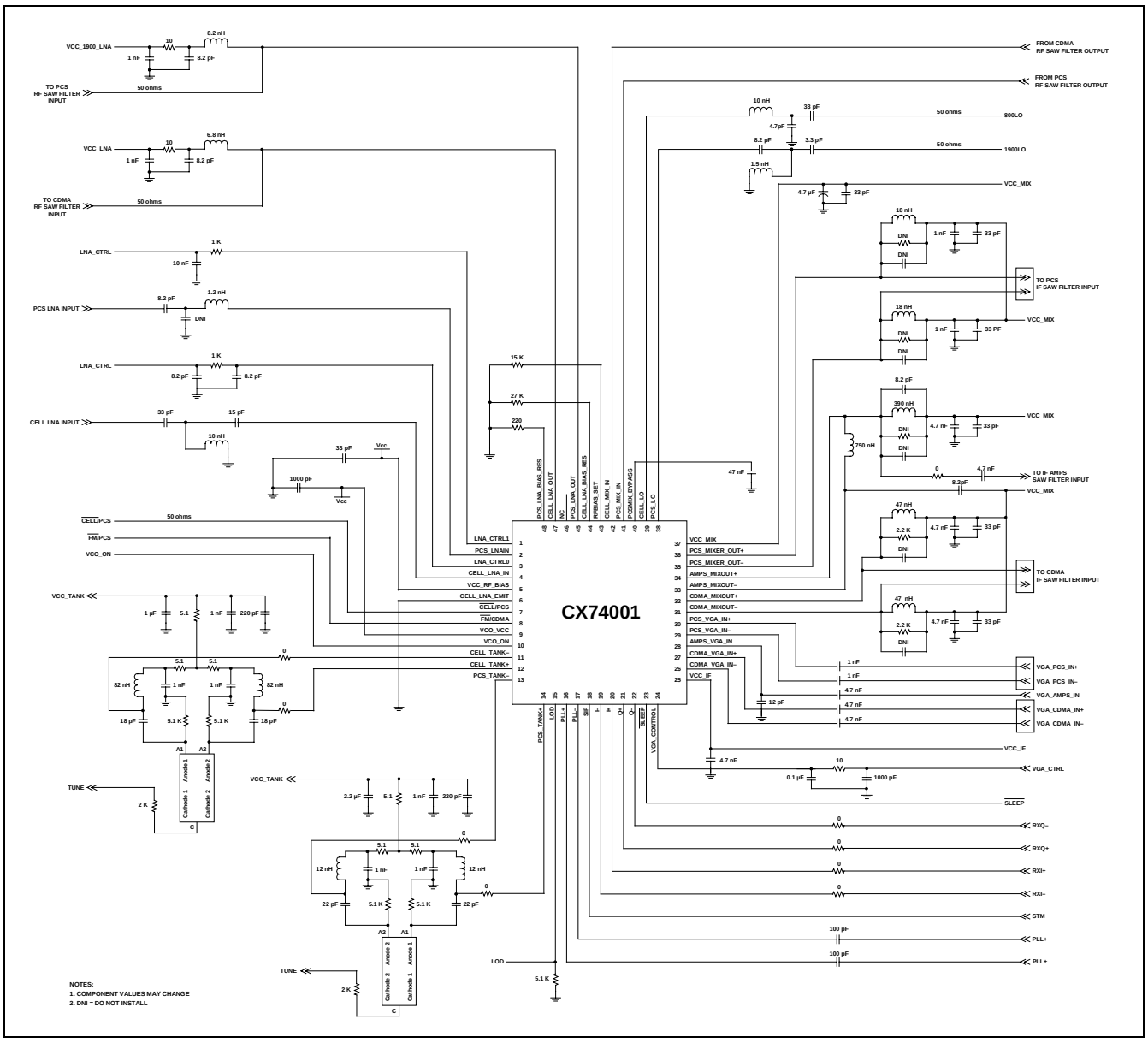
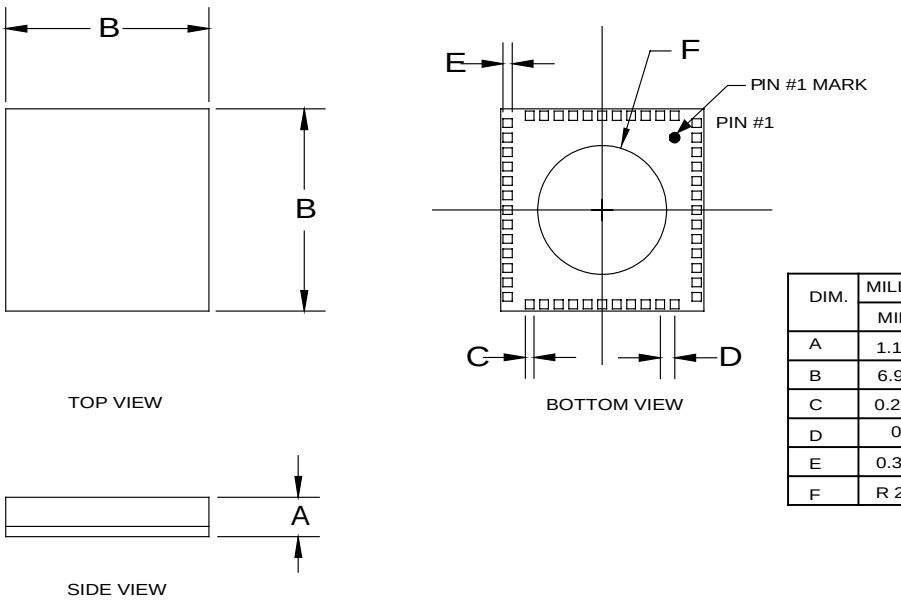


Figure 4. CX74001 Schematic Diagram



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.10	1.30	0.043	0.051
B	6.90	7.10	0.272	0.280
C	0.25	0.35	0.010	0.014
D	0.50 REF		0.020 REF	
E	0.31	0.41	0.012	0.016
F	R 2.225 REF		R 0.089 REF	

CNXT017

Figure 5. Package Dimensions - 48-pin RF-LGA™ Package

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
Rx ASIC	CX74001	

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