

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing and consumer applications.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- Consumer applications
- Desktop Voltage Regulator Module (VRM)
- Notebook Voltage Regulator Module (VRM)

### 1.4 Quick reference data

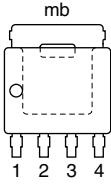
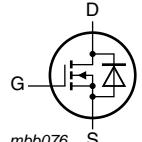
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 1</a>	[1]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 2</a>	-	-	74	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A};$	-	5	-	nC
$Q_{C(tot)}$	total gate charge	$V_{DS} = 12 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	19	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ }^\circ\text{C}$	-	2.43	3.5	$\text{m}\Omega$

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 <b>SOT669 (LFPAK)</b>	 <b>mbb076</b>

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package	Version
Name	Description	Version
PH3430AL	LFPAK	SOT669

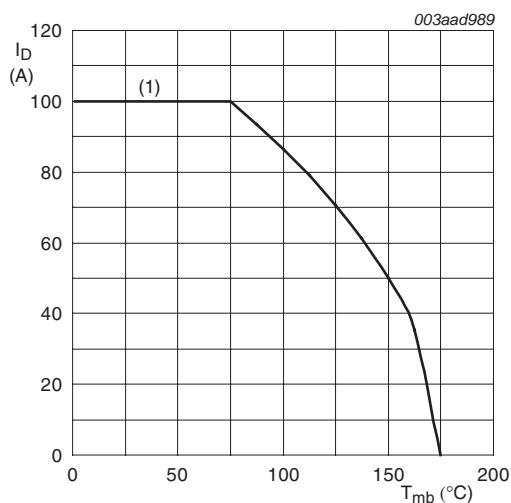
## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

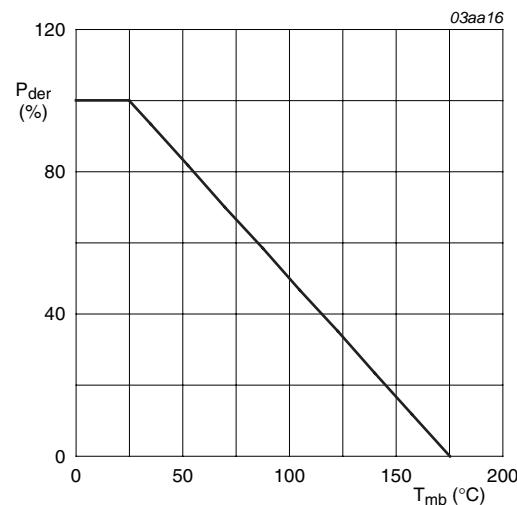
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100^\circ\text{C}$ ; see <a href="#">Figure 1</a>	[1]	-	86.5 A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 1</a>	[1]	-	100 A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 3</a>	-	447	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	74	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$ ;	[1]	-	100 A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$	-	447	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25^\circ\text{C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	54	mJ

[1] Continuous current is limited by package.



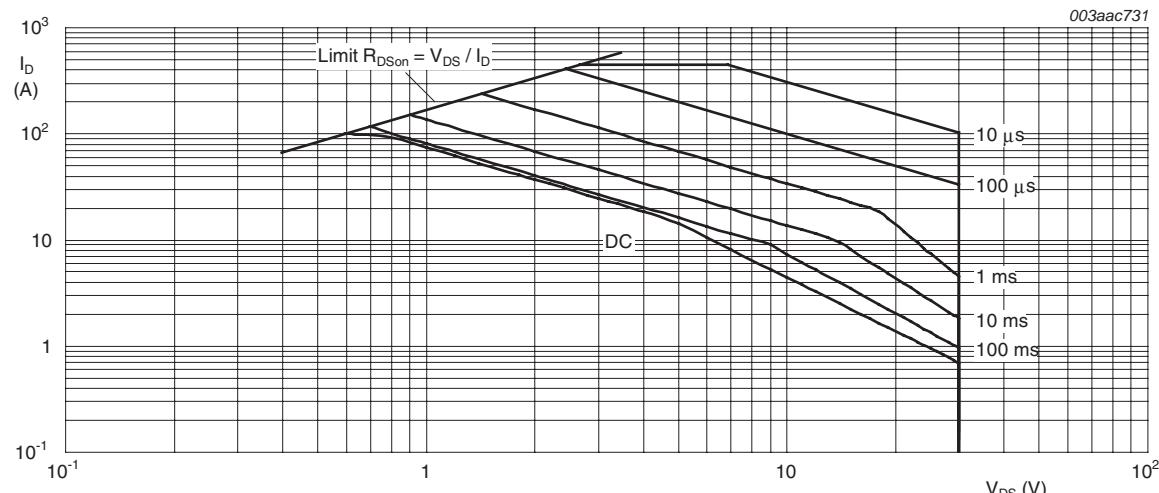
$V_{GS} \geq 10$  V; (1) Capped at 100 A due to package

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ C)} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



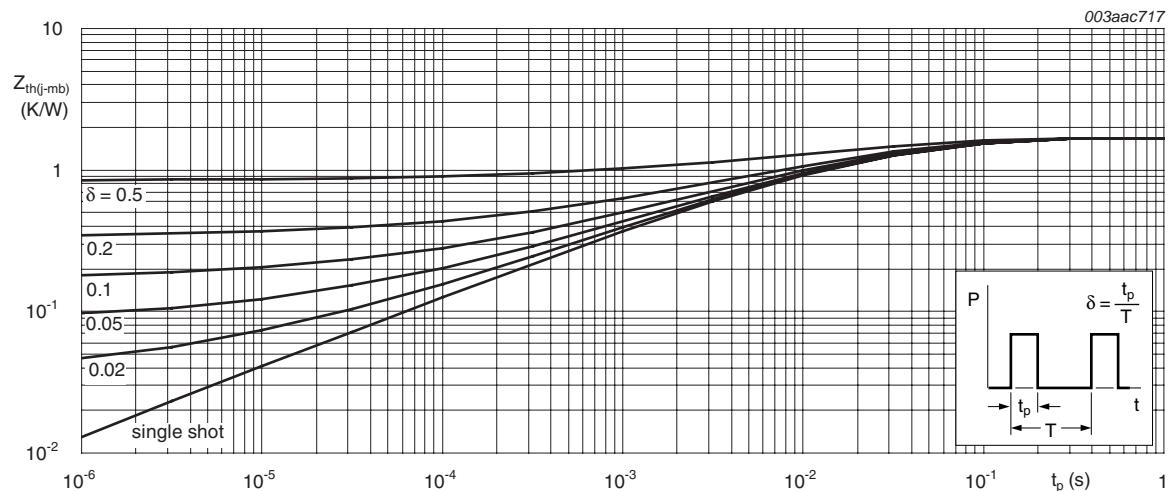
$T_{mb} = 25$  °C;  $I_{DM}$  is single pulse  
(1) Capped at 100 A due to package.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.62	1.68	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

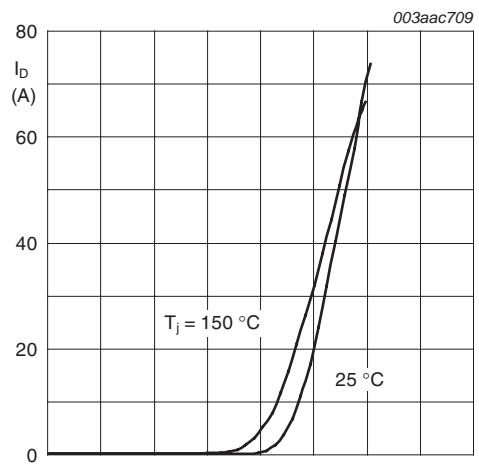
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; t_{av} = 100 \text{ ns}$	35	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> and <a href="#">12</a>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	0.65	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	3.37	4.61	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	-	6	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	2.43	3.5	$\text{m}\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	0.53	1.5	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	19	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	37	-	nC
		$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	41	-	nC
$Q_{GS}$	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	see <a href="#">Figure 14</a> and <a href="#">15</a>	-	4	-	nC
$Q_{GS(\text{th-pi})}$	post-threshold gate-source charge		-	2	-	nC
$Q_{GD}$	gate-drain charge		-	5	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$V_{DS} = 12 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	2.4	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2458	-	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	532	-	pF
$C_{rss}$	reverse transfer capacitance		-	252	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(\text{ext})} = 4.7 \Omega$	-	33	-	ns
$t_r$	rise time		-	50	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	45	-	ns
$t_f$	fall time		-	18	-	ns

Table 6. Characteristics ...continued

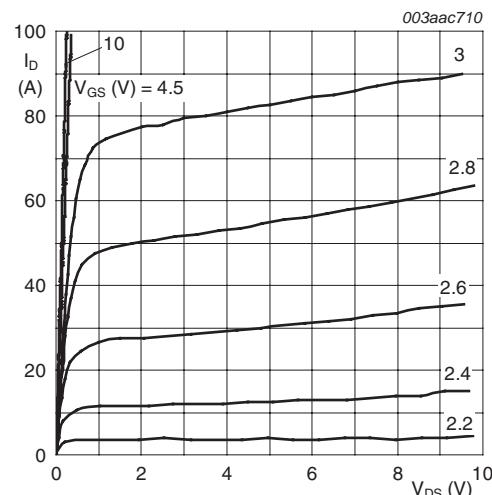
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see Figure 17	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$	-	37	-	ns
$Q_r$	recovered charge	$V_{DS} = 20 \text{ V}$	-	31	-	nC

[1] Tested to JEDEC standards where applicable.



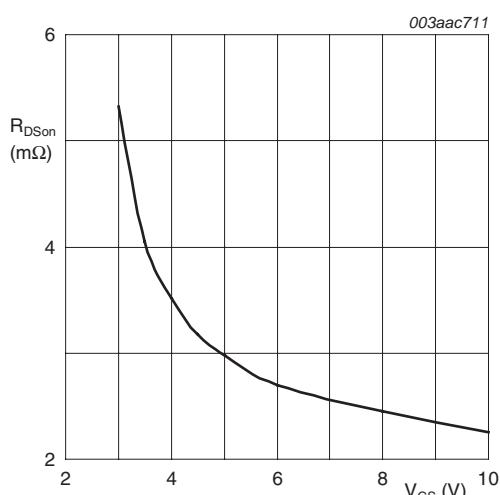
$V_{DS} = 10 \text{ V}$

Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values



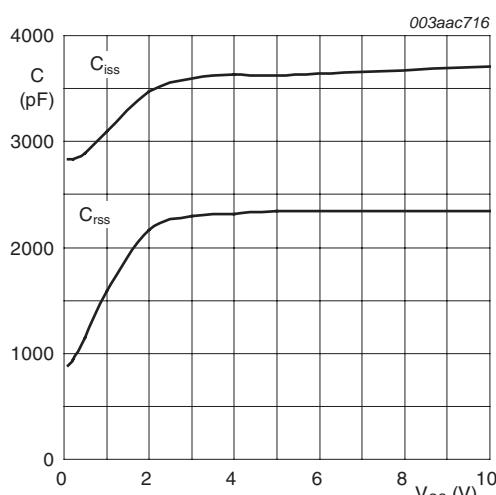
$T_j = 25 \text{ }^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



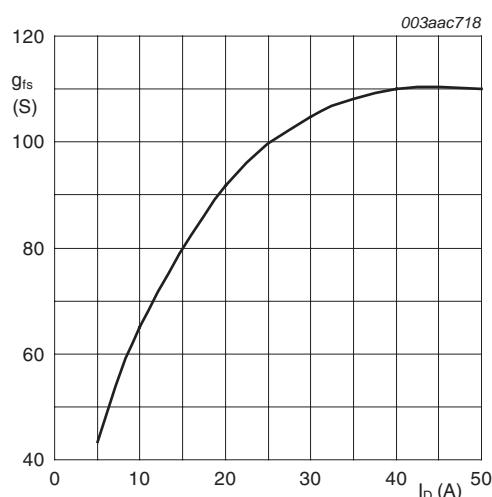
$T_j = 25 \text{ }^\circ\text{C}; I_D = 15 \text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



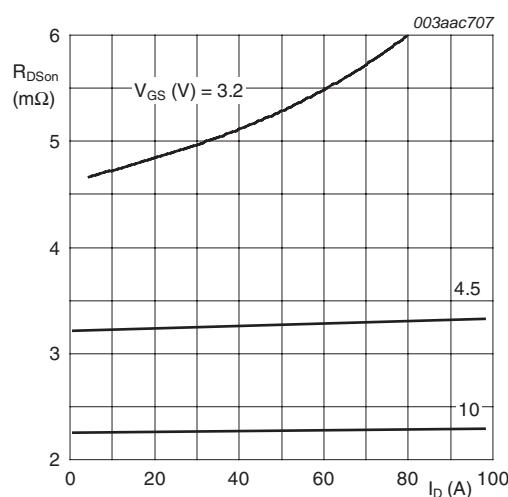
$V_{DS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



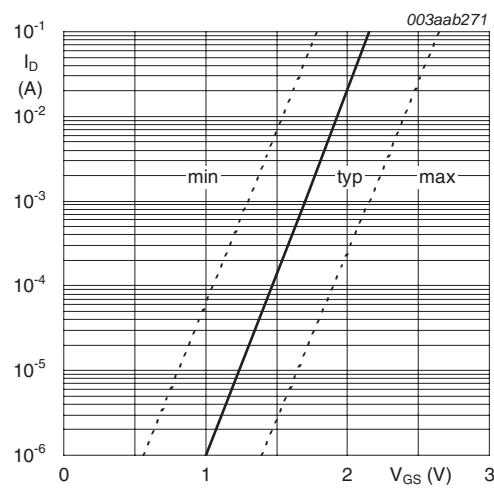
$T_j = 25^\circ C; V_{DS} = 15 V$

**Fig 9. Forward transconductance as a function of drain current; typical values**



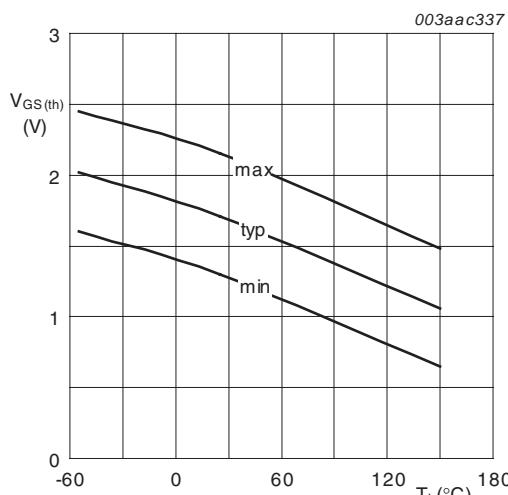
$T_j = 25^\circ C; t_p = 300 \mu s$

**Fig 10. Drain-source on-state resistance as a function of drain current; typical values**



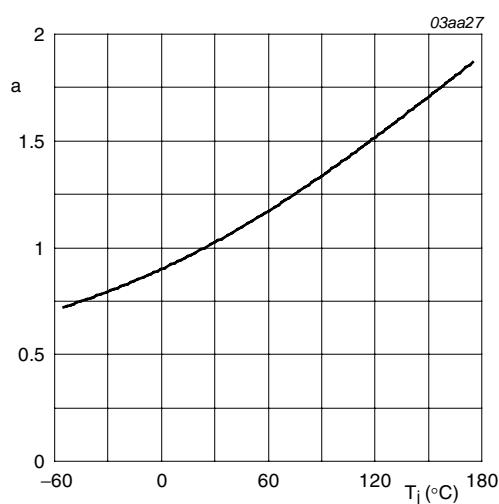
$T_j = 25^\circ C; V_{DS} = 5 V$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage**



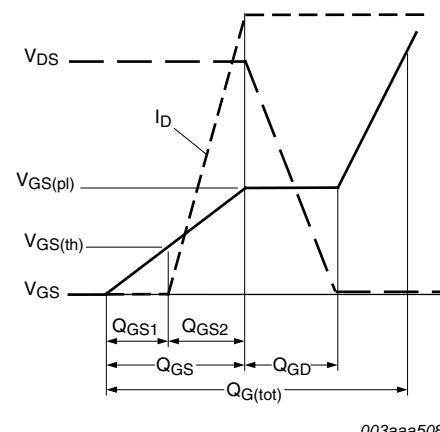
$I_D = 1 mA; V_{DS} = V_{GS}$

**Fig 12. Gate-source threshold voltage as a function of junction temperature**

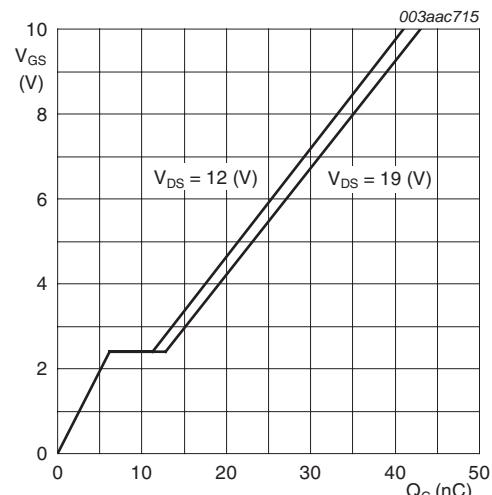


$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

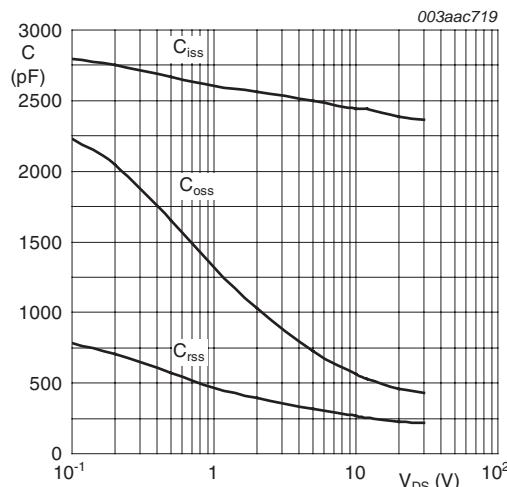


**Fig 14. Gate charge waveform definitions**



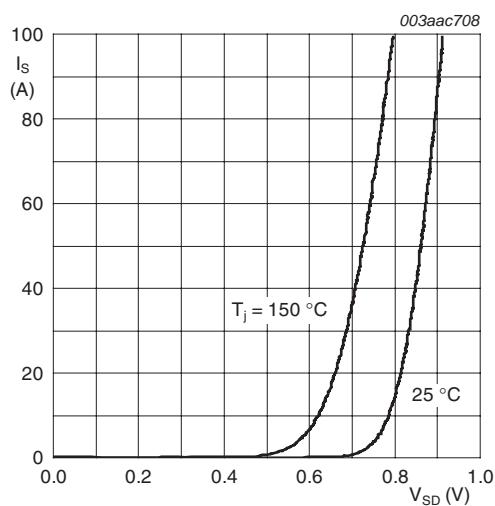
$T_j = 25^{\circ}C; I_D = 10A$

**Fig 15. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0V; f = 1MHz$

**Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$$V_{GS} = 0V$$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

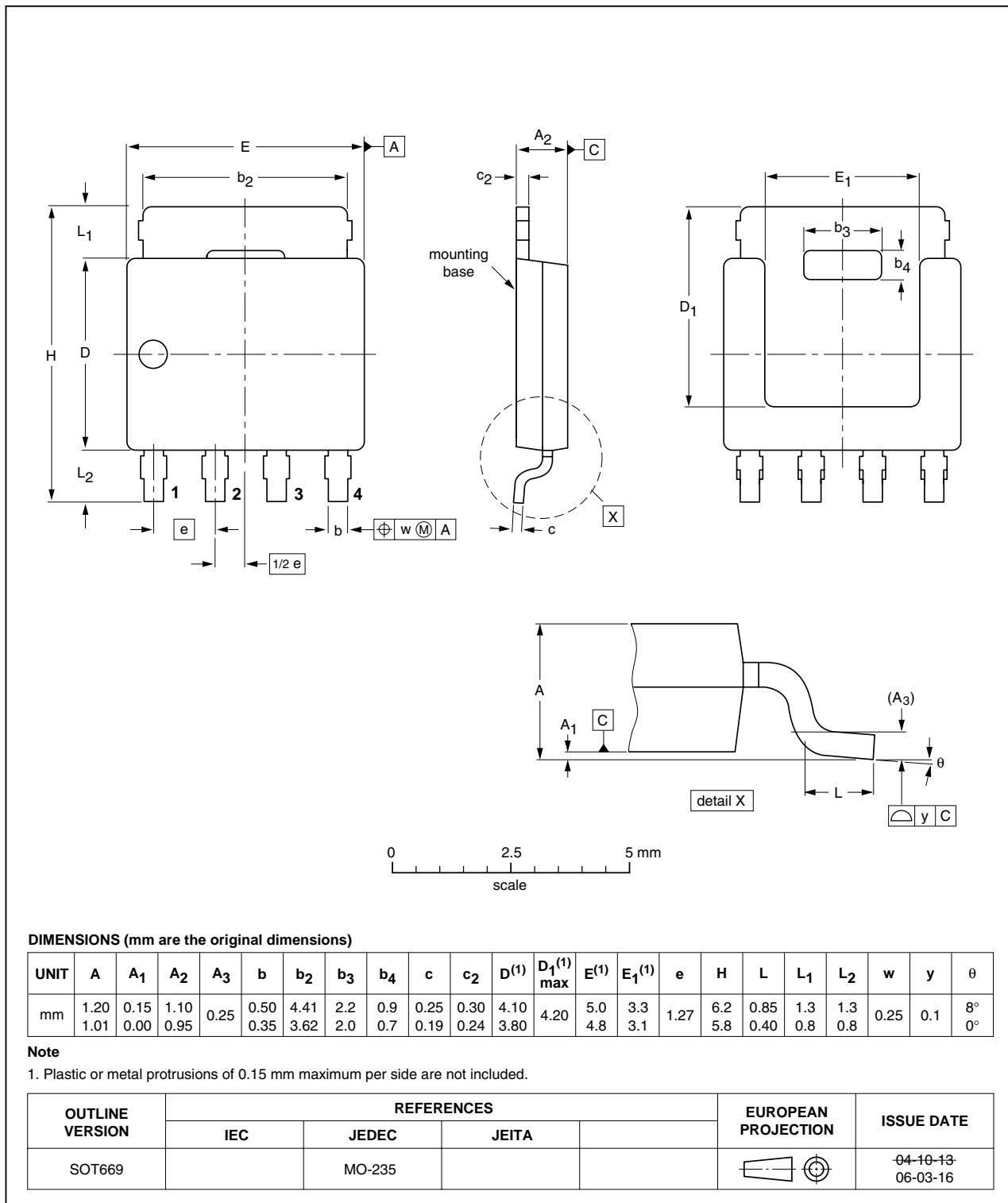


Fig 18. Package outline SOT669 (LFPAK)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH3430AL_5	20100114	Product data sheet	-	PH3430AL_4
Modifications:		• Various changes to content.		
PH3430AL_4	20091204	Product data sheet	-	PH3430AL_3
PH3430AL_3	20091203	Product data sheet	-	PH3430AL_2
PH3430AL_2	20091126	Product data sheet	-	PH3430AL_1
PH3430AL_1	20090121	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 9.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 9.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Non-automotive qualified products** — Unless the data sheet of an NXP Semiconductors product expressly states that the product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever

customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of NXP B.V.

## 10. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 11. Contents

---

<b>1</b>	<b>Product profile</b>	<b>1</b>
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
<b>2</b>	<b>Pinning information</b>	<b>2</b>
<b>3</b>	<b>Ordering information</b>	<b>2</b>
<b>4</b>	<b>Limiting values</b>	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b>	<b>4</b>
<b>6</b>	<b>Characteristics</b>	<b>5</b>
<b>7</b>	<b>Package outline</b>	<b>10</b>
<b>8</b>	<b>Revision history</b>	<b>11</b>
<b>9</b>	<b>Legal information</b>	<b>12</b>
9.1	Data sheet status	12
9.2	Definitions	12
9.3	Disclaimers	12
9.4	Trademarks	13
<b>10</b>	<b>Contact information</b>	<b>13</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP](#):

[PH3430AL,115](#)