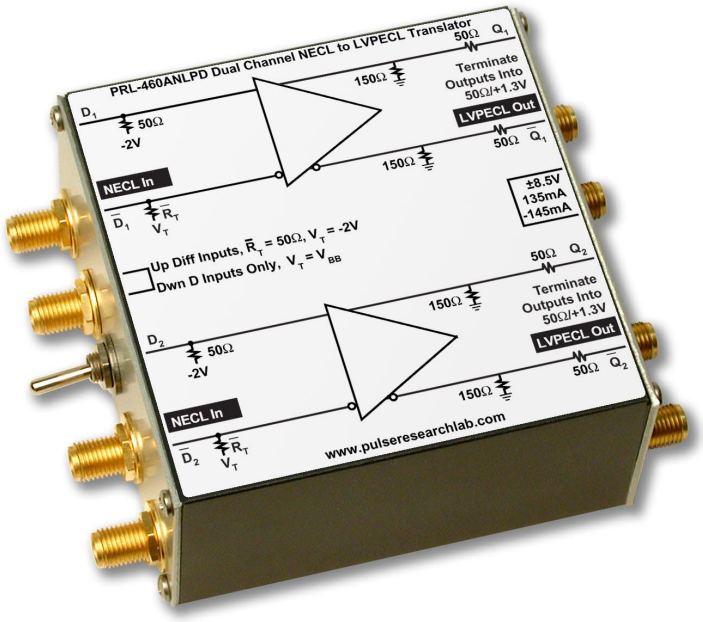
PRL-460ANPD DUAL CHANNEL NECL TO PECL TRANSLATOR
PRL-460ANLPD DUAL CHANNEL NECL TO LVPECL TRANSLATOR

APPLICATIONS

- **Converting Single Ended or Differential NECL Signals to Differential PECL or LVPECL Signals**
- **High Speed Digital Communications systems Testing**
- **High Speed SONET Clock Level Translation**

FEATURES

- **f_{max} > 2.2 GHz for PRL-460ANPD**
- **f_{max} > 1.25 GHz for PRL-460ANLPD**
- **750 ps t_r**
- **50 Ω/-2 V Input Terminations**
- **Single Ended or Differential Inputs**
- **Complementary PECL/LVPECL Outputs drive 50 Ω/V_{TT} Terminations, AC-coupled or Floating 50 Ω Loads**
- **DC coupled I/O's with SMA Connectors**
- **Self-contained 1.3 x 2.9 x 2.9-in. unit including an AC/DC Adapter**



PRL-460ANLPD
Dual Channel NECL to LVPECL Translator

DESCRIPTION

The PRL-460ANPD and PRL-460ANLPD are a dual channel NECL to PECL and NECL to LVPECL Logic Level Translator modules, respectively, intended for operation from DC to the GHz range. Maximum clock frequency is typically 2.5 GHz for the PRL-460ANPD and 1.5GHz for the PRL-460ANLPD. These modules can receive either single-ended or differential input signals, to be selected by a switch, but the complementary outputs must be used together. The short-circuit protection feature limits the output swing to 400 mV_{P-P} into a 50 Ω load, which is PECL/LVPECL compatible only if both outputs are used.

The complementary outputs of the PRL-460ANPD are designed for driving 50 Ω loads terminated to +3 V, and they can also drive AC coupled or floating 50 Ω loads. The complementary outputs of the PRL-460ANLPD are designed for driving 50 Ω loads terminated to +1.3 V, and they can also drive AC coupled or floating 50 Ω loads. These high speed translator modules facilitate testing and integration of high speed digital communications circuits and systems, where conversion of signals from NECL to PECL or LVPECL logic families is often required.

The PRL-460ANPD and PRL-460ANLPD inputs are designed to interface with NECL circuits operating with a -5.2 V or -3.3 V supply. In the differential input mode, both inputs D and $\overline{D}$ are terminated into 50 Ω/-2 V. In this mode, either one or both inputs can accept AC-coupled signals as well. In the single-input mode, signals should be connected to the D inputs only. Inputs $\overline{D}$ are switched internally to V_{BB}, nominally -1.3 V, and termination resistors $\overline{R}_T$'s for the $\overline{D}$ input channels are changed to 62 Ω. Block diagrams of the PRL-460ANPD and PRL-460ANLPD are shown in Fig. 1.

The PRL-460ANPD and PRL-460ANLPD are each supplied with a ±8.5 V AC/DC Adapter and housed in a 1.3 x 2.9 x 2.9-in. extruded aluminum enclosure.

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*SPECIFICATIONS (0º C ≤ T_A ≤ 35º C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50 Ω/+3 V for PRL-460NPD and 50 Ω/+1.3 V for PRL-460NLPD

Symbol	Parameter	PRL-460ANPD			PRL-460ANLPD			Unit
		Min	Typ	Max	Min	Typ	Max	
R_{in}	Input Resistance	49.5	50	50.5	49.5	50	50.5	Ω
R_{out}	Output Resistance		50			50		Ω
V_{TT}	"D" Input Termination Voltage (fixed)	-2.2	-2	-1.8	-2.2	-2	-1.8	V
V_T	"$\overline{D}$" Input Termination Voltage (variable)	-1.17/ -2.2	-1.3/ -2	-1.43/ -1.8	-1.17/ -2.2	-1.3/ -2	-1.43/ -1.8	V
VOL	Output Low Level	3.0	3.15	3.3	1.25	1.4	1.55	V
VOH	Output High Level	3.4	3.55	3.8	1.7	1.85	2	V
Vop-p	Output voltage swing, f ≤ 700 MHz Output voltage swing, f ≤ 550 MHz		400			280 400		mV
I_{DC}	DC Input Current		+125 -138	135 -145		+125 -138	135 -145	mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	103	115	127	V
t_{PLH}	Propagation Delay to output ↑		1.25			1.25		ns
t_{PHL}	Propagation Delay to output ↓		1.25			1.25		ns
t_r/t_f	Rise/Fall Times (20%-80%)*		500	750		600	850	ps
t_{SKEW}	Skew between any 2 outputs		50	120		50	120	ps
f_{max}	Max Clock Frequency	2.2	2.5		1.25	1.5		GHz
	Size	1.3 x 2.9 x 2.9			1.3 x 2.9 x 2.9			in.
	Weight		7			7		Oz

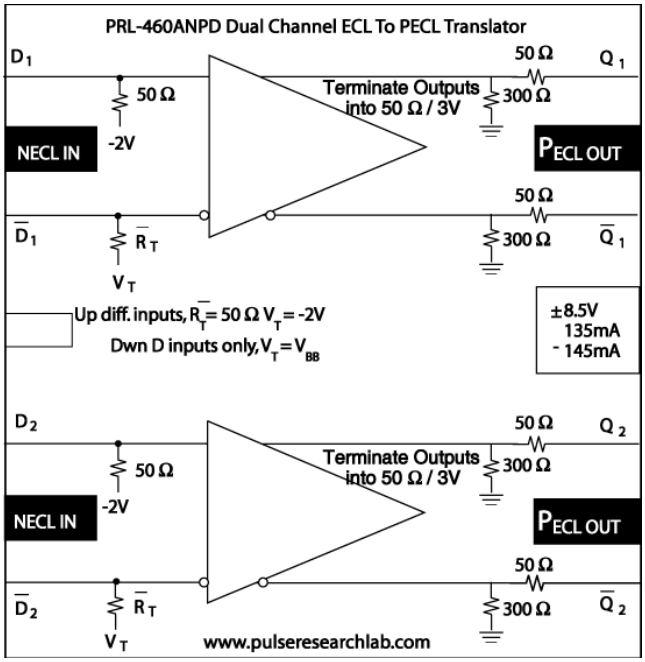

Fig. 1A PRL-460ANPD Block Diagram

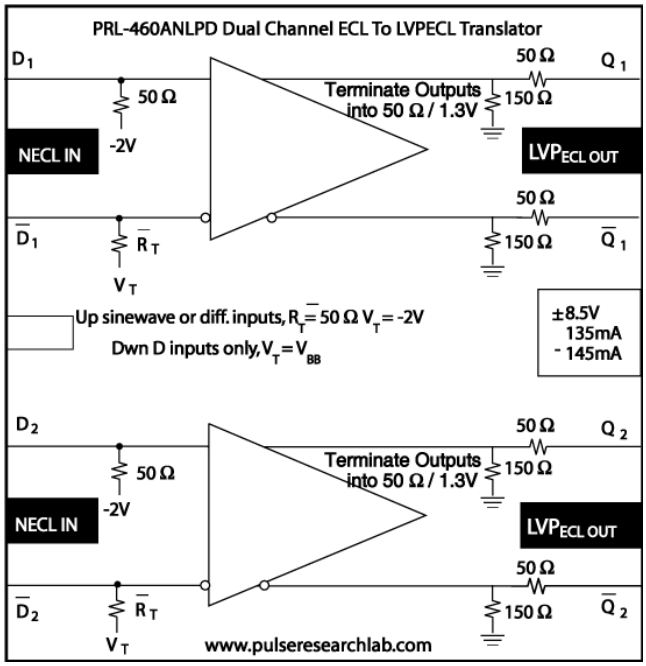

Fig. 1B PRL-460ANLPD Block Diagram

*An unused complementary output must be either terminated into 50 Ω/V_{TT} or AC coupled into a 50 Ω load; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-ACT-50 dual channel AC coupled 50 Ω Termination for terminating unused complementary outputs and the PRL-SC-104 DC Block or PRL-ACX-12dB AC coupled attenuator for connection of NECL signals to 50 Ω input oscilloscopes, if DC information is not needed. Otherwise, use the PRL-550NQ4X four channel NECL Terminators for the 50 Ω/V_{TT} termination and for connection of NECL signals to 50 Ω input oscilloscopes.