

74HC595-Q100; 74HCT595-Q100

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Rev. 4 — 20 March 2024

Product data sheet

1. General description

The 74HC595-Q100; 74HCT595-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset MR input. A LOW on MR will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- Complies with JEDEC standard no. 7A
- Input levels:
 - For 74HC595-Q100: CMOS level
 - For 74HCT595-Q100: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC595D-Q100 74HCT595D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC595PW-Q100 74HCT595PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC595BQ-Q100 74HCT595BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

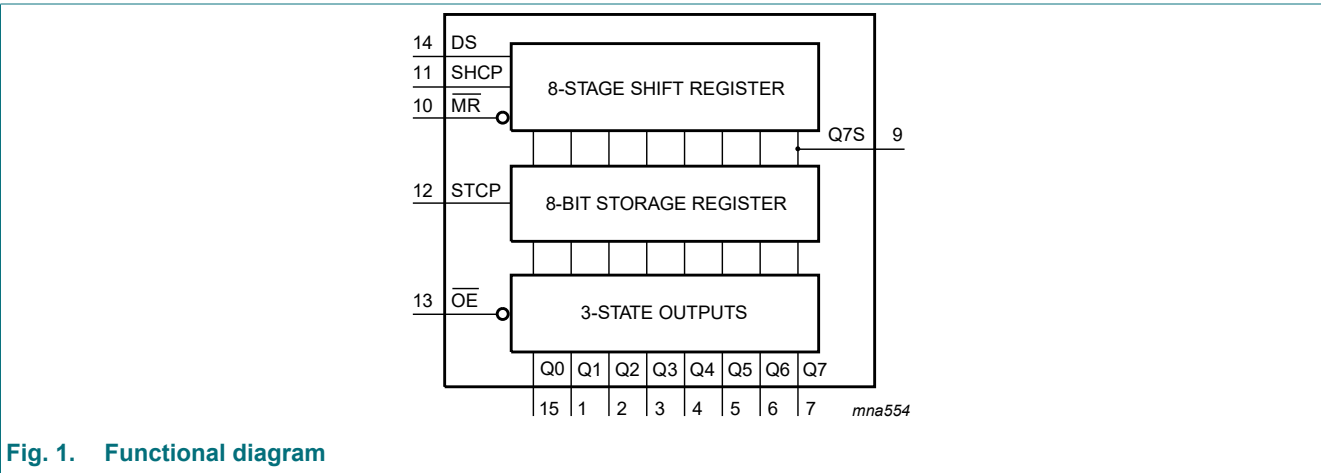


Fig. 1. Functional diagram

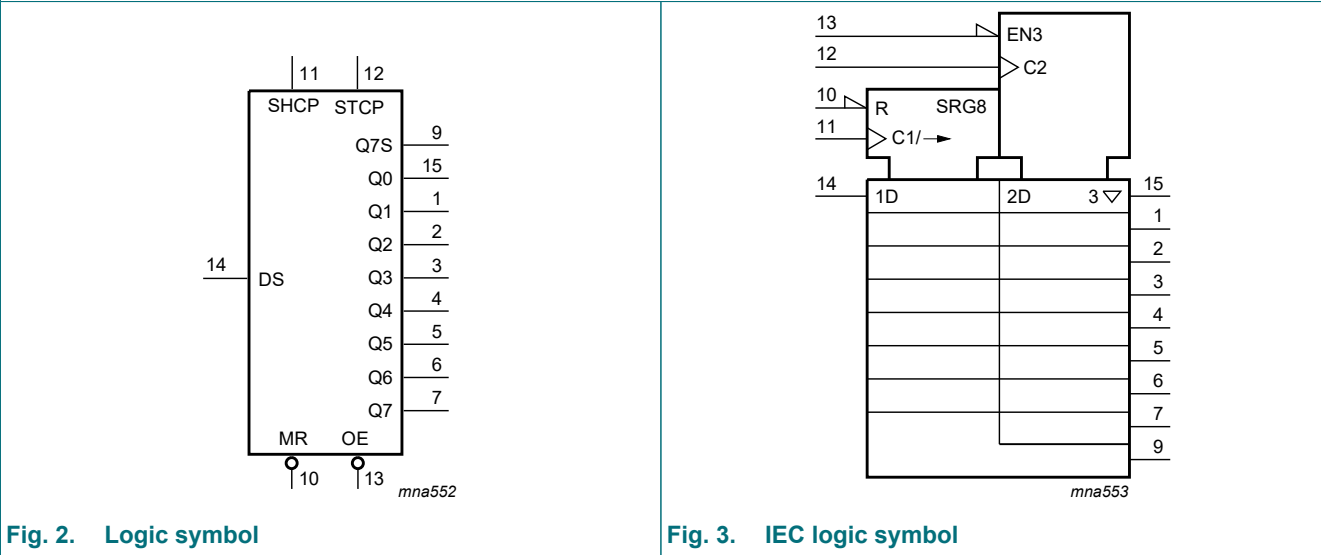
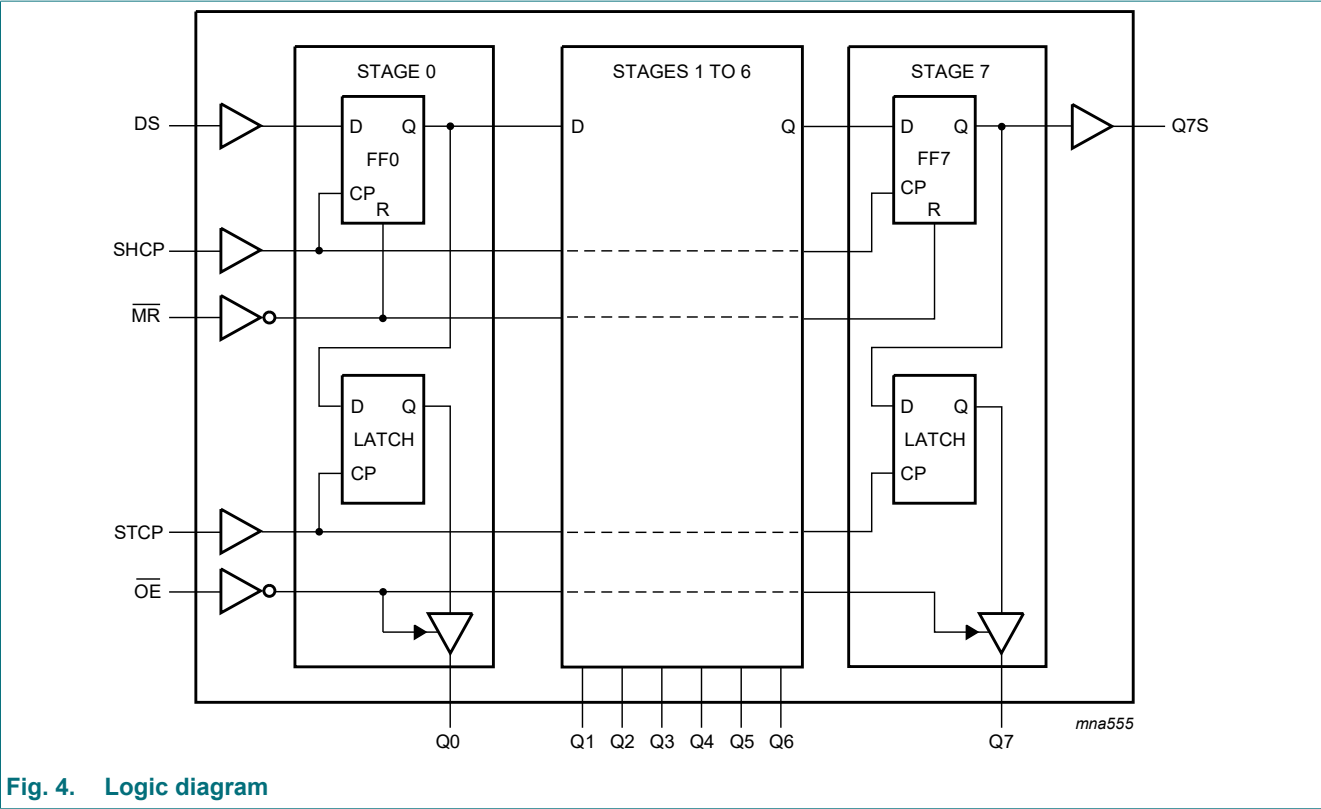


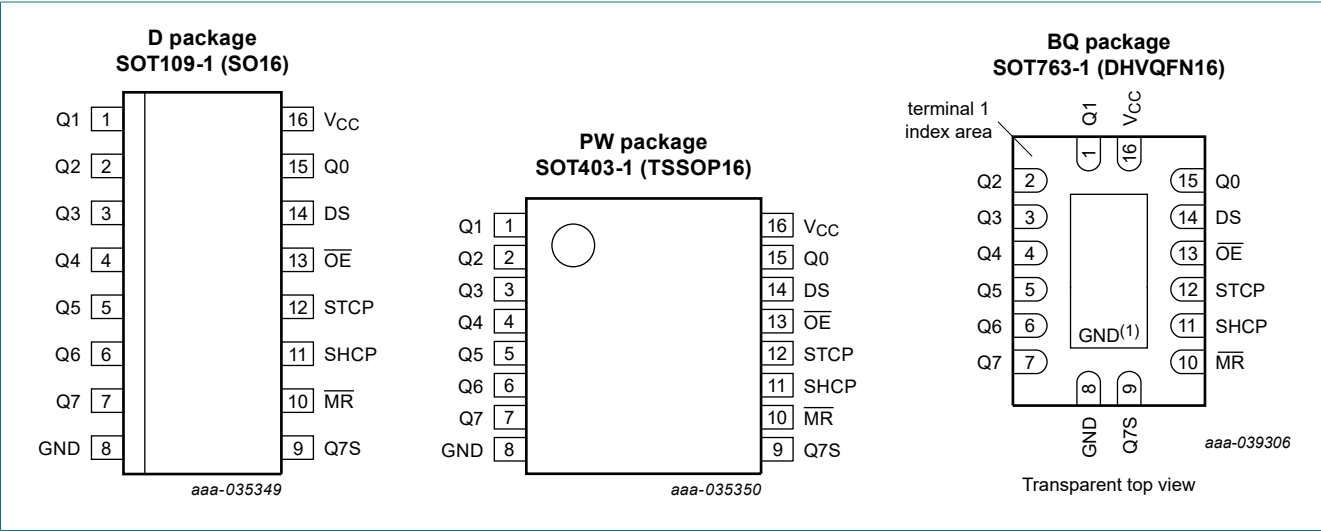
Fig. 2. Logic symbol

Fig. 3. IEC logic symbol



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

*H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition;
X = don't care; NC = no change; Z = high-impedance OFF-state.*

Control				Input	Output		Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

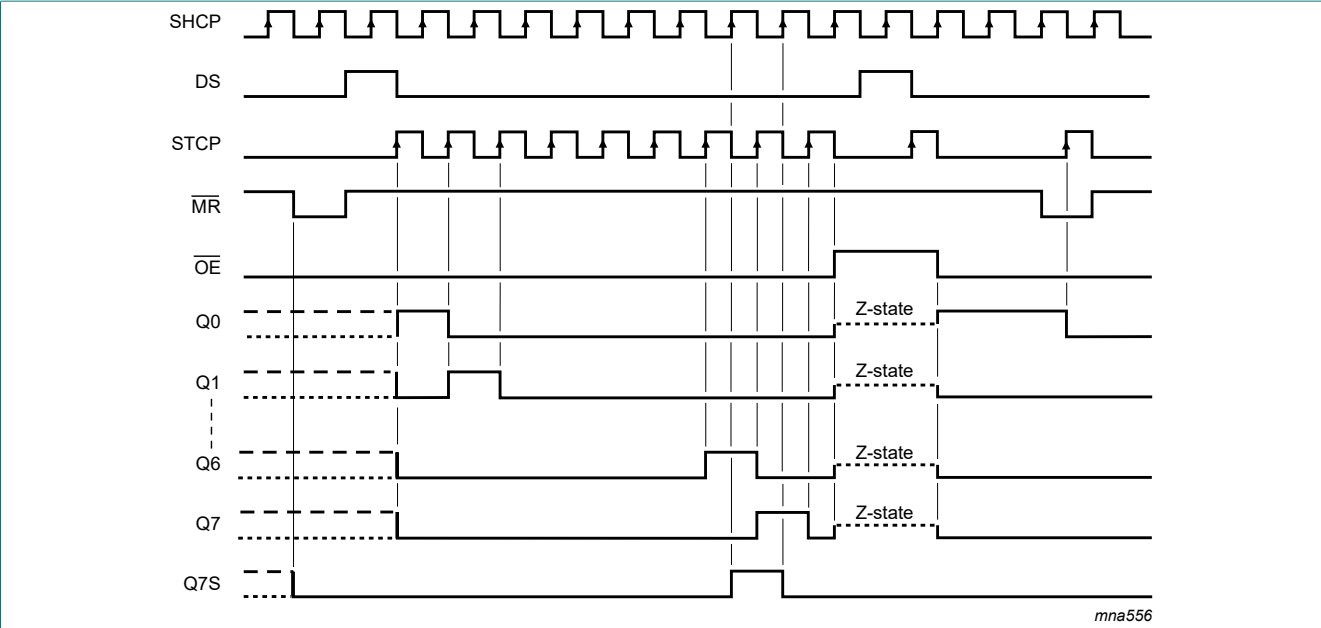


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$			
		pin Q7S	-	± 25	mA
		pins Qn	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SOT109-1; SOT403-1; SOT763-1 [1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC595-Q100			74HCT595-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC595-Q100								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		all outputs						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		Q7S output						
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
		Qn bus driver outputs						
		I _O = -6 mA; V _{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.34	5.81	-	5.2	-	V

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		all outputs						
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		Q7S output						
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
		Qn bus driver outputs						
I _I	input leakage current	I _O = 6 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	pF
74HCT595-Q100								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		all outputs						
		I _O = -20 µA	4.4	4.5	-	4.4	-	V
		Q7S output						
		I _O = -4 mA	3.84	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	Qn bus driver outputs						
		I _O = -6 mA	3.7	4.32	-	3.7	-	V
		V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		all outputs						
		I _O = 20 µA	-	0	0.1	-	0.1	V
V _{OL}	LOW-level output voltage	Q7S output						
		I _O = 4.0 mA	-	0.15	0.33	-	0.4	V
		Qn bus driver outputs						
		I _O = 6.0 mA	-	0.16	0.33	-	0.4	V

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND	-	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; other inputs at V _{CC} or GND; I _O = 0 A; V _I = V _{CC} - 2.1 V; V _{CC} = 4.5 V to 5.5 V						
		pins $\overline{\text{MR}}$, SHCP, STCP, $\overline{\text{OE}}$	-	150	675	-	735	µA
		pin DS	-	25	113	-	123	µA
C _I	input capacitance		-	3.5	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HC595-Q100										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]								
		V _{CC} = 2 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 6 V	-	15	27	-	34	-	41	ns
		STCP to Qn; see Fig. 7 [2]								
		V _{CC} = 2 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
t _{PHL}	HIGH to LOW propagation delay	V _{CC} = 6 V	-	16	30	-	37	-	45	ns
		MR to Q7S; see Fig. 9								
		V _{CC} = 2 V	-	47	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	17	35	-	44	-	53	ns
t _{en}	enable time	V _{CC} = 6 V	-	14	30	-	37	-	45	ns
		OE to Qn; see Fig. 10 [3]								
		V _{CC} = 2 V	-	47	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	17	30	-	38	-	45	ns
t _{dis}	disable time	V _{CC} = 6 V	-	14	26	-	33	-	38	ns
		OE to Qn; see Fig. 10 [4]								
		V _{CC} = 2 V	-	41	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V _{CC} = 6 V	-	12	27	-	33	-	38	ns

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _W	pulse width	SHCP HIGH or LOW; see Fig. 6								
		V _{CC} = 2 V	75	17	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V _{CC} = 6 V	13	5	-	16	-	19	-	ns
		STCP HIGH or LOW; see Fig. 7								
		V _{CC} = 2 V	75	11	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	4	-	19	-	22	-	ns
		V _{CC} = 6 V	13	3	-	16	-	19	-	ns
		MR LOW; see Fig. 9								
		V _{CC} = 2 V	75	17	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V _{CC} = 6 V	13	5	-	16	-	19	-	ns
t _{su}	set-up time	DS to SHCP; see Fig. 8								
		V _{CC} = 2 V	50	11	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	4	-	13	-	15	-	ns
		V _{CC} = 6 V	9	3	-	11	-	13	-	ns
		SHCP to STCP; see Fig. 8								
		V _{CC} = 2 V	75	22	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	8	-	19	-	22	-	ns
		V _{CC} = 6 V	13	7	-	16	-	19	-	ns
t _h	hold time	DS to SHCP; see Fig. 8								
		V _{CC} = 2 V	3	-6	-	3	-	3	-	ns
		V _{CC} = 4.5 V	3	-2	-	3	-	3	-	ns
		V _{CC} = 6 V	3	-2	-	3	-	3	-	ns
t _{rec}	recovery time	MR to SHCP; see Fig. 9								
		V _{CC} = 2 V	50	-19	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	-7	-	13	-	15	-	ns
		V _{CC} = 6 V	9	-6	-	11	-	13	-	ns
f _{max}	maximum frequency	SHCP or STCP; see Fig. 6 and Fig. 7								
		V _{CC} = 2 V	9	30	-	4.8	-	4	-	MHz
		V _{CC} = 4.5 V	30	91	-	24	-	20	-	MHz
		V _{CC} = 6 V	35	108	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [5] [6]	-	115	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HCT595-Q100; V _{CC} = 4.5 V to 5.5 V										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]	-	25	42	-	53	-	63	ns
		STCP to Qn; see Fig. 7 [2]	-	24	40	-	50	-	60	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q7S; see Fig. 9	-	23	40	-	50	-	60	ns
t _{en}	enable time	OE to Qn; see Fig. 10 [3]	-	21	35	-	44	-	53	ns
t _{dis}	disable time	OE to Qn; see Fig. 10 [4]	-	18	30	-	38	-	45	ns
t _W	pulse width	SHCP HIGH or LOW; see Fig. 6	16	6	-	20	-	24	-	ns
		STCP HIGH or LOW; see Fig. 7	16	5	-	20	-	24	-	ns
		MR LOW; see Fig. 9	20	8	-	25	-	30	-	ns
t _{su}	set-up time	DS to SHCP; see Fig. 8	16	5	-	20	-	24	-	ns
		SHCP to STCP; see Fig. 8	16	8	-	20	-	24	-	ns
t _h	hold time	DS to SHCP; see Fig. 8	3	-2	-	3	-	3	-	ns
t _{rec}	recovery time	MR to SHCP; see Fig. 9	10	-7	-	13	-	15	-	ns
f _{max}	maximum frequency	SHCP and STCP; see Fig. 6 and Fig. 7	30	52	-	24	-	20	-	MHz
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} - 1.5 V [5] [6]	-	130	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

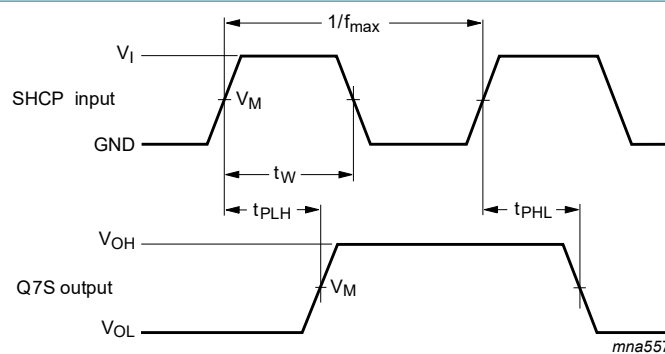
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

[6] All 9 outputs switching.

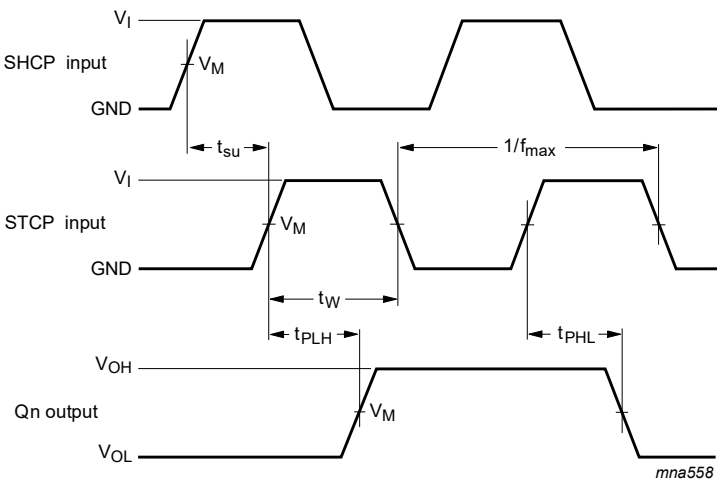
11.1. Waveforms and test circuit



Measurement points are given in Table 8.

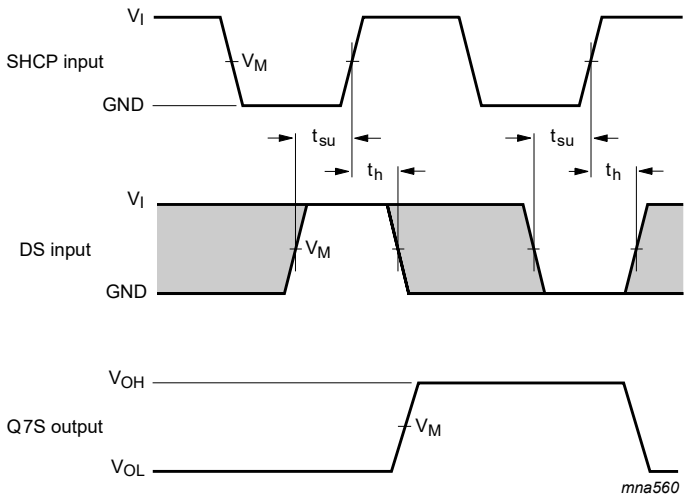
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Shift clock pulse, maximum frequency and input to output propagation delays



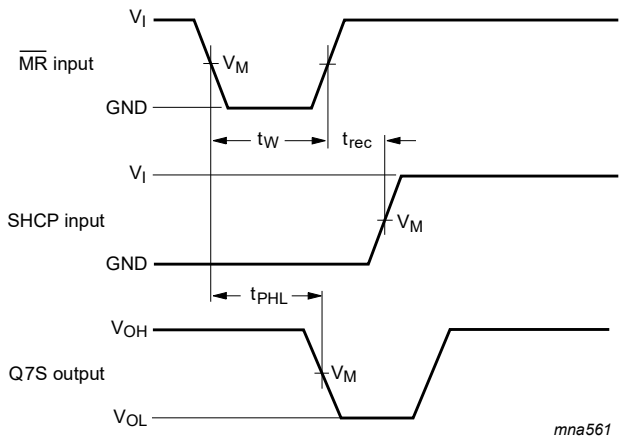
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Storage clock to output propagation delays



Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Data set-up and hold times



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Master reset to output propagation delays

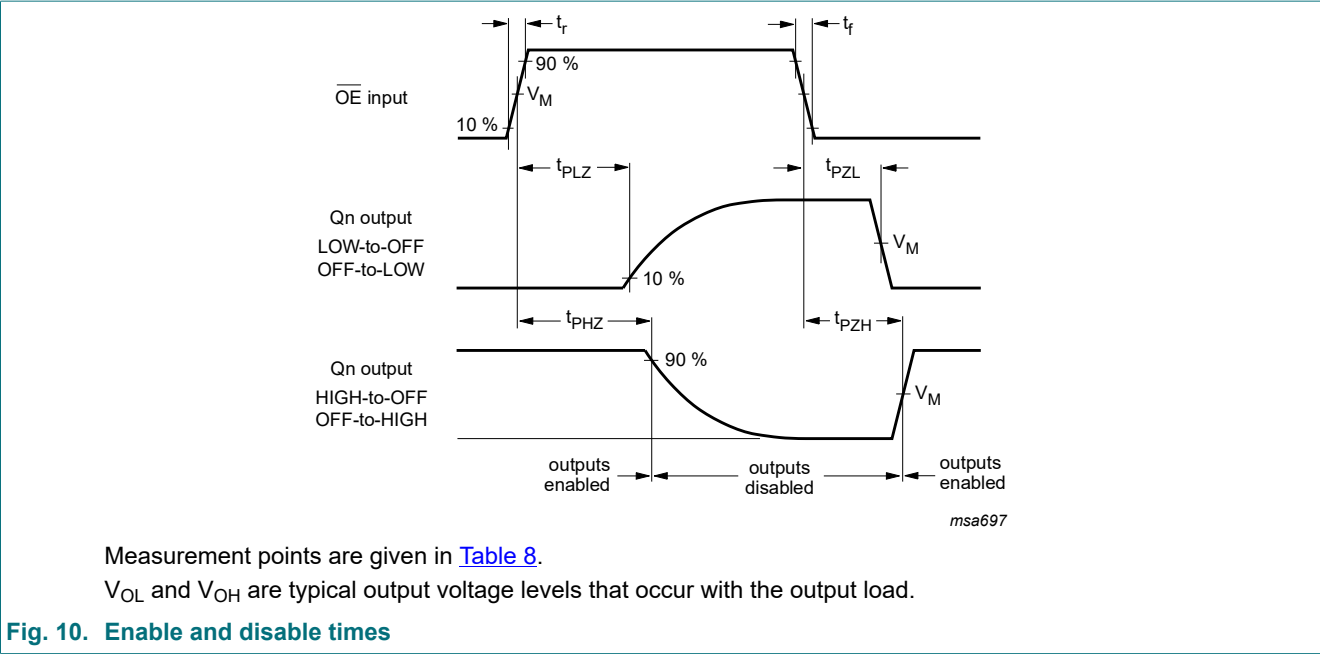
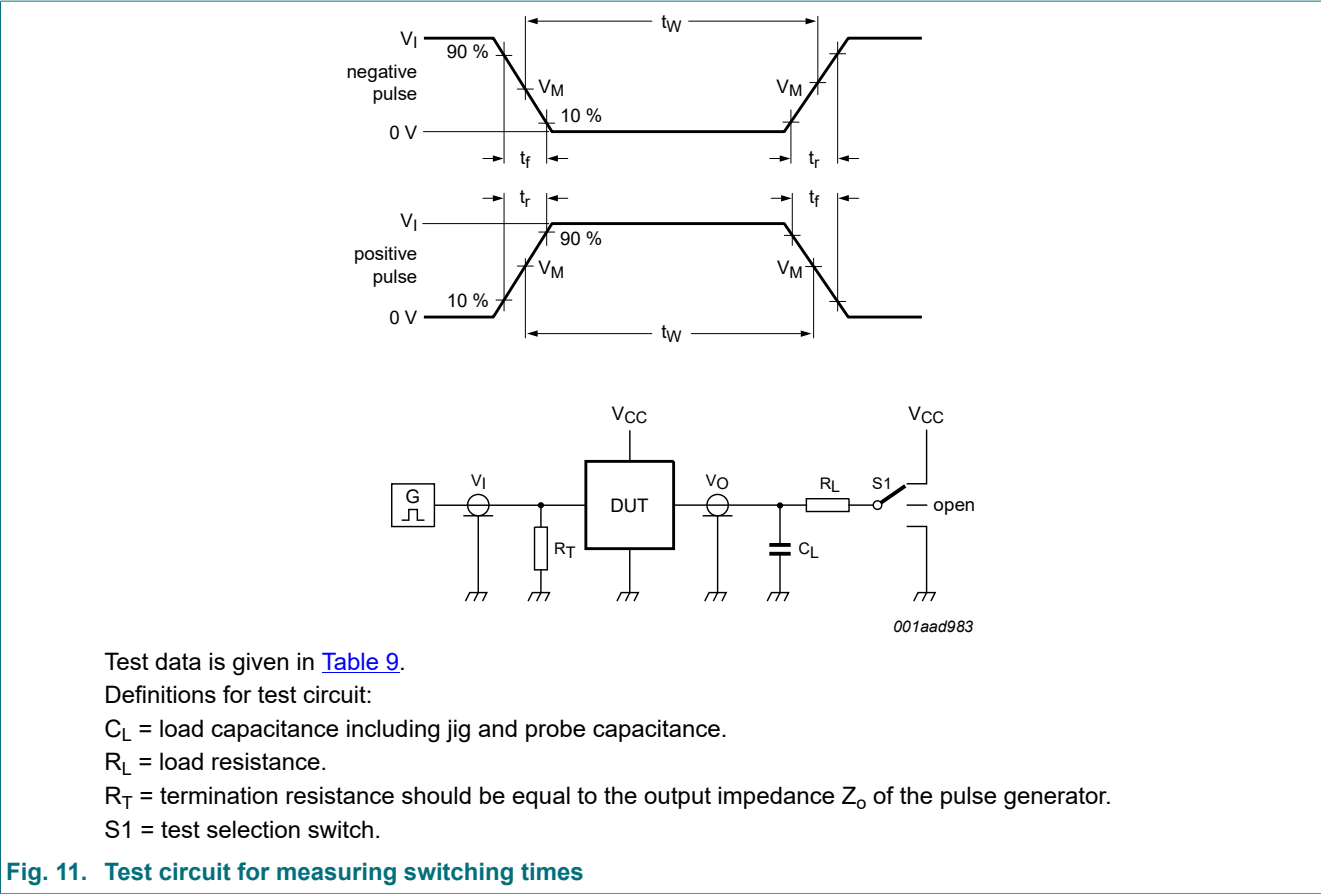


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC595-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74HCT595-Q100	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

- C_L = load capacitance including jig and probe capacitance.
- R_L = load resistance.
- R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.
- S1 = test selection switch.

Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595-Q100	V_{CC}	6 ns	50 pF	1 k Ω	open	GND	V_{CC}
74HCT595-Q100	3 V	6 ns	50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

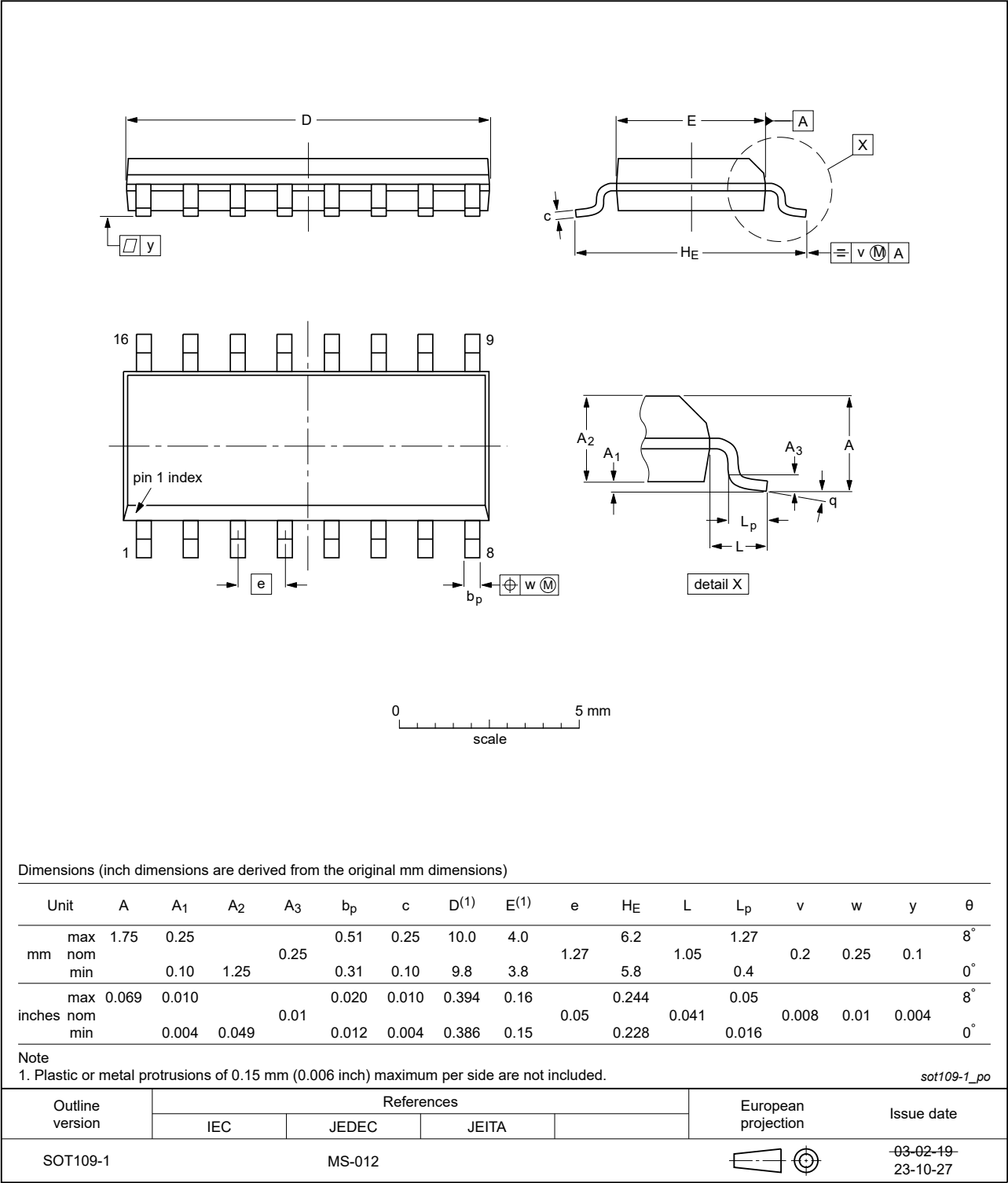


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

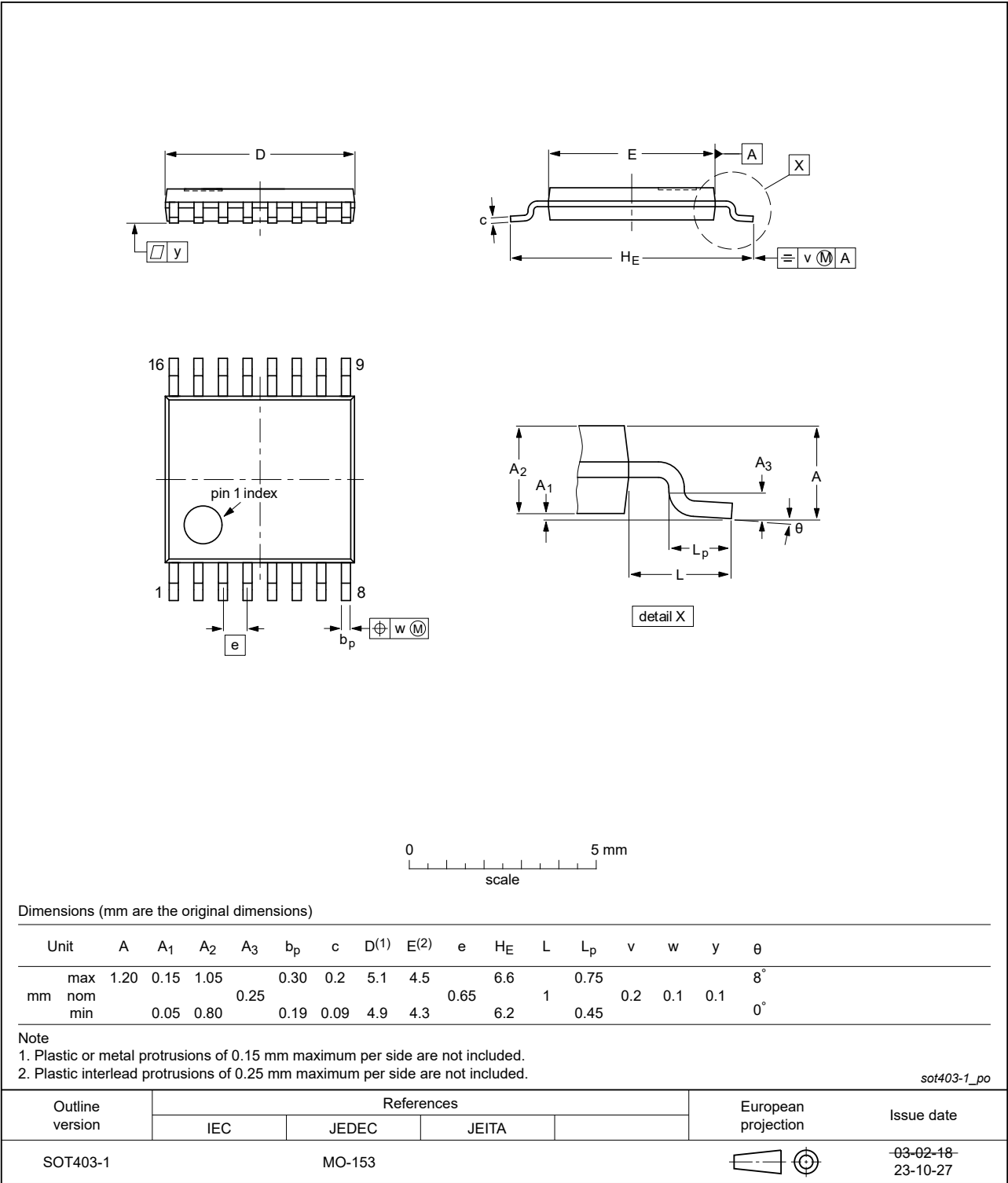


Fig. 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

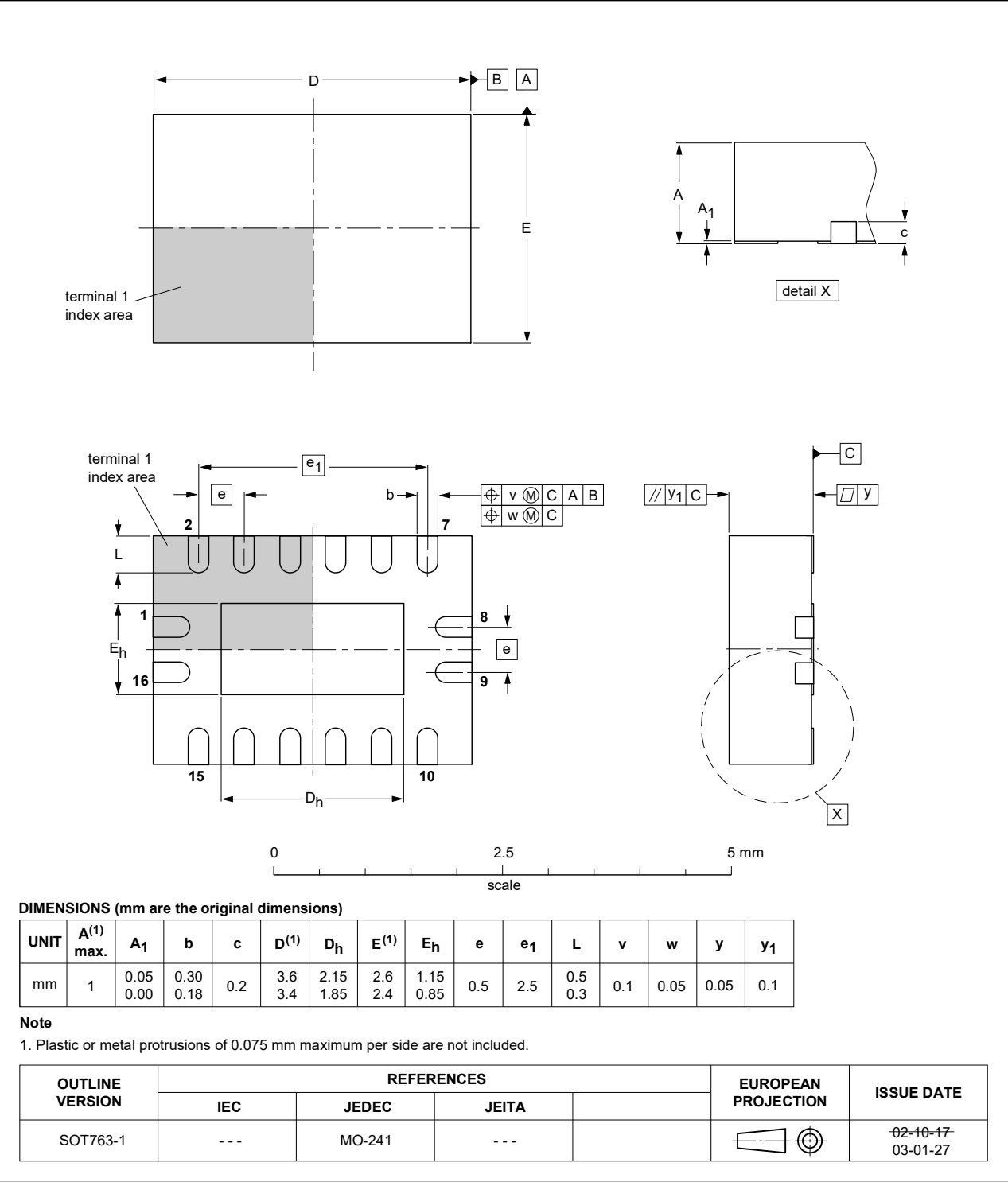


Fig. 14. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT595_Q100 v.5	20240320	Product data sheet	-	74HC_HCT595_Q100 v.4
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 12 and Fig. 13: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74HC_HCT595_Q100 v.4	20200311	Product data sheet	-	74HC_HCT595_Q100 v.3
Modifications:	- Type numbers 74HC595DB-Q100 and 74HCT595DB-Q100 (SOT338-1) removed. - Section 2 updated. - Table 4: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT595_Q100 v.3	20170228	Product data sheet	-	74HC_HCT595_Q100 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT595_Q100 v.2	20130410	Product data sheet	-	74HC_HCT595_Q100 v.1
Modifications:	Type numbers 74HC595DB-Q100 and 74HCT595DB-Q100 added.			
74HC_HCT595_Q100 v.1	20120802	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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