ES_LPC177x/8x

Errata sheet LPC177x/8x

Rev. 3.4 — 26 November 2013 | Errata sheet

Document information

Info	Content
Keywords	LPC1788FBD208, LPC1788FET208, LPC1788FET180, LPC1788FBD144, LPC1787FBD208, LPC1786FBD208, LPC1785FBD208, LPC1778FBD208, LPC1778FET208, LPC1778FET180, LPC1778FBD144, LPC1777FBD208, LPC1776FBD208, LPC1776FET180, LPC1774FBD208, LPC1774FBD144, LPC177x/8x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
3.4	20131126	• Added IBAT.1.
3.3	20130214	• Added I2C.1.
3.2	20121207	• Added ETHERNET.1.
3.1	20121109	• Added Rev 'F'.
3	20120901	• Added PBOOST.1.
2.4	20120612	• Added APB.1.
2.3	20120503	• Added Note.1.
2.2	20120117	• Added ADC.2.
2.1	20111101	• Added Rev 'E'.
2	20110901	• Added ISP.1. • Added Rev 'A'.
1.1	20110601	• Added WDT.1. • Added DPD.1. • Added USART.
1	20110525	• Initial version.

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1. Product identification

The LPC177x/8x devices typically have the following top-side marking:

LPC17xxXXX

xxxxxxx

xxYYWWR[x]

The last digit in the last line (field ‘R’) will identify the device revision. Note: Pre-production parts are marked differently and this system does not apply. This Errata Sheet covers the following revisions of the LPC177x/8x:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision
‘E’	Third device revision
‘F’	Fourth device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier[1]	Detailed description
ADC.1	External sync inputs not operational	‘-’, ‘A’, ‘E’	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	‘-’, ‘A’, ‘E’	Section 3.2
APB.1	Access to the APB peripherals may not operate correctly when the APB bus's PCLK divider is set to 5 or more.	‘-’, ‘A’, ‘E’, ‘F’	Section 3.3
ETHERNET.1	In Ethernet MII mode, the transmit data TXD3:0 and transmit enable TX_EN incorrectly reference RX_CLK in data transmission.	‘-’, ‘A’, ‘E’	Section 3.4
I2C.1	In slave-transmitter mode, the device set in monitor mode must write a dummy value of 0xFF into the DAT register.	‘-’, ‘A’, ‘E’, ‘F’	Section 3.5
IBAT.1	Typical lots have about 5 % parts with higher than normal I_{BAT} current when only V_{BAT} power is provided (VDD_{BAT} is grounded).	‘-’, ‘A’, ‘E’, ‘F’	Section 3.6
ISP.1	Maximum UART ISP baud rate limited to 57,600	‘-’, ‘A’, ‘E’	Section 3.7
PBOOST.1	Boost control bits PBOOST[0:1] are not set to 11 when user code is first executed following reset.	‘-’, ‘A’, ‘E’	Section 3.8
RTC.1	The RTC may lose time when RESET is toggled	‘-’, ‘A’, ‘E’, ‘F’	Section 3.9
USART.1	Smart Card TX retry error interrupt not working	‘-’, ‘A’, ‘E’	Section 3.10

Table 2. Functional problems table *...continued*

Functional problems	Short description	Revision identifier[1]	Detailed description
USART.2	'False positive' break indicator events may occur	'-', 'A', 'E'	Section 3.11
USB.1	USB host controller hangs on a dribble bit	'-', 'A', 'E'	Section 3.12
WDT.1	WDT timeout does not wake from deep sleep	'-', 'A', 'E'	Section 3.13

[1] Rev 'F' applies to LPC1774FBD144 only.

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
DPD.1	Increase of Deep power-down leakage current over time	'-'	Section 4.1

Table 4. Errata notes table

Errata notes	Short description	Revision identifier[1]	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'-', 'A', 'E', 'F'	Section 5.1

[1] Rev 'F' applies to LPC1774FBD144 only.

3. Functional problems detail

3.1 ADC.1

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

32.5.1 A/D Control Register (AD0CR - 0x4003 4000)

Table 656: A/D Control Register (AD0CR - address 0x4003 4000) bit description

Bit	Symbol	Value	Description	Reset value
7:0	SEL		Selects which of the AD0[7:0] pins is (are) to be sampled and converted. For AD0, bit 0	0x01
26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on the P2[10] pin.	
		011	Start conversion when the edge selected by bit 27 occurs on the P1[27] pin.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1. Note that this does not require that the MAT0.1 function appear on a device pin.	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3. Note that it is not possible to cause the MAT0.3 function to appear on a device pin.	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0. Note that this does not require that the MAT1.0 function appear on a device pin.	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1. Note that this does not require that the MAT1.1 function appear on a device pin.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P2.10 or P1.27 may be missed. The occurrence of this problem is peripheral clock (PCLK) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK = 100 MHz, probability error = 12 %
- For PCLK = 50 MHz, probability error = 6 %
- For PCLK = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.2 ADC.2

Introduction:

On the LPC177x/8x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.3 APB.1

Introduction:

The peripheral clock selection register PCLKSEL controls the base clock used for all APB peripherals. A 5-bit divider allows a range of frequencies to be used.

Problem:

On the LPC177x_8x, access to the APB peripherals may not operate correctly when the APB's divider is set to 5 or more. Both APB buses have the same issue.

Work-around:

Use PCLK divider ratio of 1, 2, 3 and 4 only.

3.4 ETHERNET.1

Introduction:

The Ethernet block contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration. The Ethernet block interfaces between an off-chip Ethernet PHY using the MII (Media Independent Interface) or RMII (reduced MII) protocol and the on-chip MIIM (Media Independent Interface Management) serial bus.

Problem:

In MII mode, the transmit data TXD3:0 and transmit enable TX_EN should reference the TX_CLK from the Ethernet PHY. However, due to a configuration error in the chip, the transmit data TXD3:0 and transmit enable TX_EN reference RX_CLK in data transmission. The consequence of this error is that a small percentage of packets cannot be received by the PHY.

Work-around:

This will be fixed with the next silicon release.

Note: There is no issue in RMII mode operation.

3.5 I2C.1

Introduction:

The I2C monitor mode allows the I2C module to monitor traffic on the I^2C-bus without actually participating in traffic or interfering with the I^2C-bus.

Problem:

In slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I^2C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1);     //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for slave-transmitter mode:

```
case 0xA8:      // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:      // data byte in DAT transmitted, ACK received
case 0xC0:      // (last) data byte transmitted, NACK received
case 0xC8:      // last data byte in DAT transmitted, ACK received
     DataByte = LPC_I2C->DATA_BUFFER; //Save data. Data can be processed in Main loop
     LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
     LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.6 IBAT.1

Introduction:

Two independent power domains (VDD_{REG} domain and V_{BAT} domain) are provided that allow the bulk of the device to have power removed while maintaining operation of the Real Time Clock (RTC). The V_{BAT} pin supplies power only to the RTC domain and is active when V_{BAT} is greater than VDD_{REG}. The RTC requires a minimum of power to operate, which can be supplied by an external battery (V_{BAT}). Whenever the device core power (VDD_{REG}) is greater than V_{BAT}, VDD_{REG} is used to operate the RTC. When VDD_{REG} is grounded, the I_{BAT} is typically around 1 uA.

Problem:

Typical lots have about 5 % parts with I_{BAT} current as high as about 10 uA when only V_{BAT} is applied (VDD_{REG} is grounded). This is due to a leakage current path in a level shifter in the power domain.

Work-around:

The problematic leakage path is disabled when the part is entered into Deep power-down mode. If the application allows, the customer should put the device into Deep power-down mode before the VDD_{REG} power is grounded; the BOD ISR could potentially be used for this purpose.

3.7 ISP.1

Introduction:

In-System Programming (ISP) is programming or reprogramming the on-chip flash memory, using the boot loader software and UART0 serial port. This can be done when the part resides in the end-user board.

Problem:

UART ISP cannot be used at rates higher than 57,600 bits per second.

Work-around:

UART ISP must be used at 57,600 bits per second or a lower communications speed.

3.8 PBOOST.1

Introduction:

The Power Boost control register allows choosing between high-speed operation above 100 MHz (PBOOST[0:1] is set to 11), or power savings when operation is at 100 MHz or lower (PBOOST[0:1] is cleared to 00), by controlling the output of the main on-chip regulator. This boost is on by default (PBOOST[0:1] is set to 11) when user code begins after a chip reset.

Problem:

Certain products with date code (marked on the 3rd line of the product) on or before wk1238 do not have their PBOOST[0:1] set to 11 when user code is first executed following reset. These products may not operate reliably when running above 100 MHz.

Work-around:

Set PBOOST[0:1] to 11 with user code.

3.9 RTC.1

Introduction:

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses very little power when its registers are not being accessed by the CPU, especially in reduced power modes.

Problem:

RTC temporarily pauses and loses fractions of a second during the rising and falling edges of RESET. This occurs only in the LQFP packages with certain voltage swings and ramp rates. The problem is exacerbated by low temperatures. Reducing the voltage swing and/or ramp rate of the reset pulse will eliminate this loss of time counts. When this issue occurs, the impact on RTC accuracy is expected to be one second every several thousand reset events.

Work-around:

Adding an RC filter between the reset pin and the external reset input to control the reset signal voltage ramp rate can prevent this problem.

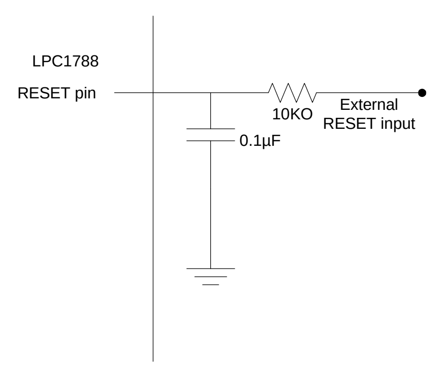

Fig 2. RTC.1 work-around

3.10 USART.1

Introduction:

USART4 includes a synchronous mode and a Smart Card mode supporting ISO 7816-3. This allows smart cards to be interfaced to support high security applications.

Problem:

The USART4 Transmit Interrupt is entered after failed retries (based on NACK) but source of error is not given in IIR or LSR registers. This happens when the TX FIFO has one or more items still to be sent out. When there are no other items in the TX FIFO and the FIFO head item fails the retry, the interrupt works correctly with bit 8 flagged in the LSR.

Work-around:

A workaround is to avoid using the FIFO on USART4 in Smart Card mode. When there is data ready to transmit, hold it in a software queue until the FIFO is empty then send it one character at a time. Another workaround is to check all of the interrupt sources in the TX interrupt and if there is no interrupt source, to assume that a NAK could have been received. This allows use of the FIFO but could require changes to program logic.

3.11 USART.2

Introduction:

The LPC177x/8x device family features an option to operate the USART4 in synchronous mode.

Problem:

When using synchronous UART mode (USART) under the following conditions:

- CSCEN = 0 (SCK active only during transmission)
- CSRC = 0 (Synchronous Slave Mode)
- FES = 1 (Falling Edge Sampling)
- SSDIS = 0 (Use Start and Stop Bit)
- The external transmitting device (Master) sends start and stop bits
- The external device transmits 0x00

The Break Interrupt (BI) flag can become set, despite the fact that no break condition on the bus has occurred. This problem does not manifest when the external master device uses two stop bits.

Work-around:

None, however in some cases system designers have control over the protocol being used between devices and can avoid the error condition outlined above in their system design and/or communication protocol.

3.12 USB.1

Introduction:

Full-/low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred and the packet should be ignored.

The time interval just before an EOP is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet for which there are up to six full bit times at the port with no transitions prior to the EOP.

Problem:

The USB host controller will hang indefinitely if it sees a dribble bit on the USB bus. It will hang the first time a dribble bit is seen. Once it is in this state there is no recovery other than a hard chip reset. This problem has no effect on the USB device controller.

Work-around:

None.

3.13 WDT.1

Introduction:

The purpose of the Watchdog Timer is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, a watchdog event will be generated if the user program fails to "feed" (or reload) the Watchdog within a predetermined amount of time. The Watchdog event will cause a chip reset if configured to do so.

Problem:

WDT timeout operates in run and sleep modes, but does not wake the MCU from deep sleep mode.

Work-around:

None.

4. AC/DC deviations detail

4.1 DPD.1

Introduction:

Deep power-down is a low-power mode that achieves currents in the low single-digit microamperes.

Problem:

Increase of $I_{DDREG(3V3)}$ current in Deep power-down mode for on-chip regulator over time (to about 100-200 uA). There is no functional impact.

Expected time to result in high regulator Deep power-down current vs. temperature and bias is listed in Table 5.

Table 5. LPC177x/8x on-chip regulator expected time (years) to result in high regulator Deep power-down current under different bias and temp condition

V_{DD}	Years at 25 °C	Years at 85 °C
2.5 V	4.98E+05	7190.00
3.0 V	714	10.30
3.3 V	14.1	0.20

Identification of Changed Product: All Rev '-' devices.

Remarks:

1. Issue described will lead to problems only if customer puts bias on V_{DD_REG} at over 3.0 V with application sensitive to $I_{DDREG(3V3)}$ curent in Deep power-down mode (few hundred uA)
2. If the biased V_{DD} can be restricted to 3.0 V then the expected time to result in high leakage current will be over 10 years at Industrial temp range.
3. Biased V_{DD} of 3.3 V at 25 °C (room temp) will also guarantee datasheet spec for over 10 years.
4. If $I_{DDREG(3V3)}$ current in Deep power-down mode (few hundred uA) is a key parameter, it is not advised to bias V_{DD_REG} above 3.0 V.

Work-around:

None. This has been fixed in Rev 'A'.

5. Errata notes detail

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

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Date of release: 26 November 2013

Document identifier: ES_LPC177X_8X