

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515BQ is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to $1,6 \Omega$). At a supply voltage $V_p = 14,4 \text{ V}$, an output power of 24 W can be delivered into a 4Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers $2 \times 12 \text{ W}$ into 2Ω or $2 \times 7 \text{ W}$ into 4Ω .

Special features are:

- flexibility in use — mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. $1 \mu\text{A}$), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- a.c. and d.c. short-circuit safe to ground up to $V_p = 18 \text{ V}$
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

QUICK REFERENCE DATA

Supply voltage range (operating)	V_p	6 to 18 V
Supply voltage (non-operating)	V_p max.	28 V
Supply voltage (non-operating; load dump protection)	V_p max.	45 V
Repetitive peak output current	I_{ORM} max.	4 A
Total quiescent current	I_{tot} typ.	75 mA
Stand-by current	I_{sb} typ.	$1 \mu\text{A}$
Switch-on current	I_{so} <	$100 \mu\text{A}$
Input impedance	$ Z_i $ >	$1 \text{ M}\Omega$
Bridge tied load application (BTL)	V_p =	14,4 13,2 V
Output power at $R_L = 4 \Omega$ (with bootstrap)		
$d_{tot} = 0,5\%$	P_o typ.	18 15 W
$d_{tot} = 10\%$	P_o typ.	24 20 W
Supply voltage ripple rejection; $R_S = 0 \Omega$; $f = 100 \text{ Hz}$	RR typ.	50 50 dB
D.C. output offset voltage between the outputs	$ \Delta V_{5-g} $ <	50 50 mV
Stereo application		
Output power at $d_{tot} = 10\%$ (with bootstrap)		
$R_L = 4 \Omega$	P_o typ.	7 6 W
$R_L = 2 \Omega$	P_o typ.	12 10 W
Output power at $d_{tot} = 0,5\%$ (with bootstrap)		
$R_L = 4 \Omega$	P_o typ.	5,5 4,5 W
$R_L = 2 \Omega$	P_o typ.	9 7,5 W
Channel separation	α >	40 40 dB
Noise output voltage; $R_S = 10 \text{ k}\Omega$; according to IEC curve-A	V_n typ.	0,2 0,2 mV

PACKAGE OUTLINE 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

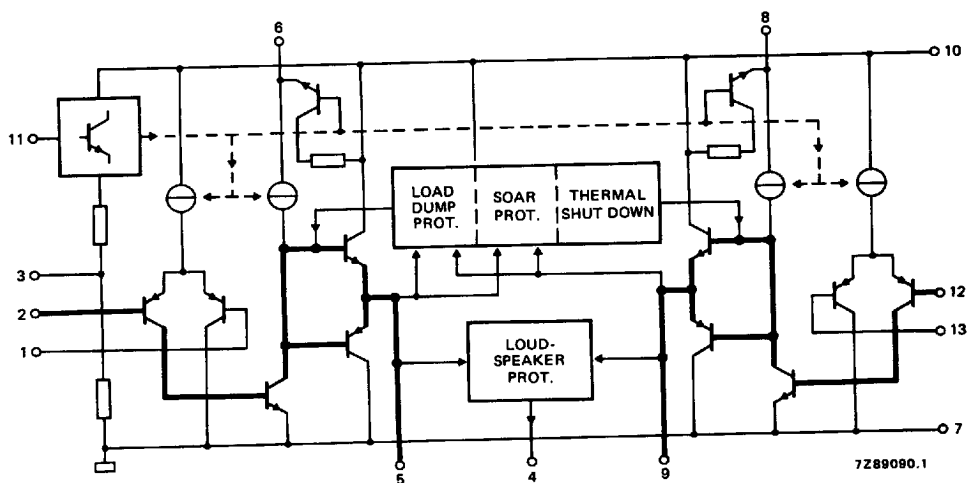


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	-55 to + 150 °C	
Crystal temperature	T_C	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

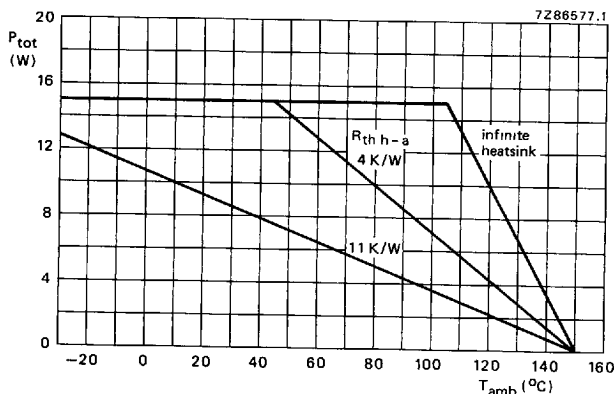


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

 $T_{amb} = 65$ °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4 \text{ K/W.}$$

2 x 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

 $T_{amb} = 65$ °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11 \text{ K/W.}$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1,8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$ Z_{OFF} $	>	100 k Ω
Stand-by current at $V_{11} = 0$ to 0,8 V	I_{sb}	typ.	1 μ A
		<	100 μ A
Switch-on current (pin 11) at $V_{11} \leq V_{10}$ (note 1)	I_{so}	typ.	10 μ A
		<	100 μ A

A.C. CHARACTERISTICS

$T_{amb} = 25$ °C; $V_P = 14,4$ V; $f = 1$ kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at $R_L = 4$ Ω (with bootstrap)

$V_P = 14,4$ V; $d_{tot} = 0,5\%$

P_o	>	15,5 W
	typ.	18 W

$V_P = 14,4$ V; $d_{tot} = 10\%$

P_o	>	20 W
	typ.	24 W

$V_P = 13,2$ V; $d_{tot} = 0,5\%$

P_o	typ.	15 W
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$V_P = 13,2$ V; $d_{tot} = 10\%$

P_o	typ.	20 W
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Open loop voltage gain

G_o	typ.	75 dB
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Closed loop voltage gain (note 2)

G_c	typ.	40 ($\pm 0,5$) dB
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Output power without bootstrap (note 9)

$V_P = 14,4$ V; $d_{tot} = 10\%$

P_o	typ.	15 W
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$V_P = 14,4$ V; $d_{tot} = 0,5\%$

P_o	typ.	12 W
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$V_P = 13,2$ V; $d_{tot} = 10\%$

P_o	typ.	12 W
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$V_P = 13,2$ V; $d_{tot} = 0,5\%$

P_o	typ.	9 W
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Frequency response at -3 dB (note 3)

B		20 Hz to min. 20 kHz
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Input impedance (note 4)

$ Z_i $	>	1 M Ω
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Noise input voltage (r.m.s. value) at $f = 20$ Hz to 20 kHz

$R_S = 0$ Ω

$V_n(rms)$	typ.	0,2 mV
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$R_S = 10$ k Ω

$V_n(rms)$	typ.	0,35 mV
	<	0,8 mV

$R_S = 10$ k Ω ; according to IEC 179 curve A

V_n	typ.	0,25 mV
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Supply voltage ripple rejection (note 5)

$f = 100$ Hz

RR	>	42 dB
	typ.	50 dB

D.C. output offset voltage between the outputs

$ \Delta V_{5-9} $	<	50 mV
	typ.	2 mV

Loudspeaker protection (all conditions)
maximum d.c. voltage (across the load)

$ \Delta V_{5-9} $	<	1 V
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Power bandwidth; -1 dB; $d_{tot} = 0,5\%$

B		30 Hz to 40 kHz
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Stereo application; see Fig. 4

Output power at $d_{\text{tot}} = 10\%$; with bootstrap (note 6)

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega$$

$$V_P = 14,4 \text{ V}; R_L = 2 \Omega$$

$$V_P = 13,2 \text{ V}; R_L = 4 \Omega$$

$$V_P = 13,2 \text{ V}; R_L = 2 \Omega$$

Output power at $d_{\text{tot}} = 0,5\%$; with bootstrap (note 6)

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega$$

$$V_P = 14,4 \text{ V}; R_L = 2 \Omega$$

$$V_P = 13,2 \text{ V}; R_L = 4 \Omega$$

$$V_P = 13,2 \text{ V}; R_L = 2 \Omega$$

Output power at $d_{\text{tot}} = 10\%$; without bootstrap

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega \text{ (notes 6, 8 and 9)}$$

Frequency response at -3 dB (note 3)

Supply voltage ripple rejection (note 5)

Channel separation; $R_S = 10 \text{ k}\Omega$; $f = 1 \text{ kHz}$

Closed loop voltage gain (note 7)

Noise output voltage (r.m.s. value) at $f = 20 \text{ Hz}$ to 20 kHz

$$R_S = 0 \Omega$$

$$R_S = 10 \text{ k}\Omega$$

$$R_S = 10 \text{ k}\Omega; \text{ according to IEC 179 curve A}$$

P_O	>	6 W
	typ.	7 W
P_O	>	10 W
	typ.	12 W
P_O	typ.	6 W
P_O	typ.	10 W
P_O	typ.	5,5 W
P_O	typ.	9 W
P_O	typ.	4,5 W
P_O	typ.	7,5 W
P_O	typ.	6 W
B	40 Hz to min.	20 kHz
RR	typ.	50 dB
α	>	40 dB
	typ.	50 dB
G_c	typ.	40 dB
$V_{n(\text{rms})}$	typ.	0,15 mV
$V_{n(\text{rms})}$	typ.	0,25 mV
V_n	typ.	0,2 mV

Notes

1. The internal circuit impedance at pin 11 is $> 5 \text{ k}\Omega$ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. $100 \text{ k}\Omega$.
5. Supply voltage ripple rejection measured with a source impedance of 0Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of $56 \text{ k}\Omega$ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the $100 \mu\text{F}$ capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

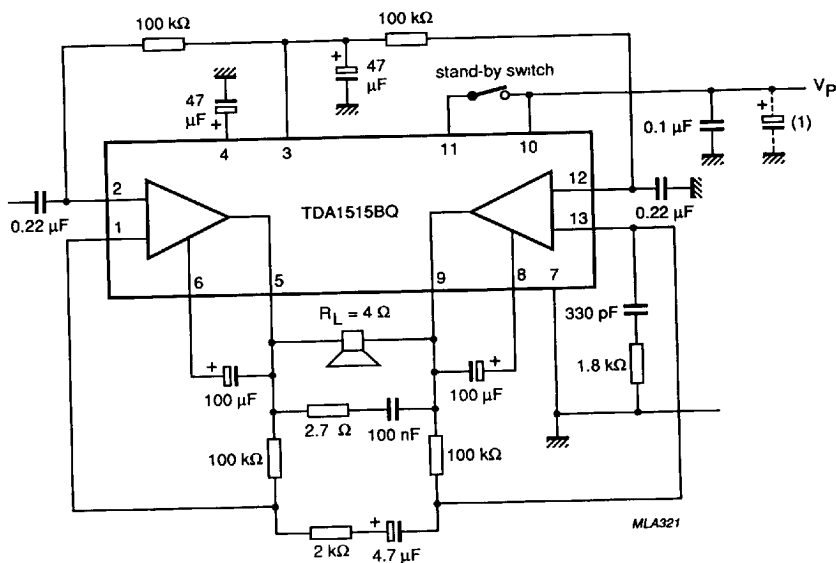


Fig. 3 Test/application circuit bridge tied load (BTL).

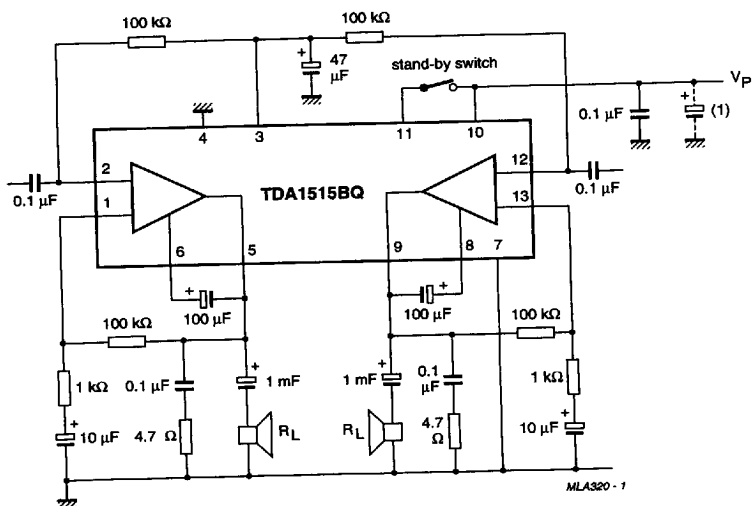


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.