

## 1-Mbit (64K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **High speed**
  - $t_{AA} = 12$  ns (Commercial & Industrial)
  - $t_{AA} = 15$  ns (Automotive)
- **CMOS for optimum speed/power**
- **Low active power**
  - 770 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in Pb-free and non Pb-free 44-pin TSOP II and 44-pin 400-mil-wide SOJ**

### Functional Description<sup>[1]</sup>

The CY7C1021B is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an

automatic power-down feature that significantly reduces power consumption when deselected.

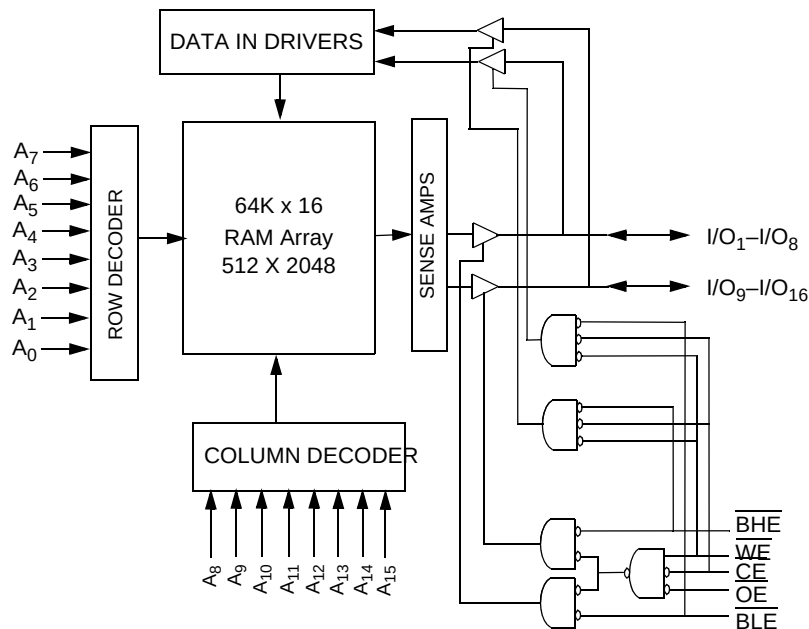
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1021B is available in standard 44-pin TSOP Type II and 44-pin 400-mil-wide SOJ packages.

### Logic Block Diagram



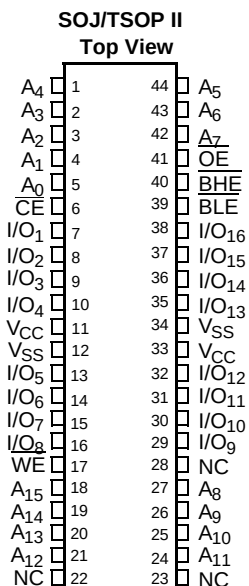
#### Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Selection Guide

|                                   |             | -12 | -15 |
|-----------------------------------|-------------|-----|-----|
| Maximum Access Time (ns)          |             | 12  | 15  |
| Maximum Operating Current (mA)    | Com'l/Ind'l | 140 | 130 |
|                                   | Automotive  |     | 130 |
| Maximum CMOS Standby Current (mA) | Com'l/Ind'l | 10  | 10  |
|                                   | Automotive  |     | 15  |
|                                   | L Version   | 0.5 | 0.5 |

## Pin Configurations



## Pin Definitions

| Pin Name                                          | SOJ, TSOP-Pin Number      | I/O Type      | Description                                                                                                                                                                                                   |
|---------------------------------------------------|---------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A <sub>0</sub> –A <sub>15</sub>                   | 1–5, 18–21, 24–27, 42–44  | Input         | <b>Address Inputs</b> used to select one of the address locations.                                                                                                                                            |
| I/O <sub>1</sub> –I/O <sub>16</sub>               | 7–10, 13–16, 29–32, 35–38 | Input/Output  | <b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.                                                                                                                    |
| NC                                                | 22, 23, 28                | No Connect    | <b>No Connects.</b> Not connected to the die.                                                                                                                                                                 |
| $\overline{\text{WE}}$                            | 17                        | Input/Control | <b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.                                                                                    |
| $\overline{\text{CE}}$                            | 6                         | Input/Control | <b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.                                                                                                              |
| $\overline{\text{BHE}}$ , $\overline{\text{BLE}}$ | 40, 39                    | Input/Control | <b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>16</sub> –I/O <sub>9</sub> , $\overline{\text{BLE}}$ controls I/O <sub>8</sub> –I/O <sub>1</sub> .                     |
| $\overline{\text{OE}}$                            | 41                        | Input/Control | <b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. |
| V <sub>SS</sub>                                   | 12, 34                    | Ground        | <b>Ground for the device.</b> Should be connected to ground of the system.                                                                                                                                    |
| V <sub>CC</sub>                                   | 11, 33                    | Power Supply  | <b>Power Supply inputs to the device.</b>                                                                                                                                                                     |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  Relative to GND<sup>[2]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC}+0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC}+0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

## Operating Range

| Range      | Ambient Temperature ( $T_A$ ) <sup>[3]</sup> | $V_{CC}$ |
|------------|----------------------------------------------|----------|
| Commercial | 0°C to +70°C                                 | 5V ± 10% |
| Industrial | -40°C to +85°C                               | 5V ± 10% |
| Automotive | -40°C to +125°C                              | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter        | Description                                        | Test Conditions                                                                                                                                        |             | -12  |      | -15  |      | Unit |
|------------------|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|------|------|------|------|
|                  |                                                    |                                                                                                                                                        |             | Min. | Max. | Min. | Max. |      |
| V <sub>OH</sub>  | Output HIGH Voltage                                | V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA                                                                                                      |             | 2.4  |      | 2.4  |      | V    |
| V <sub>OL</sub>  | Output LOW Voltage                                 | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                                                                                                       |             |      | 0.4  |      | 0.4  | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                                 |                                                                                                                                                        |             | 2.2  | 6.0  | 2.2  | 6.0  | V    |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[2]</sup>                   |                                                                                                                                                        |             | −0.5 | 0.8  | −0.5 | 0.8  | V    |
| I <sub>Ix</sub>  | Input Leakage Current                              | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                 | Com'l/Ind'l | −1   | +1   | −1   | +1   | μA   |
|                  |                                                    |                                                                                                                                                        | Auto        |      |      | −4   | +4   | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled                                                                                            | Com'l/Ind'l | −1   | +1   | −1   | +1   | μA   |
|                  |                                                    |                                                                                                                                                        | Auto        |      |      | −4   | +4   | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating<br>Supply Current        | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA,<br>f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                           | Com'l/Ind'l |      | 140  |      | 130  | mA   |
|                  |                                                    |                                                                                                                                                        | Auto        |      |      |      | 130  | mA   |
| I <sub>SB1</sub> | Automatic CE<br>Power Down Current —TTL<br>Inputs  | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f =<br>f <sub>MAX</sub> | Com'l/Ind'l |      | 40   |      | 40   | mA   |
|                  |                                                    |                                                                                                                                                        | Auto        |      |      |      | 50   | mA   |
| I <sub>SB2</sub> | Automatic CE<br>Power Down Current<br>—CMOS Inputs | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} -$<br>0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V,<br>or V <sub>IN</sub> ≤ 0.3V, f = 0            | Com'l/Ind'l |      | 10   |      | 10   | mA   |
|                  |                                                    |                                                                                                                                                        | Auto        |      |      |      | 15   | mA   |
|                  |                                                    |                                                                                                                                                        | L Version   |      | 0.5  |      | 0.5  | mA   |

## Capacitance<sup>[4]</sup>

| Parameter | Description        | Test Conditions                                                     | Max. | Unit |
|-----------|--------------------|---------------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ ,<br>$V_{CC} = 5.0V$ | 8    | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                     | 8    | pF   |

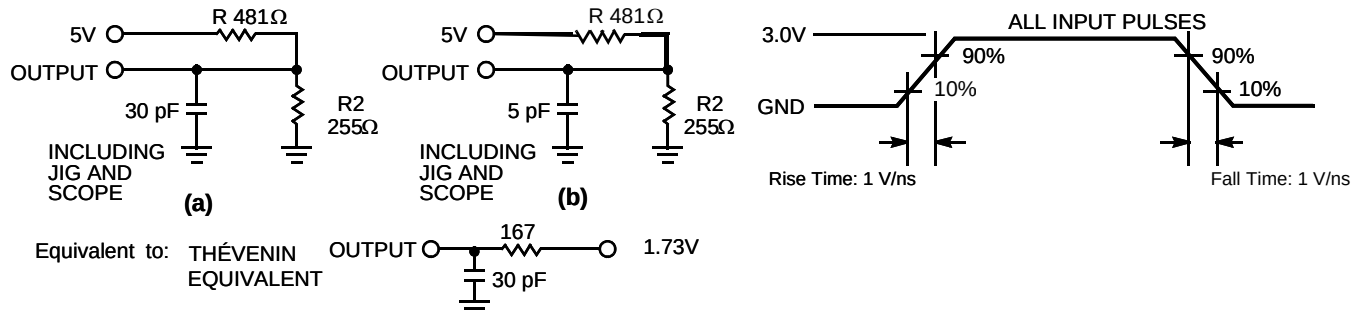
## Thermal Resistance<sup>[4]</sup>

| Parameter     | Description                              | Test Conditions                                                                                              | 44-pin SOJ | 44-pin TSOP-II | Unit |
|---------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------|------------|----------------|------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 64.32      | 76.89          | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)    |                                                                                                              | 31.03      | 14.28          | °C/W |

### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  and  $V_{IH}(\text{max.}) = V_{CC} + 0.5V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



## Switching Characteristics Over the Operating Range<sup>[5]</sup>

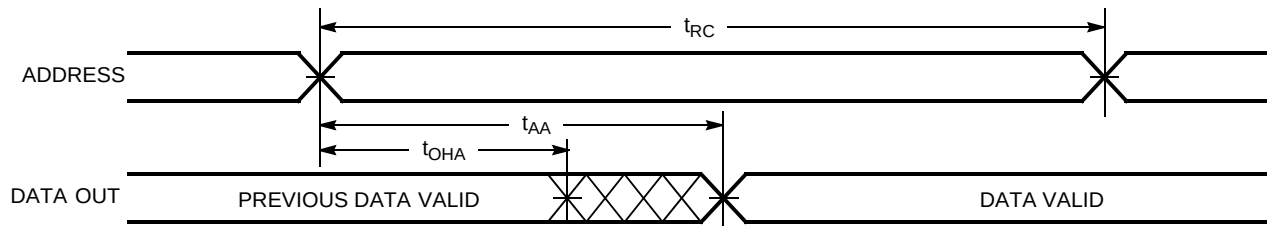
| Parameter                  | Description                                      | 7C1021B-12 |      | 7C1021B-15 |      | Unit |
|----------------------------|--------------------------------------------------|------------|------|------------|------|------|
|                            |                                                  | Min.       | Max. | Min.       | Max. |      |
| Read Cycle                 |                                                  |            |      |            |      |      |
| t <sub>RC</sub>            | Read Cycle Time                                  | 12         |      | 15         |      | ns   |
| t <sub>AA</sub>            | Address to Data Valid                            |            | 12   |            | 15   | ns   |
| t <sub>OHA</sub>           | Data Hold from Address Change                    | 3          |      | 3          |      | ns   |
| t <sub>ACE</sub>           | $\overline{CE}$ LOW to Data Valid                |            | 12   |            | 15   | ns   |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                |            | 6    |            | 7    | ns   |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z <sup>[6]</sup>      | 0          |      | 0          |      | ns   |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup> |            | 6    |            | 7    | ns   |
| t <sub>LZCE</sub>          | $\overline{CE}$ LOW to Low Z <sup>[6]</sup>      | 3          |      | 3          |      | ns   |
| t <sub>HZCE</sub>          | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup> |            | 6    |            | 7    | ns   |
| t <sub>PU</sub>            | $\overline{CE}$ LOW to Power-Up                  | 0          |      | 0          |      | ns   |
| t <sub>PD</sub>            | $\overline{CE}$ HIGH to Power-Down               |            | 12   |            | 15   | ns   |
| t <sub>DBE</sub>           | Byte Enable to Data Valid                        |            | 6    |            | 7    | ns   |
| t <sub>LZBE</sub>          | Byte Enable to Low Z                             | 0          |      | 0          |      | ns   |
| t <sub>HZBE</sub>          | Byte Disable to High Z                           |            | 6    |            | 7    | ns   |
| Write Cycle <sup>[8]</sup> |                                                  |            |      |            |      |      |
| t <sub>WC</sub>            | Write Cycle Time                                 | 12         |      | 15         |      | ns   |
| t <sub>SCE</sub>           | $\overline{CE}$ LOW to Write End                 | 9          |      | 10         |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End                      | 8          |      | 10         |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End                      | 0          |      | 0          |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start                    | 0          |      | 0          |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End                         | 6          |      | 8          |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End                         | 0          |      | 0          |      | ns   |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3          |      | 3          |      | ns   |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>  |            | 6    |            | 7    | ns   |
| t <sub>BW</sub>            | Byte Enable to End of Write                      | 8          |      | 9          |      | ns   |

### Notes:

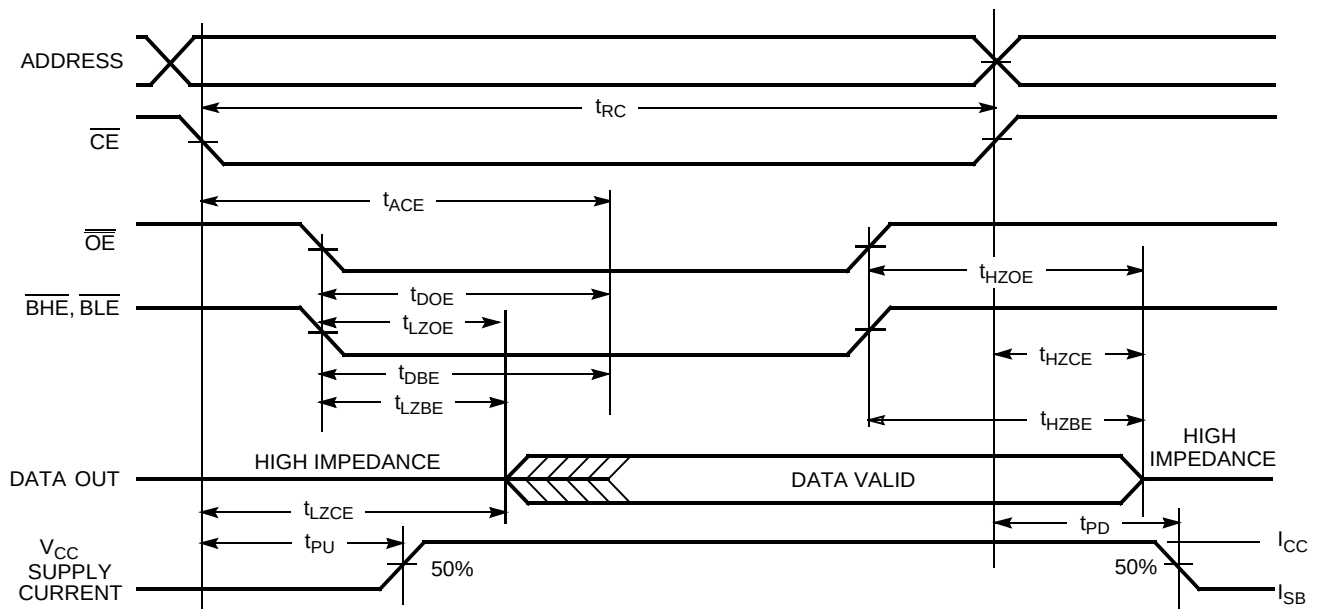
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle No. 1<sup>[9, 10]</sup>

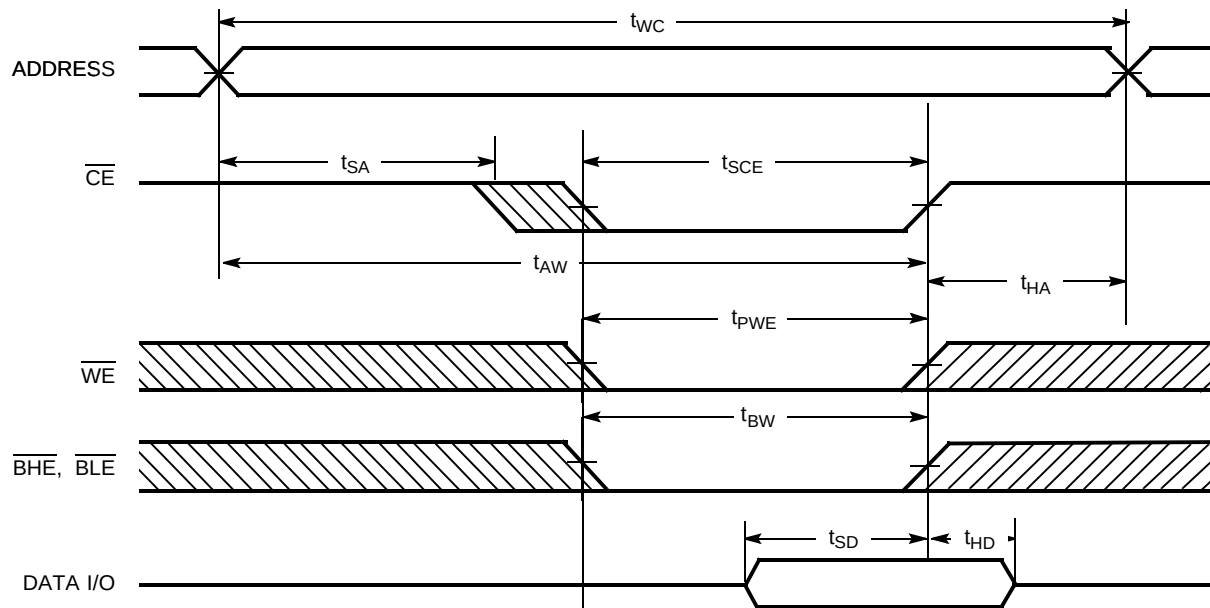
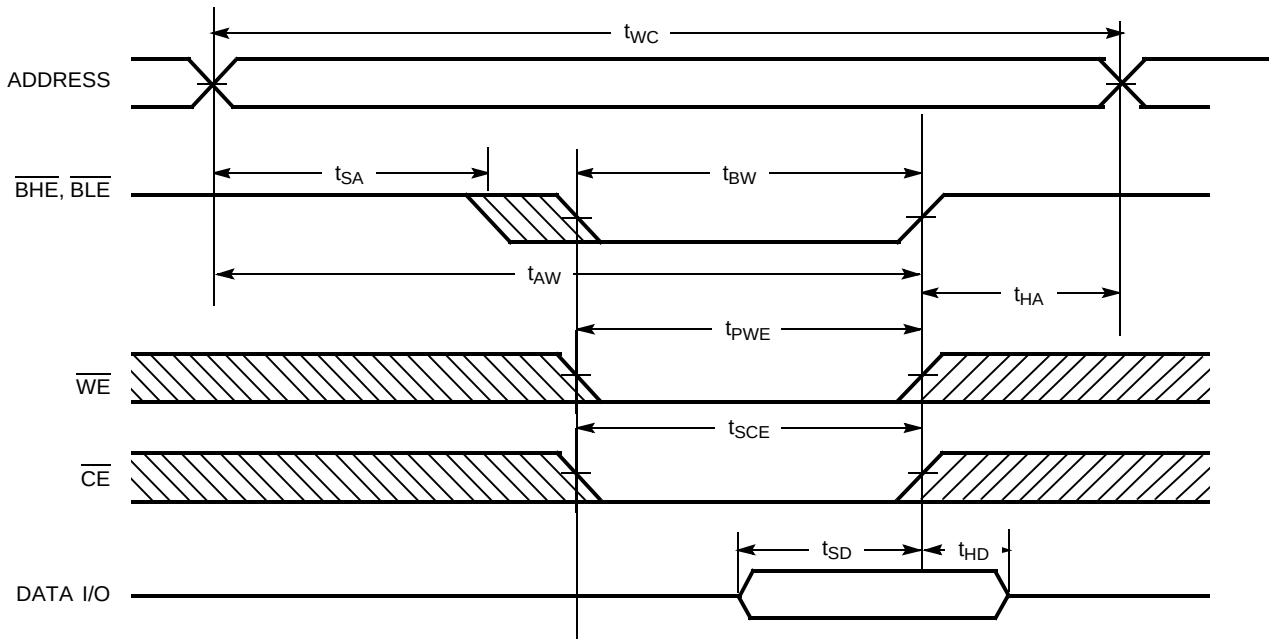


### Read Cycle No. 2 ( $\overline{\text{OE}}$ Controlled)<sup>[10, 11]</sup>



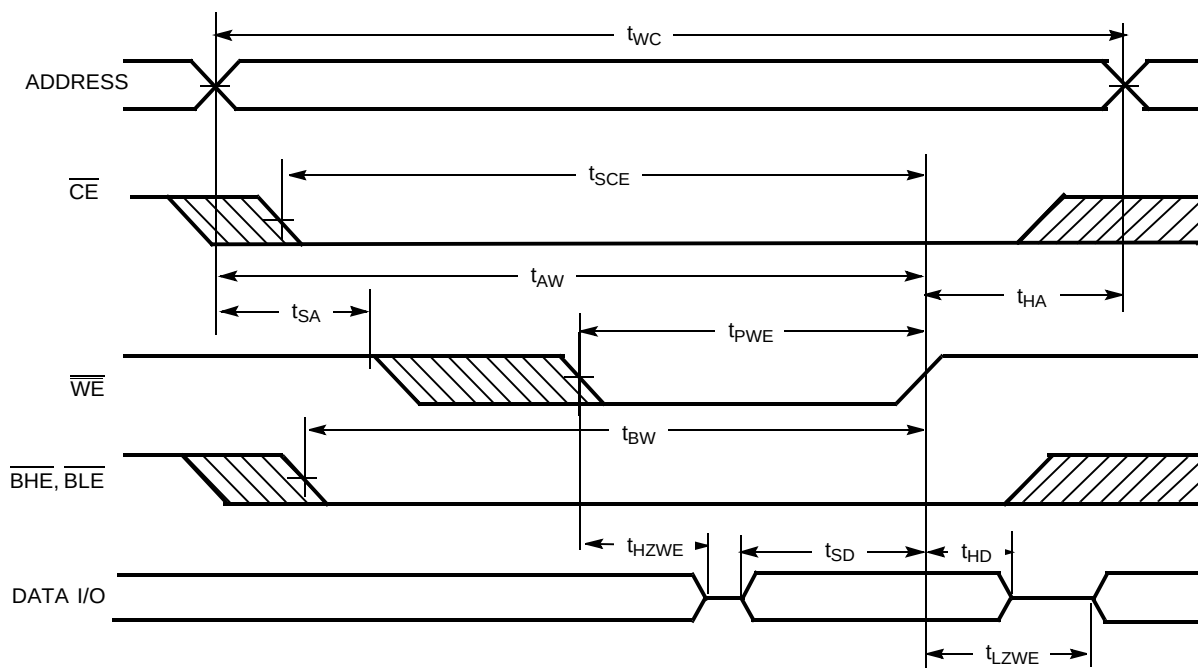
#### Notes:

9. Device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BHE}} = V_{\text{IL}}$ .
10.  $\overline{\text{WE}}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[12, 13]</sup>**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

12. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .  
 13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 (WE Controlled, OE LOW)**

**Truth Table**

| CE | OE | WE | BLE | BHE | I/O <sub>1</sub> -I/O <sub>8</sub> | I/O <sub>9</sub> -I/O <sub>16</sub> | Mode                       | Power                      |
|----|----|----|-----|-----|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H  | X  | X  | X   | X   | High Z                             | High Z                              | Power-Down                 | Standby (I <sub>SB</sub> ) |
| L  | L  | H  | L   | L   | Data Out                           | Data Out                            | Read - All bits            | Active (I <sub>CC</sub> )  |
|    |    |    | L   | H   | Data Out                           | High Z                              | Read - Lower bits only     | Active (I <sub>CC</sub> )  |
|    |    |    | H   | L   | High Z                             | Data Out                            | Read - Upper bits only     | Active (I <sub>CC</sub> )  |
| L  | X  | L  | L   | L   | Data In                            | Data In                             | Write - All bits           | Active (I <sub>CC</sub> )  |
|    |    |    | L   | H   | Data In                            | High Z                              | Write - Lower bits only    | Active (I <sub>CC</sub> )  |
|    |    |    | H   | L   | High Z                             | Data In                             | Write - Upper bits only    | Active (I <sub>CC</sub> )  |
| L  | H  | H  | X   | X   | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |
| L  | X  | X  | H   | H   | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |

**Ordering Information**

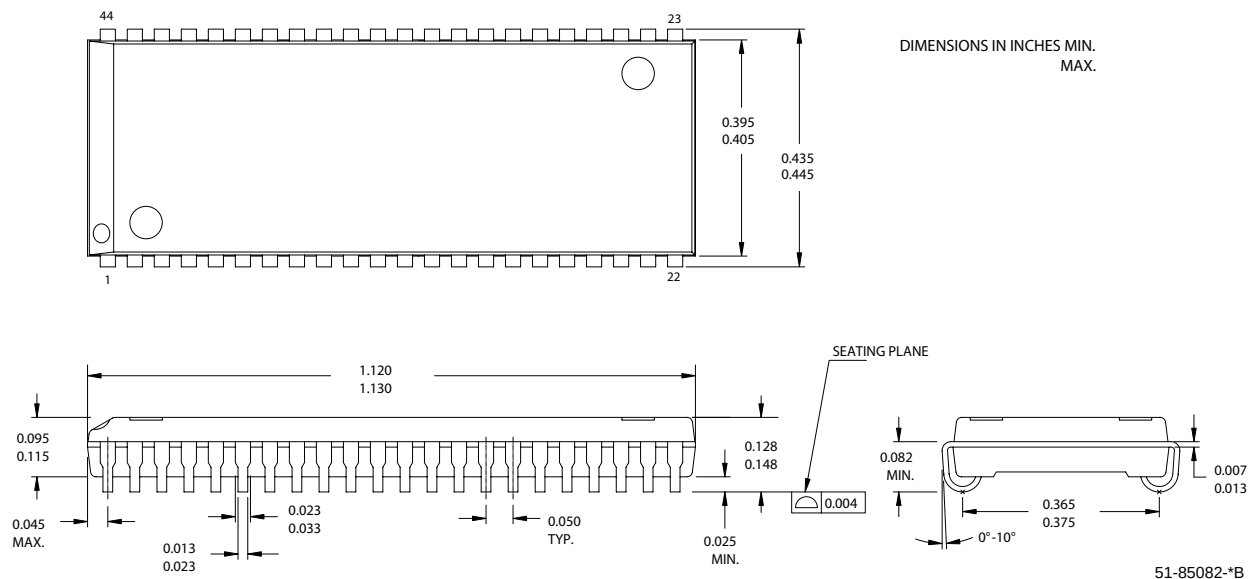
| Speed (ns) | Ordering Code   | Package Name | Package Type                          | Operating Range |
|------------|-----------------|--------------|---------------------------------------|-----------------|
| 12         | CY7C1021B-12VC  | 51-85082     | 44-pin (400-Mil) Molded SOJ           | Commercial      |
|            | CY7C1021B-12VXC |              | 44-pin (400-Mil) Molded SOJ (Pb-Free) |                 |
|            | CY7C1021B-12ZC  | 51-85087     | 44-pin TSOP Type II                   |                 |
|            | CY7C1021B-12ZXC |              | 44-pin TSOP Type II (Pb-Free)         |                 |
|            | CY7C1021B-12VI  | 51-85082     | 44-pin (400-Mil) Molded SOJ           | Industrial      |
|            | CY7C1021B-12VXI |              | 44-pin (400-Mil) Molded SOJ (Pb-Free) |                 |

**Ordering Information** (continued)

| Speed (ns) | Ordering Code    | Package Name | Package Type                          | Operating Range |
|------------|------------------|--------------|---------------------------------------|-----------------|
| 15         | CY7C1021B-15VC   | 51-85082     | 44-pin (400-Mil) Molded SOJ           | Commercial      |
|            | CY7C1021B-15VXC  |              | 44-pin (400-Mil) Molded SOJ (Pb-Free) |                 |
|            | CY7C1021B-15ZC   | 51-85087     | 44-pin TSOP Type II                   |                 |
|            | CY7C1021B-15ZXC  |              | 44-pin TSOP Type II (Pb-Free)         |                 |
|            | CY7C1021B-15VI   | 51-85082     | 44-pin (400-Mil) Molded SOJ           | Industrial      |
|            | CY7C1021B-15VXI  |              | 44-pin (400-Mil) Molded SOJ (Pb-Free) |                 |
|            | CY7C1021B-15ZI   | 51-85087     | 44-pin TSOP Type II                   |                 |
|            | CY7C1021BL-15ZI  |              | 44-pin TSOP Type II                   |                 |
|            | CY7C1021B-15ZXI  |              | 44-pin TSOP Type II (Pb-Free)         |                 |
|            | CY7C1021BL-15ZXI |              | 44-pin TSOP Type II (Pb-Free)         |                 |
|            | CY7C1021B-15VE   | 51-85082     | 44-pin (400-Mil) Molded SOJ           | Automotive      |
|            | CY7C1021B-15VXE  |              | 44-pin (400-Mil) Molded SOJ (Pb-Free) |                 |
|            | CY7C1021B-15ZE   | 51-85087     | 44-pin TSOP Type II                   |                 |
|            | CY7C1021B-15ZSXE |              | 44-pin TSOP Type II (Pb-Free)         |                 |

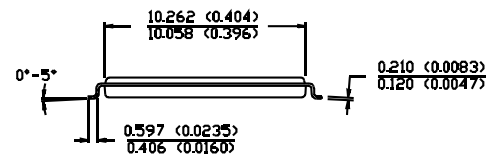
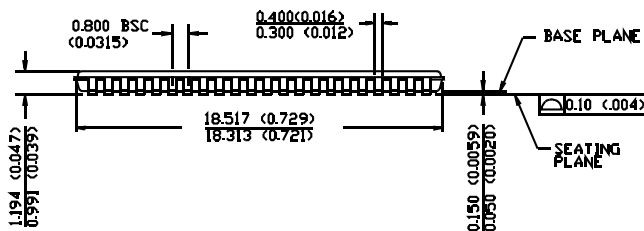
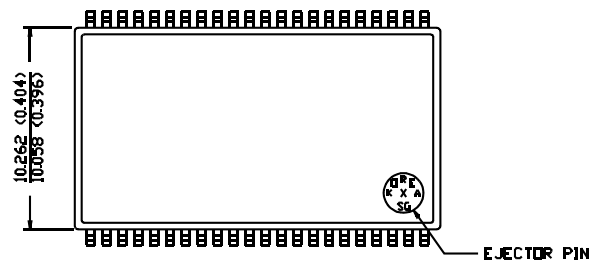
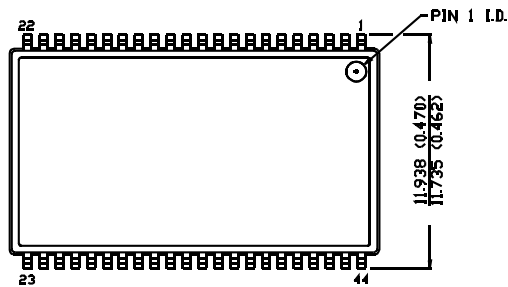
**Package Diagrams**

**44-pin (400-Mil) Molded SOJ (51-85082)**





DIMENSION [N MM (INCH)]  
MAX  
MIN.



**Document History Page**

| Document Title: CY7C1021B 1-Mbit (64K x 16) Static RAM<br>Document Number: 38-05145 |         |            |                 |                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------------------------------|---------|------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                        |
| **                                                                                  | 109889  | 09/22/01   | SZV             | Change from Spec number: 38-00951 to 38-05145                                                                                                                                                                                                                                                                                                |
| *A                                                                                  | 238454  | See ECN    | RKF             | 1) Added Automotive Specs to Data Sheet<br>2) Added Pb-Free device offering in the Ordering Information                                                                                                                                                                                                                                      |
| *B                                                                                  | 361795  | See ECN    | SYT             | Added Pb-Free offerings in the Ordering Information                                                                                                                                                                                                                                                                                          |
| *C                                                                                  | 505726  | See ECN    | NXR             | Removed CY7C10211B from Product offering<br>Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Changed teh $I_{CC}$ Max value from 150 mA to 130 mA<br>Removed $I_{OS}$ parameter from DC Electrical Characteristics table<br>Updated Ordering Information Table |