CS5462

Low Cost Power/Energy IC with Pulse Output

Features

- Single Chip; Power Measurement Solution
- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-Chip functions: Measures Energy and Performs Energy-to-Pulse Conversions
- Meets Accuracy Spec for IEC 687/1036
- On-Chip System Calibration Option
- High Pass Filter Option for Both I and V
- 2 Available Current Input Ranges
- On-Chip 2.5 V Reference (25 ppm/°C typ)
- Pulse Outputs for Stepper Motor or Mechanical Counter
- On-Chip Energy Direction Indicator
- Ground Reference Input Signals with Single Supply
- High Frequency Output for Calibration
- On-Chip Power-on Reset
- Power Supply Configurations:
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to 5 V

Description

The CS5462 is a low cost power meter solution combining two ΔΣ Analog-to-Digital Converters (ADC)'s, an energy-to-frequency converter, and energy pulse outputs on a single chip. It is designed to accurately measure and calculate energy for single phase 2- or 3-wire power metering applications with minimal external components.

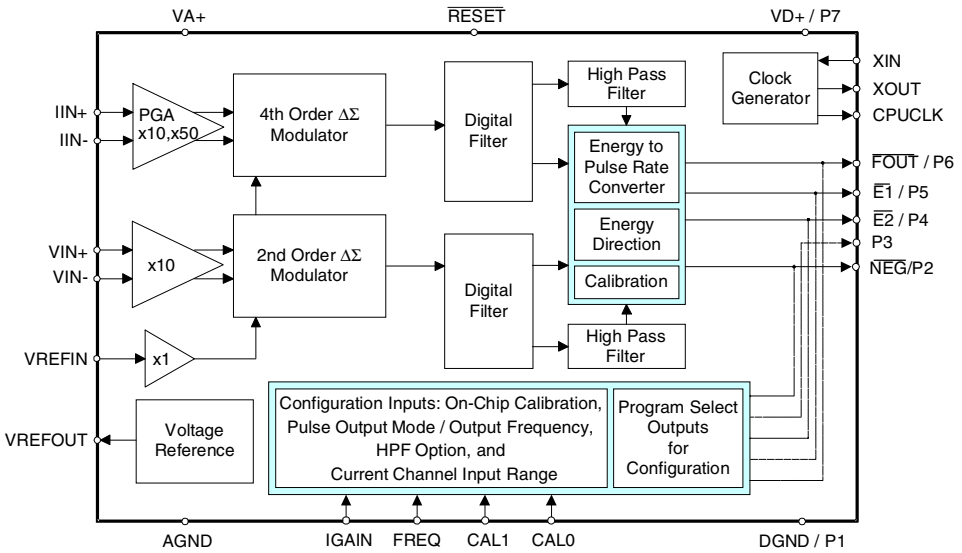
Low frequency energy outputs, $\overline{E1}$ and $\overline{E2}$, supply average real power and can be used to drive a stepper motor or a mechanical counter; the high frequency energy output $\overline{FOUT}$ can be used for calibration; and $\overline{NEG}$ indicates negative power.

The CS5462 has configuration pins which allow for direct configuration of pulse output format, pulse output frequency, current channel input range, high pass filter option, and on-chip calibration.

The CS5462 also has a power-on reset function which holds the part in reset until the supply reaches an operable level.

ORDERING INFORMATION

CS5462-IS	-40° to 85° C	24-pin SSOP



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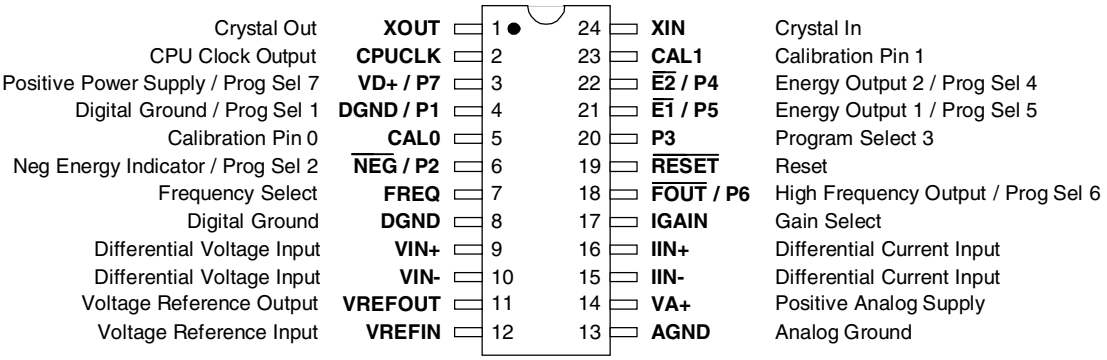
1. GENERAL DESCRIPTION

The CS5462 is a CMOS monolithic power measurement device with an energy computation engine. The CS5462 combines a programmable gain amplifier, two ΔΣ ADC's, system calibration, and energy-to-frequency conversion circuitry on a single chip.

The CS5462 is designed for energy measurement applications and is optimized to interface to a shunt or current transformer for current measurement, and to a resistive divider or transformer for voltage measurement. The current channel has a programmable gain amplifier (PGA) which provides two full-scale input level options. With a single +5 V supply on VA+/AGND, both of the CS5462's input channels accommodate common mode + signal levels between (AGND - 0.25 V) and VA+.

The CS5462 has three pulse output pins: $\overline{E1}$, $\overline{E2}$ and $\overline{FOUT}$. $\overline{E1}$ and $\overline{E2}$ can be used to directly drive a mechanical counter or stepper motor, or interface to a micro controller. The $\overline{FOUT}$ pin conveys average real power at a pulse frequency many times higher than that of the $\overline{E1}$ or $\overline{E2}$ pulse frequency, allowing for high speed calibration.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A single stage amplifier inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins		
Calibration Pins	5, 23	**CAL0, CAL1 -** Must be tied to a program select pin for calibration.
Program Selects[1,2,3,4,5,6]	4,6,20,22,21, 18,3	**P1, P2, P3, P4, P5, P6, P7 -** Used in Calibration, Frequency Select, and Input Gain Select.
Frequency Select	7	**FREQ -** Must be tied to a program select pin to determine the frequency of $\overline{E1}$ and $\overline{E2}$.
Current Channel Gain Select	17	**IGAIN -** Must be tied to a program select pin to determine the Full-Scale Input Voltage Range of the current channel.
Reset	19	**$\overline{RESET}$ -** Low activates Reset
Energy Pulse Outputs		
Energy Output 1[4], 2[3]	21, 22	**$\overline{E1}$, $\overline{E2}$ -** The energy output pin issues a fixed-width pulse train output with a rate proportional to real energy.
High Freq Output[5]	18	**$\overline{FOUT}$** - Outputs energy pulses at a maximum rate of 10 kHz. Used for calibration purposes.
Negative Energy Indicator[6]	6	**$\overline{NEG}$** - Low indicates negative energy.
Analog Inputs/Outputs		

Differential Voltage Inputs	9,10	**VIN+, VIN- -** Differential analog input pins for voltage channel.
Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2. 5V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN -** The voltage input to this pin establishes the voltage reference for the on-chip modulator.
Differential Current Inputs	16,15	**IIN+, IIN- -** Differential analog input pins for current channel.
Power Supply Connections		
Positive Digital Supply	3	**VD+ -** The positive digital supply.
Digital Ground	4*	**DGND -** Digital Ground
Analog Ground	13	**AGND -** Analog Ground
Positive Analog Supply	14	**VA+ -** The positive analog supply.

Notes: [1] Pin number 4 is described as Digital Ground (DGND) and also P1

[2] Pin number 3 is described as Positive Power Supply (VD+) and also P7

[3] Pin number 22 is described as Energy Output 2 ($\overline{E2}$) and also P4

[4] Pin number 21 is described as Energy Output 1 ($\overline{E1}$) and also P5

[5] Pin number 18 is described as High Frequency Output ($\overline{FOUT}$) and also P6

[6] Pin number 6 is described as Negative Energy Indicator ($\overline{NEG}$) and also P2

3.CHARACTERISTICS/SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25 °C.
- AGND = DGND = 0 V. All voltages with respect to 0 V.
- CAL0 and CAL1 are connected to P4 unless otherwise noted.

ANALOG CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channel)					
Maximum Differential Input Voltage Range (Gain = 10) {(I_{IN}+)-(I_{IN}-)} (Gain = 50)	I_{IN}	- -	- -	500 100	mV_{P-P} mV_{P-P}
Input Capacitance (All Gain Ranges)	C_{inI}	-	25	-	pF
Effective Input Impedance (All Gain Ranges)(Note 2)	Z_{inI}	30	-	-	kΩ
Analog Inputs (Voltage Channel)					
Maximum Differential Input Voltage Range {(V_{IN}+)-(V_{IN}-)}	V_{IN}	-	-	500	mV_{P-P}
Input Capacitance	C_{inV}	-	0.2	-	pF
Effective Input Impedance (Note 2)	Z_{inV}	5	-	-	MΩ
Accuracy (Energy Outputs)					
Offset Error	VOS	-	.01	-	%F.S.
Full-Scale Error (Note 1)	FSE	-	.1	-	%F.S.

Notes: 1. Applies After System Calibration

2. VA+ = VD+ = 5 V ±10 %; MCLK = 4.096 MHz

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
High Pass Filter Pole Frequency	-3 dB		-	0.5	-	Hz
Power Supplies						
Power Supply Currents	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption	(VD+ = 5 V)	PC	-	21	25	mW
(Note 3)	(VD+ = 3.3 V)		-	11.6	-	mW
Power Supply Rejection Ratio	(50, 60 Hz)			-	-	
(Note 4)	Voltage Channel (Gain = 10)	PSRR	48	-	-	dB
	Current Channel (Gain = 10)	PSRR	75	-	-	dB
	(Gain = 50)	PSRR	56	-	-	dB

Notes: 3. All outputs unloaded. All inputs CMOS level.

4. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sine wave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5462 is put into an internal test mode and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{0.150V}{V_{eq}}\right\}$$

VREFOUT REFERENCE OUTPUT VOLTAGE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	REFOUT	+2.4		+2.6	V
VREFOUT Temperature Coefficient	TC_{VREF}		25	60	ppm/°C
Load Regulation (Output Current 1 µA Source or Sink)	ΔV_R		6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 5. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\left(1.0 \times 10^{6}\right)$$

DIGITAL CHARACTERISTICS (Note 6)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}				
	XIN		(VD+) - 0.5	-	-	V
	$\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage (VD = 5 V)		V_{IL}				
	XIN		-	-	1.5	V
	$\overline{\text{RESET}}$		-	-	0.2 VD+	V
Low-Level Input Voltage (VD = 3.3 V)		V_{IL}				
	XIN		-	-	0.3	V
	$\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XOUT)	I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XOUT)	I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF
Drive Current $\overline{\text{FOUT}}$, $\overline{\text{E1}}$, $\overline{\text{E2}}$, $\overline{\text{NEG}}$, CPUCLK				90		mA

Notes: 6. All measurements performed under static conditions.

SWITCHING CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Gate Oscillator	MCLK	3	4.096	5	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 7)		40		60	%
Rise Times	Any Digital Input	t_{rise}	-	-	1.0	µs
(Note 8)	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input	t_{fall}	-	-	1.0	µs
(Note 8)	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 9)	t_{ost}	-	60	-	ms

7. If external MCLK is used, then the duty cycle must be between 45% and 55% to maintain this specification.
8. Specified using 10% and 90% points on wave-form of interest. Output loaded wi th 50pF.
9. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 10, 10 and 12)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 13, 14, 15)	I_{IN}	-	-	±10	mA
Power Dissipation	(Note 16)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

10. VA+ and AGND must satisfy {(VA+) - (AGND)} ≤ + 6.0 V.
11. VD+ and AGND must satisfy {(VD+) - (AGND)} ≤ + 6.0 V.
12. VA+ and VD+ can differ by as much as 200 mV, as long as VA+ > VD+.
13. Applies to all pins including continuous over-voltage conditions at the analog input pins.
14. Transient current of up to 100 mA will not cause SCR latch-up.
15. Maximum DC input current for a power supply pin is ±50 mA.
16. Total power dissipation, including all input currents and output currents.

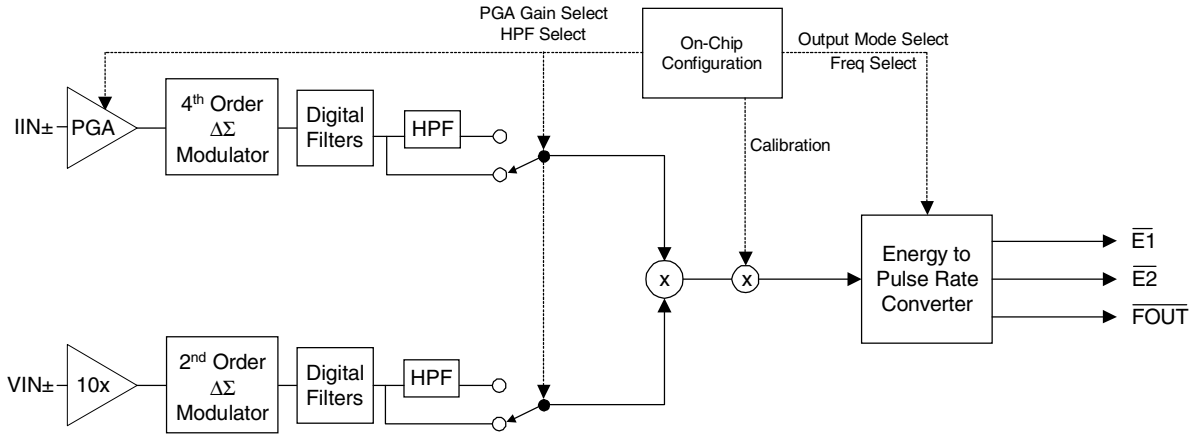


Figure 1. Data Flow

3.1 Theory of Operation

A computational flow diagram for the two data paths is shown in Figure 1. The analog waveforms at the voltage/current channel inputs are subject to the gains of the input PGAs.

3.1.1 Digital Filters

The modulators convert the analog input voltages on the I and V channels to a digital bitstream; which is then filtered by the digital filter section. The digital filter is composed of low pass $sinc^3$ and IIR filters. The IIR filters are used to compensate for the magnitude roll-off of the low pass filter section.

Both channels provide a high-pass filter option which can be engaged into the signal path to remove the DC content from the current/voltage signal before the energy calculations are made.

3.1.2 Gain Calibration

After being filtered, the instantaneous voltage and current digital codes are used to calculate real average power. This power is then adjusted based on the internal calibration setting defined at startup. Calibrating the CS5462 is done by externally connecting the configuration input pins, CAL1 and CAL0, to the program select output pins, P1 - P7, in a particular sequence. These connections will internally compensate for small gain errors.

3.1.3 Energy-to-Frequency Conversion

The calibrated energy value is then converted into a pulse output stream with a average frequency proportional to the measured energy. Pulse output pins $\overline{E1}$ and $\overline{E2}$ can be set to lower frequencies to directly drive a stepper motor or a mechanical counter or interface a microcontroller or infrared LED. The $\overline{FOUT}$ pulse output pin is set to max frequency of 10 kHz. With full scale inputs on both the current and voltage channels $\overline{FOUT}$ will output pulses with an average frequency of 10 kHz.

4. FUNCTIONAL DESCRIPTION

4.1 Programmable Gain Amplifier (PGA)

The CS5462 is equipped with a PGA on the current channel. While the voltage channel is always set to a 10x differential input voltage range (50 0mV$_{P-P}$), the current channel can be set to one of two different input ranges. The maximum differential voltage range on the current channel can be set to 10x (500 mV$_{P-P}$) and 50x (100 mV$_{P-P}$).

The gain setting of the current channel's PGA and also the high pass filter option are selected by connecting the IGAIN pin to one of seven Program Select output pins. For all applications the IGAIN pin must be tied to one and only one Program Select pins. Figure 2 below shows the different options that can be selected at startup. These seven different options allow the CS5462's PGA to be set up in either 10x or 50x mode and enable or disable the high pass filters in either of the voltage or the current channels.

	IGAIN		
P1	500mV$_{P-P}$	10x	no hpf
P2	100mV$_{P-P}$	50x	no hpf
P3	500mV$_{P-P}$	10x	hpf both
P4	100mV$_{P-P}$	50x	hpf both
P5	500mV$_{P-P}$	10x	hpf Ich
P6	100mV$_{P-P}$	50x	hpf Ich
P7	500mV$_{P-P}$	10x	hpf Vch

Figure 2. PGA Settings

During Startup the CS5462 will scan the IGAIN input pin and determine which Program Select output it is connected to and then set the PGA and HPF's accordingly.

4.2 Pulse-Rate Output

$\overline{E1}$ and $\overline{E2}$ pins provide a simple interface from which signed energy can be accumulated. $\overline{E1}$ and $\overline{E2}$ can be set to either stepper motor mode or mechanical counter mode. The connectivity of the FREQ pin determines the pulse output mode and also the maximum frequency for $\overline{E1}$ and $\overline{E2}$. Figure 3 below describes the options for $\overline{E1}$ and $\overline{E2}$.

	FREQ
P1	0.25 Hz / Step
P2	0.5 Hz / Step
P3	1 Hz / Step
P4	2 Hz / Step
P5	4 Hz / Step
P6	2 Hz / mech cnt
P7	16 Hz / mech cnt

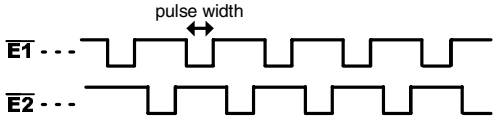
Figure 3. Pulse Output Settings

For all applications FREQ must be connected to one and only one of the Program Selects outputs (P1 - P7). The frequency setting chosen using the above table is equal to the set pulse rate frequency if and only if a full-scale signal is applied to each channel. As the input signal decreases the pulse rate and pulse width will decrease by a percentage equal to the product of the percentages of full-scale inputs across each channel. For example, if if FREQ is connected to P5, the maximum pulse output rate is 4 Hz. Assuming 500 mV is selected as full scale on each channel, 400 mV is measured on current and voltage channels. 400 mV is 80% of full scale. Since power is the product of current and voltage the pulse outputs will be 80% * 80% = 64% of full scale. Since 4Hz is the set full scale output rate, pulses should appear on $\overline{E1}$ and $\overline{E2}$ at a 64% * 4 Hz = 2.56 Hz rate.

4.2.1 Stepper Motor Format.

In stepper motor mode the CS5462 produces alternating pulses on $\overline{E1}$ and $\overline{E2}$. This pulse format is designed to directly drive a stepper motor. Each pin produces active-low pulses with frequency dependent pulse widths. The figure below shows the frequency and corresponding pulse width for each option.

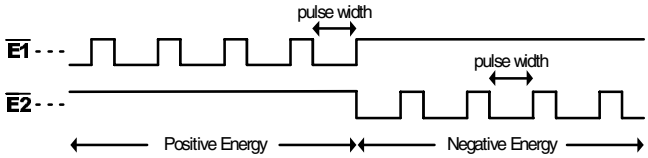
FREQ connected to:	P1	P2	P3	P4	P5
Frequency	0.25 Hz	0.5 Hz	1 Hz	2 Hz	4 Hz
Pulse Width	250 ms	250 ms	250 ms	250 ms	125 ms



4.2.2 Mechanical Counter Format

In mechanical counter mode, the CS5462 produces pulses on $\overline{E1}$ and $\overline{E2}$ which can be used to drive a bi-directional mechanical counter. Each pin produces active-low pulses which have pulse widths of 125 ms or 15 ms, depending on the frequency selected. In the figure below, the frequency and corresponding pulse width is shown for each option available. In this mode when energy is positive, the pulses appear on $\overline{E1}$; when energy is negative, pulses appear on $\overline{E2}$.

FREQ connected to:	P6	P7
Frequency	2 Hz	16 Hz
Pulse Width	125 ms	15 ms



4.3 Energy Direction Indicator

For either pulse output mode, the $\overline{NEG}$ pin can be used to indicate the direction of the energy calculated. The $\overline{NEG}$ pin is updated at the sample rate of the converter. If negative energy is detected the $\overline{NEG}$ pin will become active low and will remain active low until positive energy is detected.

4.4 Internal Calibration Option

For most power meter applications the standard accuracy requirements require the meter be calibrated to within a certain percentage. Calibrating a CS5462 meter can be done a number of ways. One calibration method is to externally adjust the front-end input circuit by using a potentiometer or resistor network. By adjusting the amount of gain in the resistor divider on the front end the energy outputs can be adjusted to fit the accuracy required. Although this method is available, it may be costly to add the additional components and the accuracy required is often difficult to achieve. As an alternative the CS5462 is designed to allow the user to calibrate the part without the need for external potentiometers or resistor networks. The CS5462 provides a digital on-chip calibration solution. This digital alternative can calibrate energy registration error to within 0.1% without any analog adjustments.

	CAL1	CAL0
P1	+4.2%	+0.6%
P2	+2.8%	+0.4%
P3	+1.4%	+0.2%
P4	0%	0%
P5	-1.4%	-0.2%
P6	-2.8%	-0.4%
P7	-4.2%	-0.6%

Figure 6. Calibration Options

This calibration is accomplished by connecting each Configuration Input pin, CAL1 and CAL0, to one of the Program Select Output pins, P1 - P7. At startup the CS5462 will scan the CAL1 and CAL0 pins to discern what connections are made, and then calibrate the gain accordingly.

CAL1 and CAL0 each have seven options which allows for 49 different steps of 0.2% between +4.8% and -4.8% of expected energy output. Before startup, CAL1 and CAL0 must each be connected to only one of the program select pins.

To Calibrate the CS5462:

1. Connect CAL1 and CAL0 to P4. This connection will adjust the energy outputs by 0%.

2. Apply known current and voltage signals to the inputs of the CS5462.

3. Measure the average pulse output frequency of $\overline{FOUT}$, $\overline{E1}$, or $\overline{E2}$.

4. The average frequency will be within some percentage of the expected frequency. Depending on the output of the uncalibrated chip, the CAL0 and CAL1 pins can be adjusted using the above options (see "User Defined Settings" on page 14 for more on calibration).

4.5 Power-on Reset

The CS5462 is equipped with internal circuitry that will put the chip into reset if power supply is lost. This is particularly useful in black-out or brown-out situations in which the power supply temporarily interrupted. The CS5462 will enter into reset if the power drops below 2.5 V. The chip will remain in reset until the supply rises to 4 V (See Figure 6) at

which time the CS5462 will configure itself and resume normal operation.

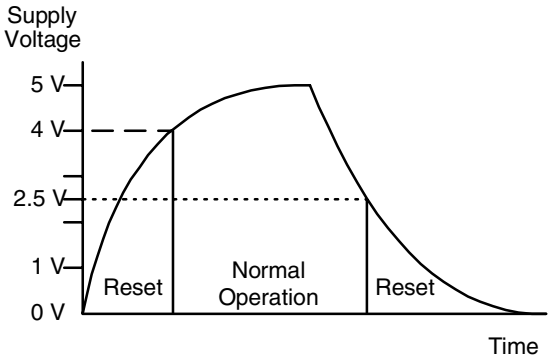


Figure 7. Power-on Reset

4.6 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier which can provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 8. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device, one between XIN and DGND, one between XOUT and DGND. Lead lengths should be minimized to reduce stray capacitance. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

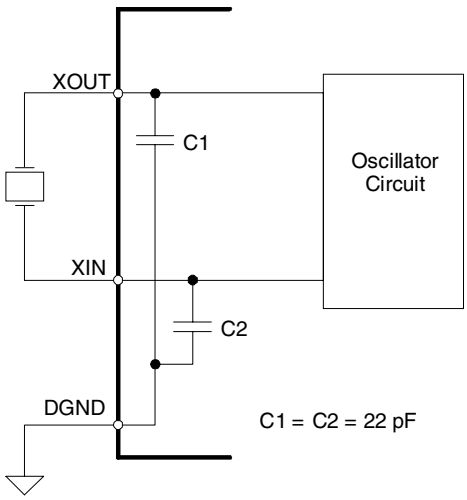


Figure 8. Oscillator Connection

4.7 User Defined Settings

EXAMPLE: Design a hybrid stepper motor meter with an 2 Hz maximum pulse output frequency on the $\overline{E1}$, $\overline{E2}$ pins with 500 mV_{P-P} signal on the inputs of the current and voltage channels and the high pass filter enabled on the current channel only. Using the figure below these settings can be selected with two connections.

	CAL1	CAL0	FREQ	IGAIN		
P1	+4.2%	+0.6%	0.25 Hz (stp)	10x	500mV	no hpf
P2	+2.8%	+0.4%	0.5 Hz (stp)	50x	100mV	no hpf
P3	+1.4	+0.2%	1 Hz (stp)	10x	500mV	hpf both
P4	0	0	2 Hz (stp)	50x	100mV	hpf both
P5	-1.4%	-0.2%	4 Hz (stp)	10x	500mV	hpf Ich
P6	-2.8%	-0.4%	4 Hz (mc)	50x	100mV	hpf Ich
P7	-4.2%	-0.6%	16 Hz (mc)	10x	500mV	hpf Vch

Figure 9. Calibration, Frequency Select, and PGA Select

By directly connecting FREQ with P4 and IGAIN with P5 the CS5462 is configured to drive a stepper motor with a maximum pulse output rate of 2 Hz, to support an input range of 50 $0mV_{P-P}$, and to remove all DC content on the current signals by enabling the HPFs on the Ich. The CS5462 is now ready for calibration.

Before applying power to the chip, connect the CAL0 and CAL1 pins to P4. This will select 0% + 0% = 0% gain adjustment. After making this connection the CS5462 is ready to be calibrated. Once power is applied the CS5462 will begin a startup sequence in which it will scan the FREQ, IGAIN, CAL0, and CAL1 pins. After determining which connections are made the FREQ, IGAIN, CAL0, and CAL1 pins will become high impedance inputs and the part will begin normal operation and start converting. If on-chip calibration is required place known voltages across the inputs on IIN± and VIN±.

For example, 150 mV_{RMS} = ~424.26 mV_{P-P} will be used for both the current and voltage inputs. 424.26 mV_{P-P} is ~84.853% of the maximum full scale input of both the current and voltage channels. With this input on both channels the expected pulse output frequency is 84.853% * 84.853% = 72% of full scale. This

means that $\overline{E1}$ and $\overline{E2}$ should have an average pulse output frequency of 2 Hz * 72% = 1.44 Hz and $\overline{FOUT}$ should have an average pulse output frequency of 10 kHz * 72% = 7.2 kHz. Assuming that $\overline{FOUT}$ is used for calibration (although the gain error will be the same for $\overline{E1}$ and $\overline{E2}$), $\overline{FOUT}$ should be measured to find the gain error. Suppose the measured pulse output frequency is 6.96 6kHz instead of 7. 2kHz. 6.99 6kHz is 96.76% of 7. 2kHz. This means that the gain error is 96.76% - 100% = -3.24%. This error can be calibrated out by connecting CAL1 to P2 and CAL0 to P2 (see Figure 7 for all connection options). This will adjust the pulse rate frequency by 2.8% + 0.4% = 3.2% (since the smallest calibration step size is 0.2%, 3.2% is the closest value that can offset the error of -3.24). After these connections are made the average pulse output frequency of $\overline{FOUT}$, $\overline{E1}$, and $\overline{E2}$ will have a gain error less than or equal to -0.04% of full scale.

CAL1 connected to: \ CAL0 connected to:	P1	P2	P3	P4	P5	P6	P7
P1	+4.8%	+4.6%	+4.4%	+4.2%	+4.0%	+3.8%	+3.6%
P2	+3.4%	+3.2%	+3.0%	+2.8%	+2.6%	+2.4%	+2.2%
P3	+2.0%	+1.8%	+1.6%	+1.4%	+1.2%	+1.0%	+0.8%
P4	+0.6%	+0.4%	+0.2%	+0.0%	-0.2%	-0.4%	-0.6%
P5	-0.8%	-1.0%	-1.2%	-1.4%	-1.6%	-1.8%	-2.0%
P6	-2.2%	-2.4%	-2.6%	-2.8%	-3.0%	-3.2%	-3.4%
P7	-3.6%	-3.8%	-4.0%	-4.2%	-4.4%	-4.6%	-4.8%

Figure 7. Power-on Reset

4.8 Basic Application Circuit Configurations

Figure 9 shows the CS5462 configured to measure power in a single-phase 2-wire system while operating in a single supply configuration. In this diagram, the shunt resistor used to monitor the line current is connected on the “Line” (hot) side of the power mains. In most residential power metering applications, the power meter’s current-sense shunt resistor is intentionally placed on the hot side of the power mains in order to detect a subscriber’s attempt to steal power. In this type of shunt-resistor configuration, the common-mode level of the CS5462 must be referenced to the hot side of the power line. This means that the common-mode potential of the CS5462 will typically oscillate to very high voltage levels, as well as very low voltage levels, with respect to earth ground potential.

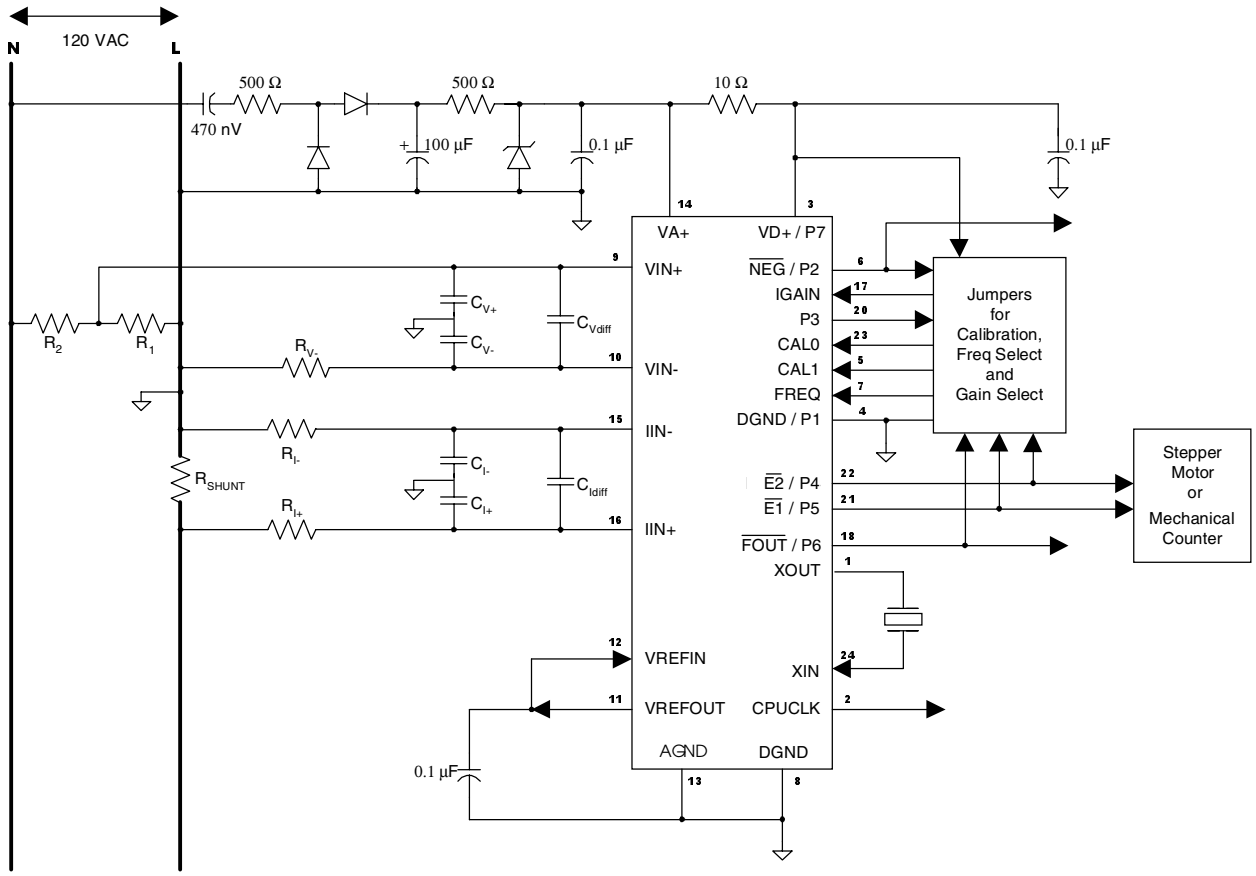
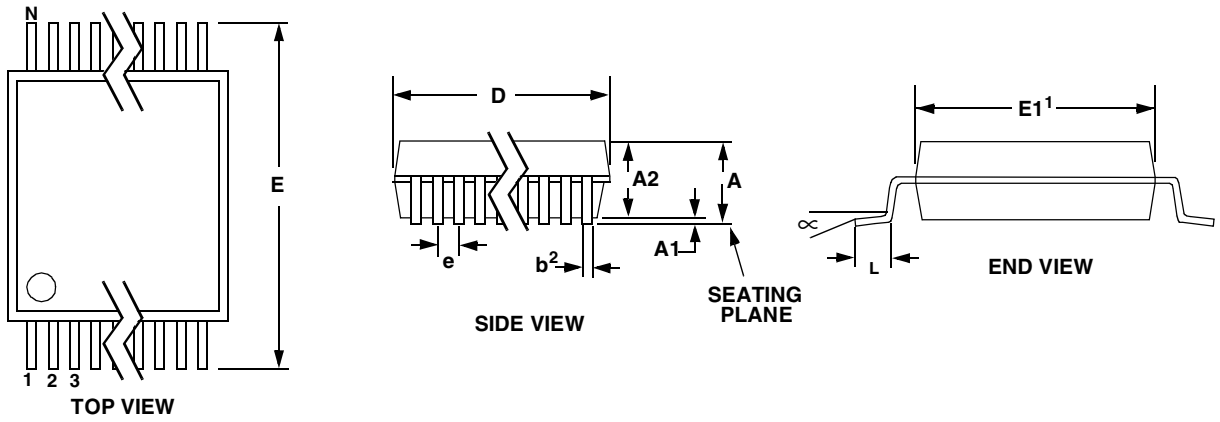


Figure 8. Typical Connection Diagram

5. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.0 7mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 a nd 0.25mm from lead tips.

6. REVISIONS

Revision	Date	Changes
A1	March 2003	Initial Release
PP1	13 October 2003	Initial release for Preliminary Product Information

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to **www.cirrus.com**