



FEATURES

- ## DESCRIPTION

This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LCXXB.

	24C01A	24C02A	24C04A
Organization	128 x 8	258 x 8	2 x 256 x 8
Write Protect	None	080-0FF	100-1FF
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

DIP

Pin	Signal	Pin	Signal
1	A0	8	V _{CC}
2	A1	7	WP*
3	A2	6	SCL
4	V _{SS}	5	SDA

8-lead SOIC

Pin	Signal	Pin	Signal
1	A0	8	V _{CC}
2	A1	7	WP*
3	A2	6	SCL
4	V _{SS}	5	SDA

14-lead SOIC

Pin	Signal	Pin	Signal
1	NC	14	NC
2	A0	13	V _{CC}
3	A1	12	WP
4	NC	11	NC
5	A2	10	SCL
6	V _{SS}	9	SDA
7	NC	8	NC

* "TEST" pin in 24C01A

The block diagram illustrates the internal architecture of the 24C02. It features a central **Control Logic** block at the bottom, which is connected to the **Slave Addr.** block and the **Data Buffer (FIFO)** block. The **Control Logic** also receives inputs from **A0**, **A1**, **A2**, and **WP** pins. It outputs an **Increment** signal to the **Pointers** block and an **A8** signal to the **Memory Array**. The **Slave Addr.** block is connected to the **SDA** line and the **Control Logic**. The **Data Buffer (FIFO)** block is connected to **VCC** and **VSS** and has a bidirectional connection to the **SDA** line. It also has a bidirectional connection to the **Data Reg.** block. The **Data Reg.** block is connected to the **Control Logic** and the **Pointers** block. The **Pointers** block is connected to the **Control Logic** and the **Memory Array**. It also receives a **VPP** input and outputs **A0 to A7** to the **Memory Array**. The **Memory Array** is connected to the **Pointers** block and the **R/W Amp** block. The **R/W Amp** block is connected to the **Memory Array** and the **SDA** line. It also receives a **VPP** input and has a bidirectional connection to the **Data Buffer (FIFO)** block.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
 All inputs and outputs w.r.t. V_{SS}-0.6V to V_{CC} +1.0V
 Storage temperature-65°C to +150°C
 Ambient temp. with power applied-65°C to +125°C
 Soldering temperature of leads (10 seconds) ...+300°C
 ESD protection on all pins..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0	No Function for 24C04A only, Must be connected to V _{CC} or V _{SS}
A0, A1, A2	Chip Address Inputs
V _{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	(24C01A only) V _{CC} or V _{SS}
WP	Write Protect Input
V _{CC}	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +5V (±10%)		Commercial	(C):	Tamb =	0°C to +70°C
		Industrial	(I):	Tamb =	-40°C to +85°C
		Automotive	(E):	Tamb =	-40°C to +125°C
Parameter	Symbol	Min.	Max.	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	IOL = 3.2 mA (SDA only)
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	
A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	μA	VIN = 0V to VCC
Output leakage current	ILO	—	10	μA	VOUT = 0V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICC Write	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0°C to +70°C
	ICC Write	—	4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E)
	ICC Read	—	750	μA	VCC = 5V, Tamb= (C), (I) and (E)
Standby current	ICCS	—	100	μA	SDA=SCL=Vcc=5V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

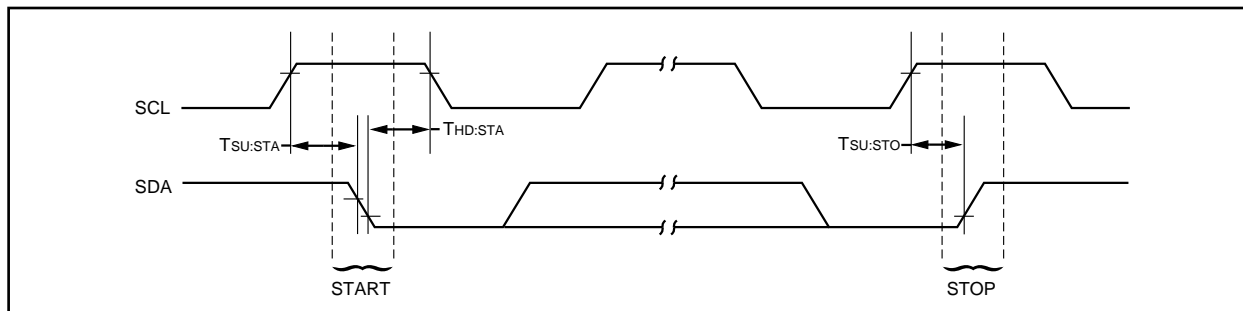
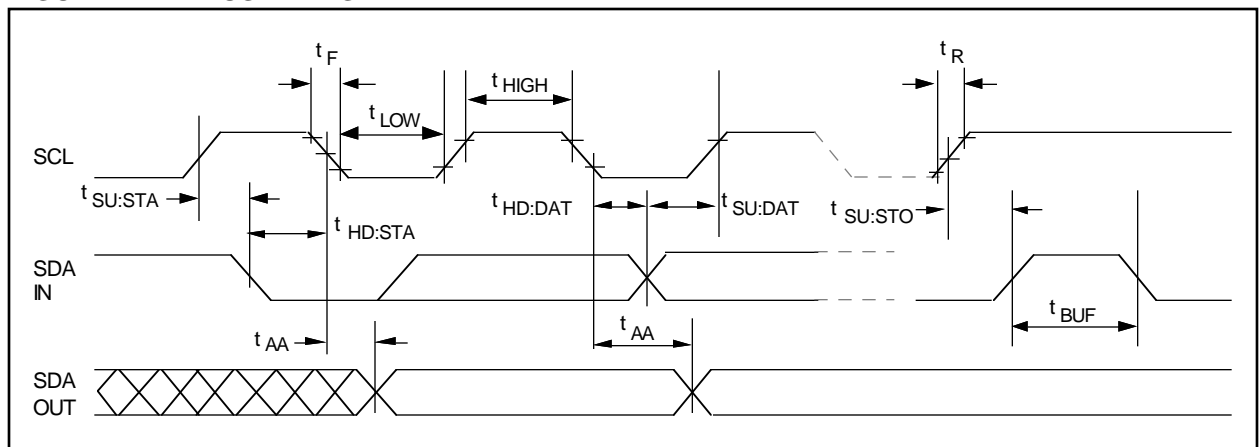


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ	Max.	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	T _{HIGH}	4000	—	—	ns	
Clock low time	T _{LOW}	4700	—	—	ns	
SDA and SCL rise time	T _R	—	—	1000	ns	
SDA and SCL fall time	T _F	—	—	300	ns	
START condition hold time	T _{HD:STA}	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	T _{SU:STA}	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	T _{HD:DAT}	0	—	—	ns	
Data input setup time	T _{SU:DAT}	250	—	—	ns	
Data output delay time	T _{AA}	300	—	3500		Note 1
STOP condition setup time	T _{SU:STO}	4700	—	—	ns	
Bus free time	T _{BUF}	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	T _I	—	—	100	ns	
Program cycle time	T _{WC}	—	.4 .4N	1 N	ms ms	Byte mode Page mode, N=# of bytes

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C01A/02A/04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A/02A/04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01/24C02s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Up to four 24C04As can be connected to the bus, selected by A1 and A2 chip address inputs. A0 must be tied to Vcc or Vss for the 24C04A. Other devices can be connected to the bus but require different device codes than the 24C01A/02A/04A (refer to section Slave Address).

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

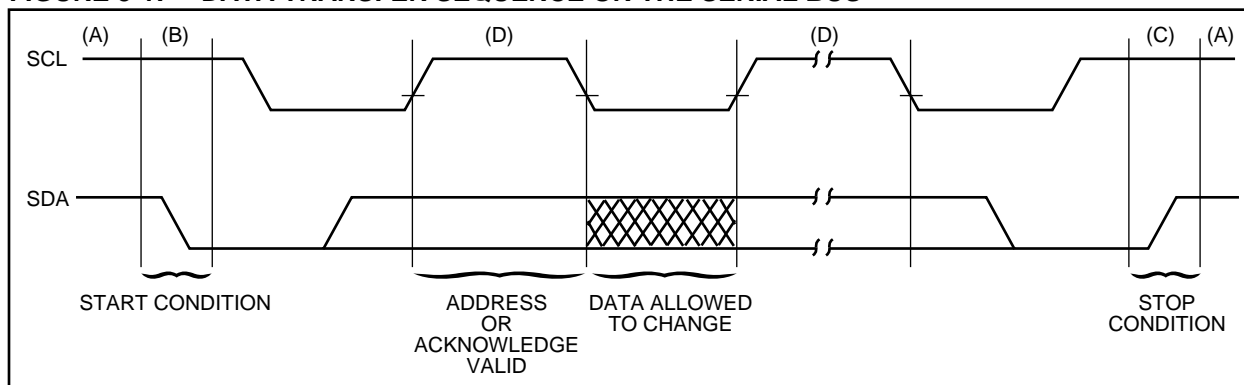
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A/02A/04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



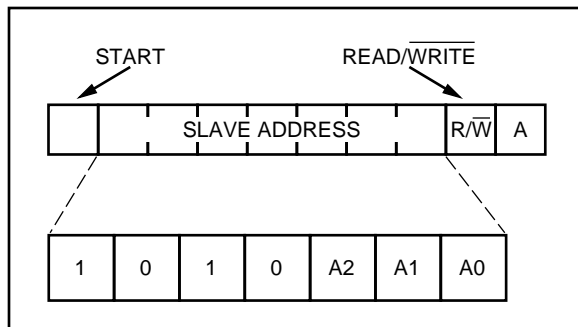
4.0 SLAVE ADDRESS

The chip address inputs A0, A1 and A2 of each 24C01A/02A/04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A/02A/04A a unique address. A0 is not used on the 24C04A and must be connected to either Vcc or Vss. Up to eight 24C01A or 24C02A devices and up to four 24C04A devices may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hard-wired logic levels of the selected 24C01A/02A/04A. After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A/02A/04A, followed by the chip address bits A0, A1 and A2. In the 24C04A, the seventh bit of that byte (A0) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A/02A/04A (see Figure 4-1).

The 24C01A/02A/04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C01A/02A/04A.

Following the START signal from the master, the device code (4-bits), the slave address (3-bits), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A/02A/04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A/02A/04A. After receiving the acknowledge of the 24C01A/02A/04A, the master device transmits the data word to be written into the addressed memory location. The 24C01A/02A/04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A/02A/04A (see Figure 6-1).

6.0 PAGE PROGRAM MODE

To program the 24C01A/02A/04A, the master sends addresses and data to the 24C01A/02A/04A which is the slave (see Figure 6-1 and Figure 6-2). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A/02A/04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The A0 bit transmitted with the slave address is the ninth bit of the address pointer for the 24C04A). The 24C01A/02A/04A will generate an acknowledge after every 8-bits received and store them consecutively in a RAM buffer until a STOP condition is detected. This STOP condition initiates the internal programming cycle. The RAM buffer is 2 bytes for the 24C01A/02A and 8 bytes for the 24C04A. If more than 2 bytes are transmitted by the master to the 24C01A/02A, the device will not acknowledge the data transfer and the sequence will be aborted. If more than 8 bytes are transmitted by the master to the 24C04A, it will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received data bytes in the page buffer will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8 for 24C04A, 2 for 24C01A/02A).

FIGURE 6-1: BYTE WRITE

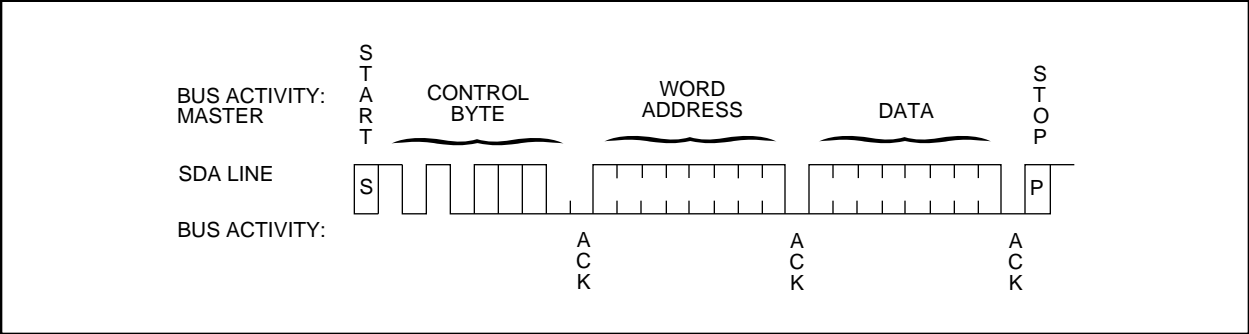
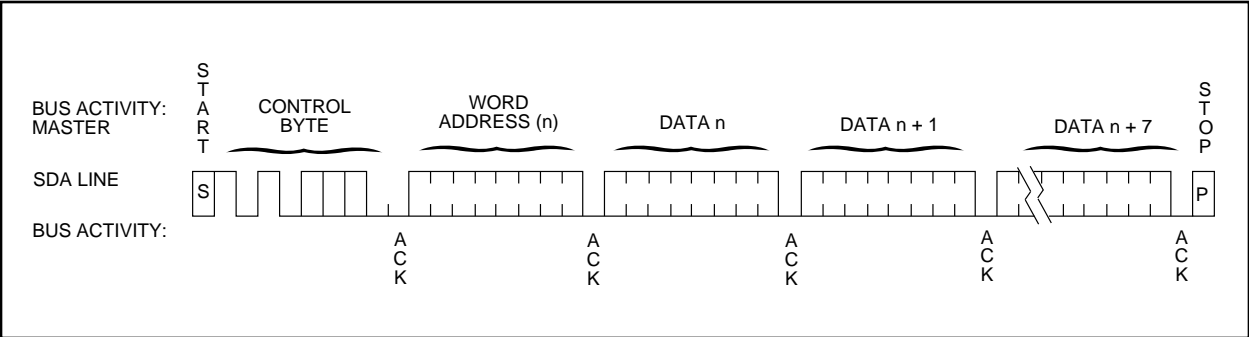


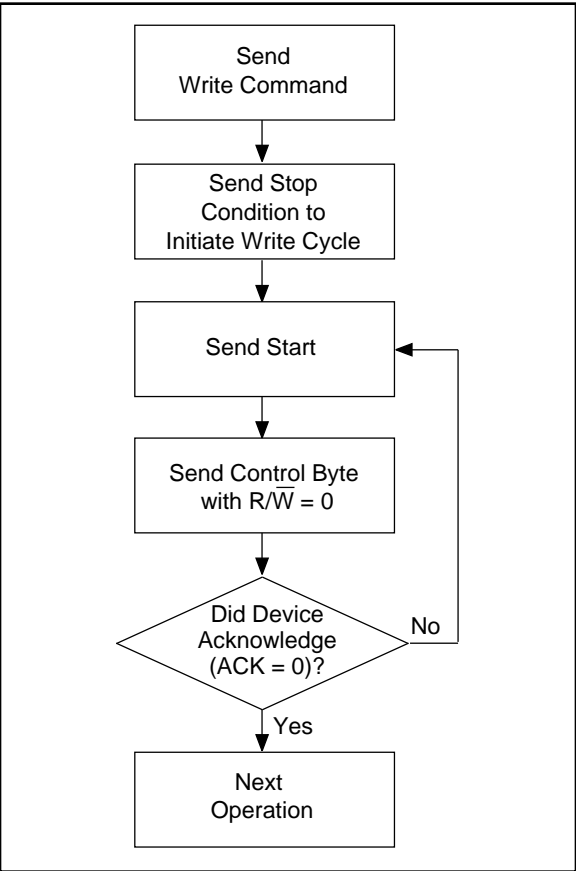
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A or 24C04A is connected to VCC (+5V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A/04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted. Polarity of the WP pin has no effect on the 24C01A.

9.0 READ MODE

This mode illustrates master device reading data from the 24C01A/02A/04A.

As can be seen from Figure 9-2 and Figure 9-3, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C01A/02A/04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at the current address (see Figure 9-1) and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 9-1: CURRENT ADDRESS READ

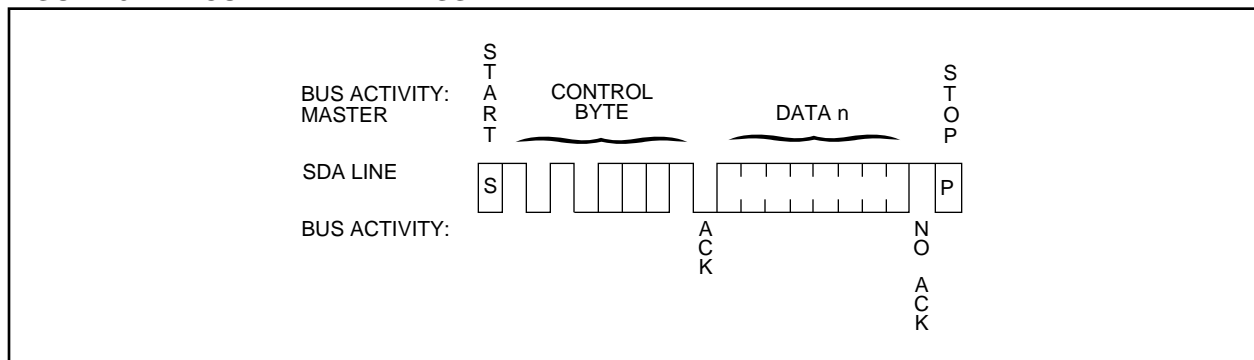


FIGURE 9-2: RANDOM READ

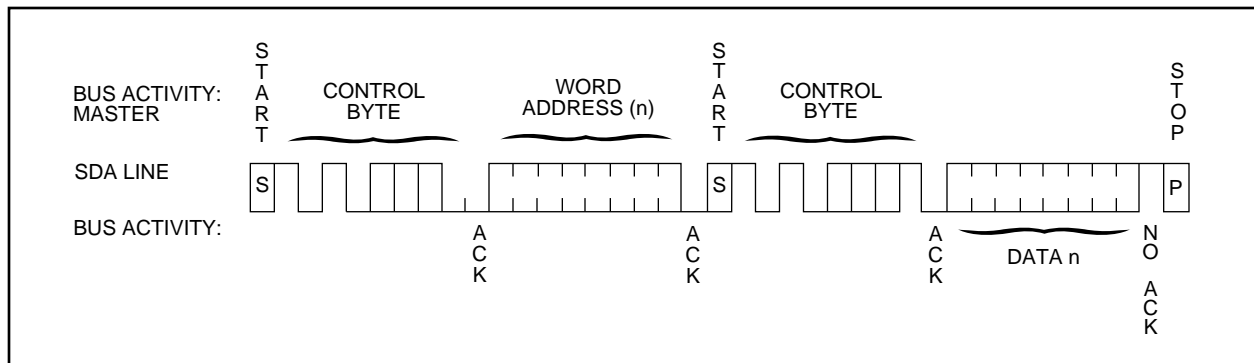
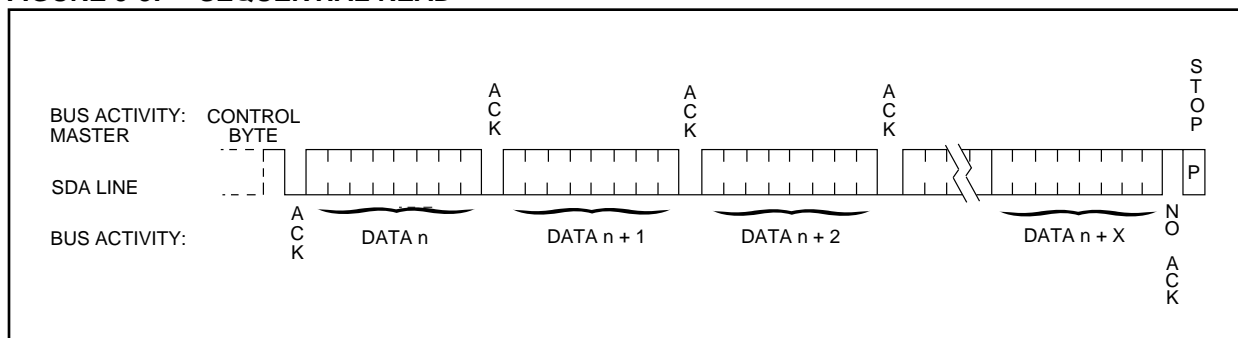


FIGURE 9-3: SEQUENTIAL READ



10.0 PIN DESCRIPTION

10.1 A0, A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 24C04 A0 is no function.

Up to eight 24C01A/02A's or up to four 24C04A's can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

10.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

10.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

10.4 WP Write Protection

This pin must be connected to either Vcc or Vss for 24C02A or 24C04A. It has no effect on 24C01A.

If tied to Vcc, PROGRAM operations onto the upper memory block will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long; the 24C01A/02A page is 2 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each. The 24C01A and 24C02A each have only one block.

NOTES

24C01A/02A/04A

24C01A/02A/04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C01A/02A/04A	-	/P	
			Package:
			P = Plastic DIP
			SN = Plastic SOIC (150 mil Body), 8-lead
			SM = Plastic SOIC (207 mil Body), 8-lead
			SL = Plastic SOIC (150 mil Body), 14-lead, 24C04A only
			Temperature Range:
			Blank = 0°C to +70°C
			I = -40°C to +85°C
			E = -40°C to +125°C
			Device:
			24C01A 1K CMOS Serial EEPROM
			24C01AT 1K CMOS Serial EEPROM (Tape and Reel)
			24C02A 2K CMOS Serial EEPROM
			24C02AT 2K CMOS Serial EEPROM (Tape and Reel)
			24C04A 4K CMOS Serial EEPROM
			24C04AT 4K CMOS Serial EEPROM (Tape and Reel)

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: <http://www.mchip.com/biz/mchip>

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas

Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 214 991-7177 Fax: 214 991-8588

Dayton

Microchip Technology Inc.
35 Rockridge Road
Englewood, OH 45322
Tel: 513 832-2543 Fax: 513 832-2841

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 455
Irvine, CA 92715
Tel: 714 263-1888 Fax: 714 263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

AMERICAS (continued)

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

ASIA/PACIFIC

Hong Kong

Microchip Technology
Unit No. 3002-3004, Tower 1
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

Korea

Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore

Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan

Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 0 1628 851077 Fax: 44 0 1628 850259

France

Arizona Microchip Technology SARL
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Pegaso Ingresso No. 2
Via Paracelso 23, 20041
Agrate Brianza (MI) Italy
Tel: 39 039 689 9939 Fax: 39 039 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

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