

## High-Speed CMOS Logic Dual 2- to 4-Line Decoder/Demultiplexer

September 1997 - Revised October 2003

### Features

- Multifunction Capability
  - Binary to 1 of 4 Decoders or 1 to 4 Line Demultiplexer
- Active Low Mutually Exclusive Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$
- Memory Decoding, Data Routing, Code Conversion

### Description

The 'HC139 and 'HCT139 devices contain two independent binary to one of four decoders each with a single active low enable input ( $\overline{1E}$  or  $\overline{2E}$ ). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally high outputs to go low.

If the enable input is high all four outputs remain high. For demultiplexer operation the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded. This device is functionally the same as the CD4556B and is pin compatible with it.

The outputs of these devices can drive 10 low power Schottky TTL equivalent loads. The HCT logic family is functionally as well as pin equivalent to the LS logic family.

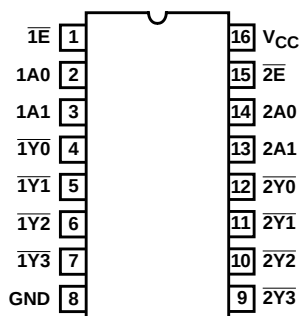
### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC139F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HCT139F3A | -55 to 125       | 16 Ld CERDIP |
| CD74HC139E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC139M    | -55 to 125       | 16 Ld SOIC   |
| CD74HC139MT   | -55 to 125       | 16 Ld SOIC   |
| CD74HC139M96  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT139E   | -55 to 125       | 16 Ld PDIP   |
| CD74HCT139M   | -55 to 125       | 16 Ld SOIC   |
| CD74HCT139MT  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT139M96 | -55 to 125       | 16 Ld SOIC   |

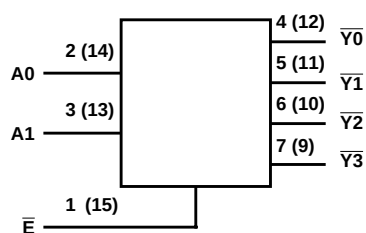
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC139, CD54HCT139  
(CERDIP)  
CD74HC139, CD74HCT139  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram

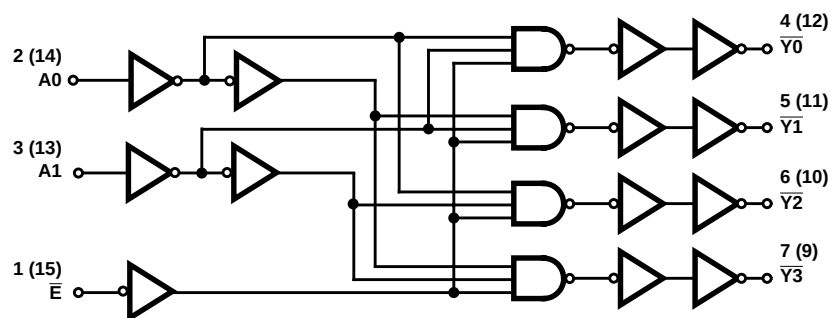


TRUTH TABLE

| INPUTS ENABLE SELECT |    |    | OUTPUTS     |             |             |             |
|----------------------|----|----|-------------|-------------|-------------|-------------|
| $\bar{E}$            | A1 | A0 | $\bar{Y}_3$ | $\bar{Y}_2$ | $\bar{Y}_1$ | $\bar{Y}_0$ |
| 0                    | 0  | 0  | 1           | 1           | 1           | 0           |
| 0                    | 0  | 1  | 1           | 1           | 0           | 1           |
| 0                    | 1  | 0  | 1           | 0           | 1           | 1           |
| 0                    | 1  | 1  | 0           | 1           | 1           | 1           |
| 1                    | X  | X  | 1           | 1           | 1           | 1           |

X = Don't Care, Logic 1 = High, Logic 0 = Low

## Logic Diagram



# CD54HC139, CD74HC139, CD54HCT139, CD74HCT139

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 E (PDIP) Package ..... 67  
 M (SOIC) Package ..... 73  
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |      |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|------|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP  | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |      |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -    | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -    | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -    | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -    | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -    | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -    | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -    | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -    | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -    | -    | 5.9           | -    | 5.9            | -    | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| -4                                      |                 |                                    | 4.5                 | 3.98                | -    | -    | 3.84 | -             | 3.7  | -              | V    |       |
| -5.2                                    |                 |                                    | 6                   | 5.48                | -    | -    | 5.34 | -             | 5.2  | -              | V    |       |
| High Level Output Voltage<br>TTL Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -    | ±0.1 | -             | ±1   | -              | ±1   | μA    |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -    | 8    | -             | 80   | -              | 160  | μA    |

# CD54HC139, CD74HC139, CD54HCT139, CD74HCT139

## DC Electrical Specifications (Continued)

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| HCT TYPES                                                      |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> and GND            | 0                   | 5.5                 | -    |     | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|-------|------------|
| All   | 0.7        |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                              | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|----------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                        |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                               |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>A0, A1 to Outputs | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 145 | -             | 180 | -              | 220 | ns    |
|                                        |                                     |                       | 4.5                 | -    | -   | 29  | -             | 36  | -              | 44  | ns    |
|                                        |                                     |                       | 6                   | -    | -   | 25  | -             | 31  | -              | 38  | ns    |
| $\overline{E}$ to Outputs              | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 135 | -             | 170 | -              | 205 | ns    |
|                                        |                                     |                       | 4.5                 | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
|                                        |                                     |                       | 6                   | -    | -   | 23  | -             | 29  | -              | 35  | ns    |
| Select to Output                       | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 15pF | 5                   | -    | 12  | -   | -             | -   | -              | -   | ns    |
| Enable to Output                       | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |

# CD54HC139, CD74HC139, CD54HCT139, CD74HCT139

## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                   | SYMBOL             | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO<br>85°C |     | -55°C TO<br>125°C |     | UNITS |
|---------------------------------------------|--------------------|---------------------|-----------------|------|-----|-----|------------------|-----|-------------------|-----|-------|
|                                             |                    |                     |                 | MIN  | TYP | MAX | MIN              | MAX | MIN               | MAX |       |
| Output Transition Time (Figure 1)           | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 75  | -                | 95  | -                 | 110 | ns    |
|                                             |                    |                     | 4.5             | -    | -   | 15  | -                | 19  | -                 | 22  | ns    |
|                                             |                    |                     | 6               | -    | -   | 13  | -                | 16  | -                 | 19  | ns    |
| Power Dissipation Capacitance, (Notes 3, 4) | $C_{PD}$           | -                   | 5               | -    | 55  | -   | -                | -   | -                 | -   | pF    |
| Input Capacitance                           | $C_{IN}$           | -                   | -               | -    | -   | 10  | -                | 10  | -                 | 10  | pF    |
| <b>HCT TYPES</b>                            |                    |                     |                 |      |     |     |                  |     |                   |     |       |
| Propagation Delay                           |                    |                     |                 |      |     |     |                  |     |                   |     |       |
| A0, A1 to Outputs                           | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 34  | -                | 43  | -                 | 51  | ns    |
| $\bar{E}$ to Outputs                        | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 34  | -                | 43  | -                 | 51  | ns    |
| Select to Output                            | $t_{PLH}, t_{PHL}$ | $C_L = 15\text{pF}$ | 5               | -    | 14  | -   | -                | -   | -                 | -   | ns    |
| Enable to Output                            | $t_{PLH}, t_{PHL}$ | $C_L = 15\text{pF}$ | 5               | -    | 14  | -   | -                | -   | -                 | -   | ns    |
| Output Transition Time (Figure 2)           | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -                | 19  | -                 | 22  | ns    |
| Power Dissipation Capacitance, (Notes 3, 4) | $C_{PD}$           | -                   | 5               | -    | 59  | -   | -                | -   | -                 | -   | pF    |
| Input Capacitance                           | $C_{IN}$           | -                   | -               | -    | -   | 10  | -                | 10  | -                 | 10  | pF    |

NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per decoder/demux.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where:  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

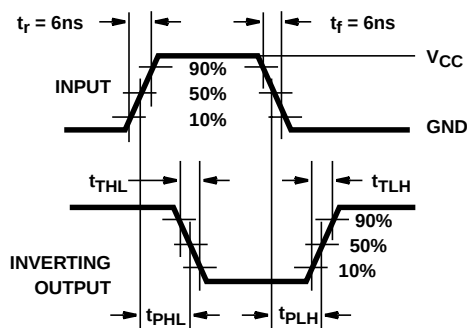


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

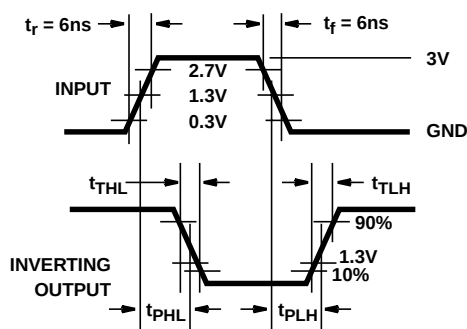


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)       |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------|
| <a href="#">CD54HC139F</a>    | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HC139F                |
| CD54HC139F.A                  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HC139F                |
| <a href="#">CD54HC139F3A</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409201EA<br>CD54HC139F3A |
| CD54HC139F3A.A                | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409201EA<br>CD54HC139F3A |
| <a href="#">CD54HCT139F</a>   | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT139F               |
| CD54HCT139F.A                 | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT139F               |
| <a href="#">CD54HCT139F3A</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT139F3A             |
| CD54HCT139F3A.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT139F3A             |
| <a href="#">CD74HC139E</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC139E                |
| CD74HC139E.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC139E                |
| <a href="#">CD74HC139M</a>    | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC139M                    |
| <a href="#">CD74HC139M96</a>  | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC139M                    |
| CD74HC139M96.A                | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC139M                    |
| <a href="#">CD74HCT139E</a>   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT139E               |
| CD74HCT139E.A                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT139E               |
| CD74HCT139EE4                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT139E               |
| <a href="#">CD74HCT139M</a>   | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT139M                   |
| <a href="#">CD74HCT139M96</a> | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT139M                   |
| CD74HCT139M96.A               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT139M                   |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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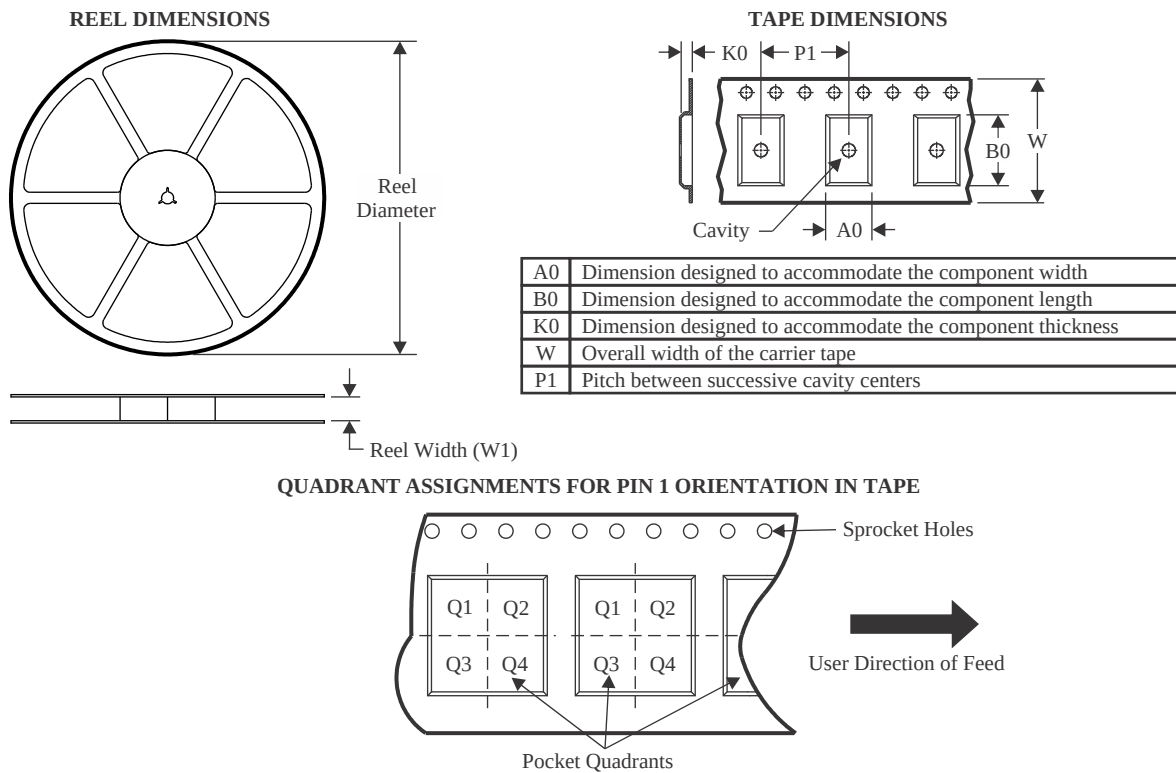
**OTHER QUALIFIED VERSIONS OF CD54HC139, CD54HCT139, CD74HC139, CD74HCT139 :**

- Catalog : [CD74HC139](#), [CD74HCT139](#)
- Military : [CD54HC139](#), [CD54HCT139](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

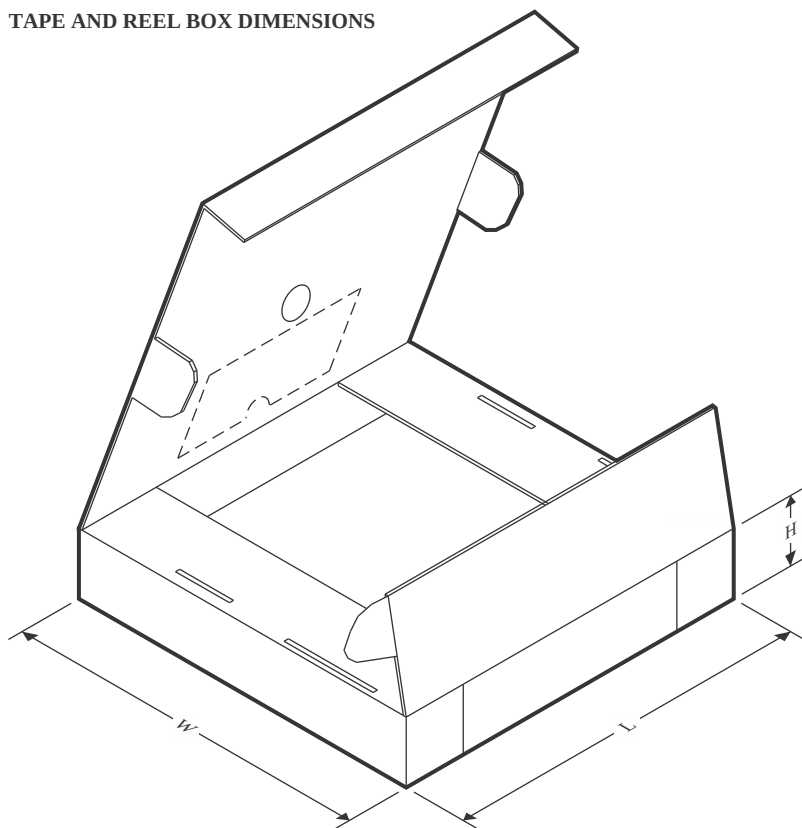


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC139M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT139M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC139M96  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| CD74HCT139M96 | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |

## TUBE

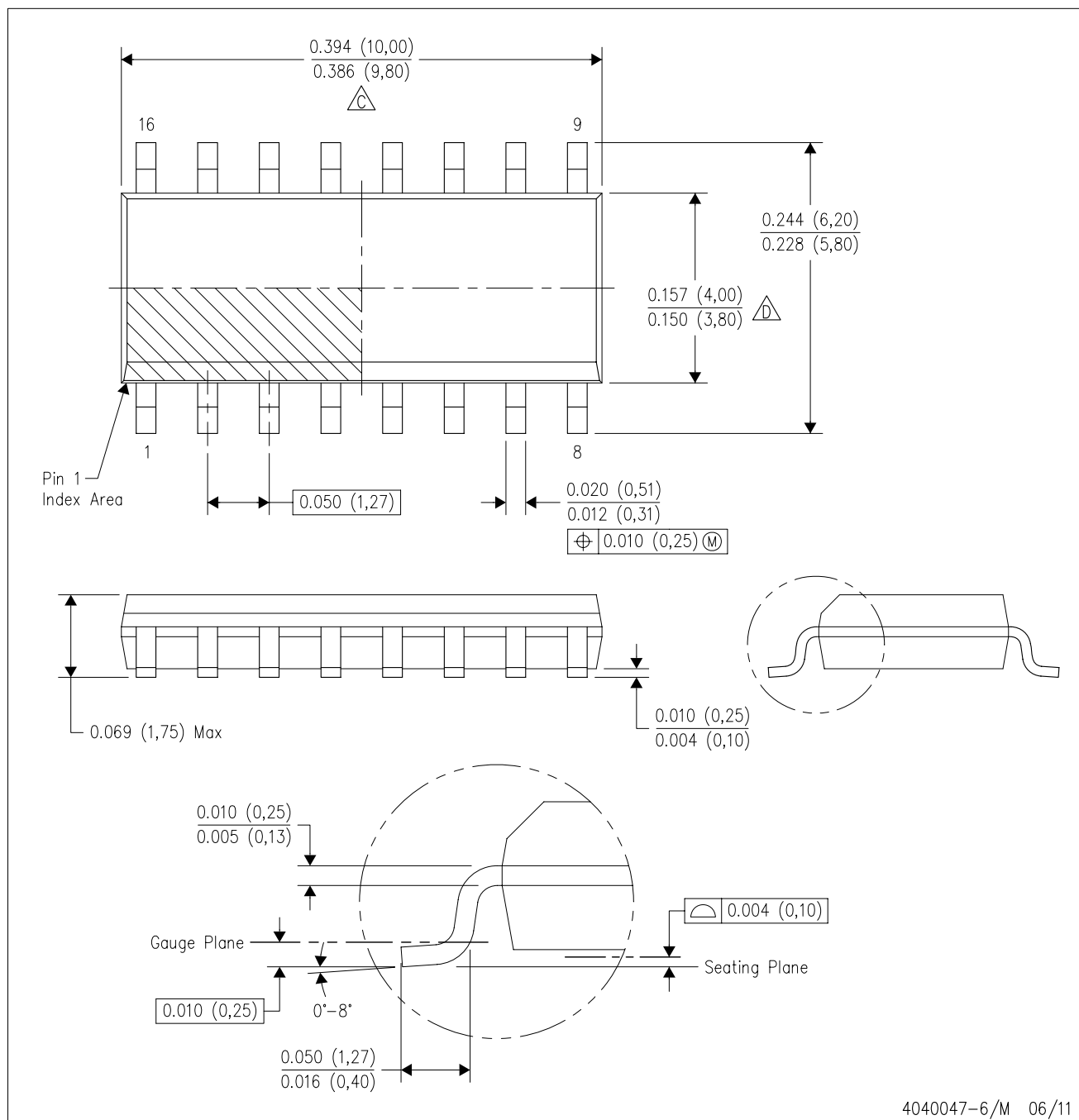


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC139E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC139E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC139E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC139E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT139EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



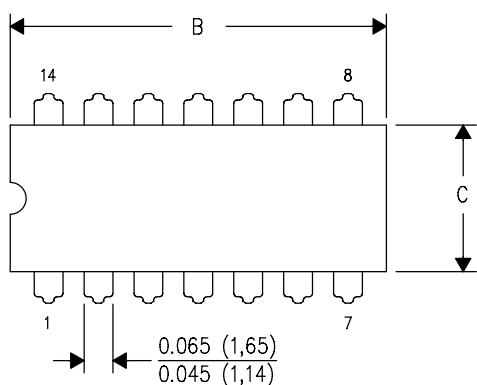
4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

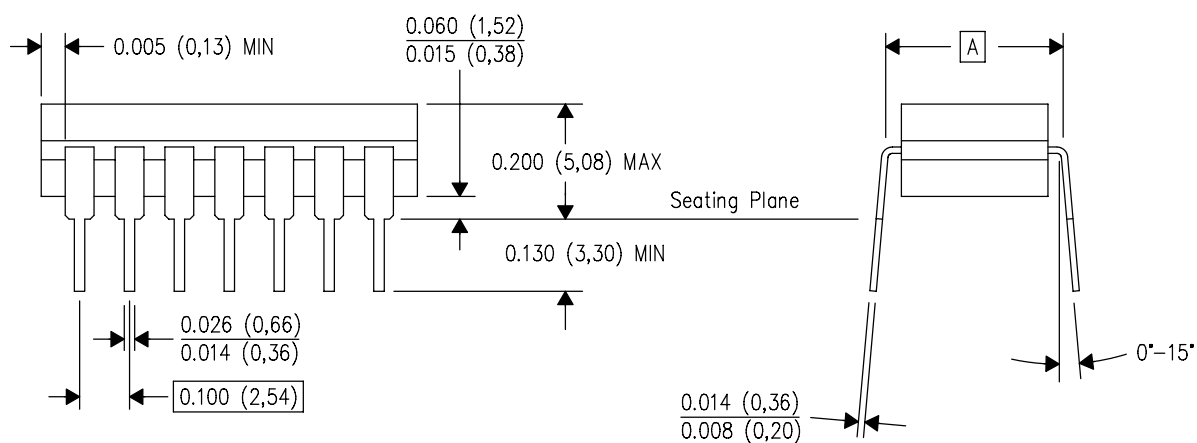
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



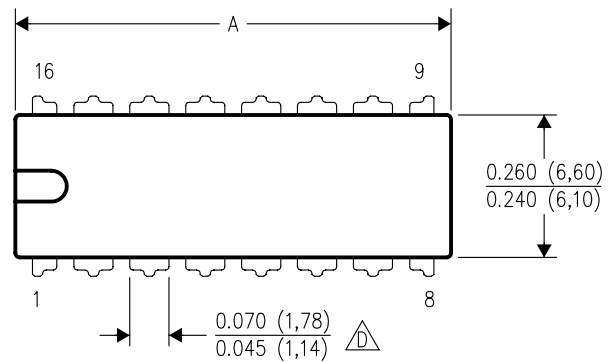
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

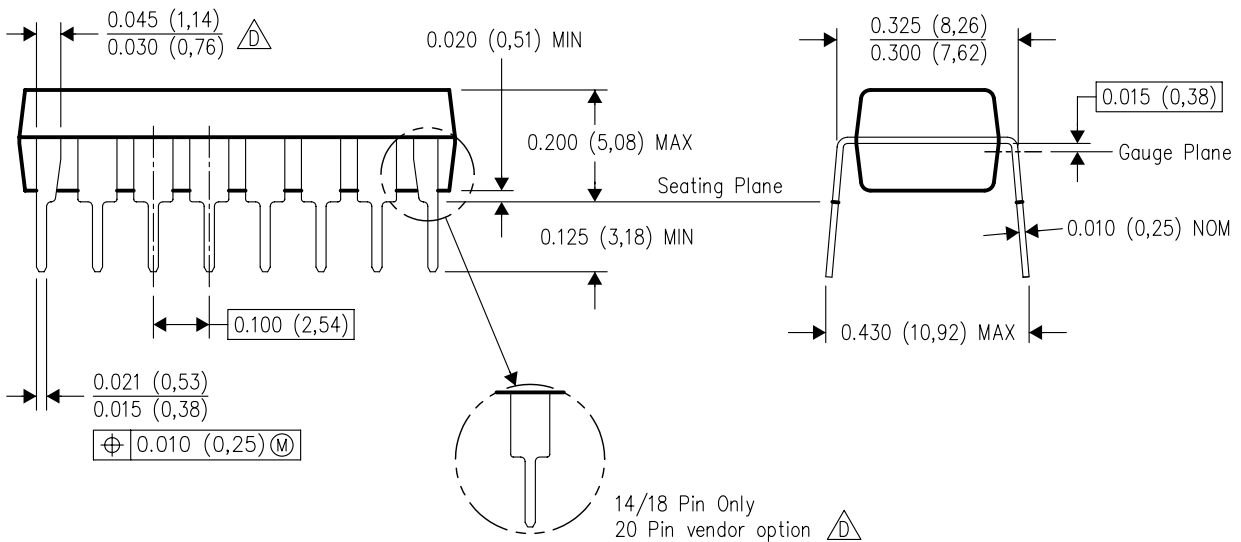
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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